EECS 598-008 & EECS 498-008: Intelligent Programming Systems

Lecture 11

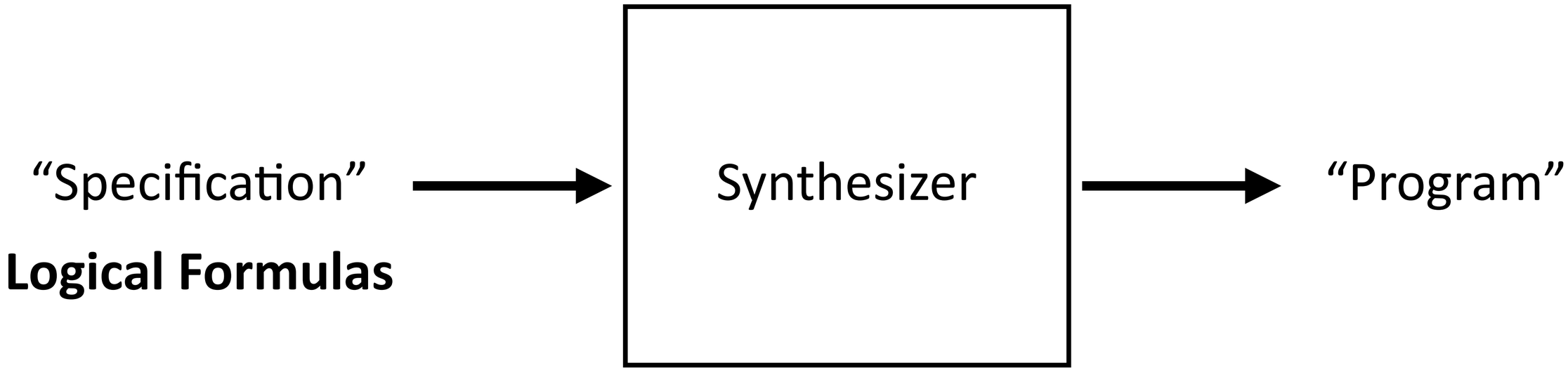
Announcements

- No lecture on Thursday (office hour instead)
- A3 due **midnight Wednesday (tomorrow)**
- First presentation Tuesday Oct 12
  - First paper review due **noon Monday Oct 11**
- Presentations
  - Speakers try to be in-person
- Friday discussion section
  - Discuss presentations with speakers in coming week
  - Schedule in advance if speakers want to discuss
  - Other students do not need to attend

So Far..

- Inductive program synthesis
  - Based on syntax-guided synthesis
  - Search space: DSL
  - Specification: examples
  - Search technique: top-down/bottom-up
  - Pruning: SMT-based deduction/equivalence class reduction
  - Prioritization: ranking/statistical models
  - Generalization: ranking/interaction/multi-modality

Today: Logical Specifications



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	strict sorted list insert	14	8	14.1	0.18
	merge sort	9	11	14.3	2.1
JEN	BST find	51	6	64.8	0.09
	bin. heap 1-element	80	5	61.6	0.02
	bin. heap find	76	6	51.9	0.38
MYTH	sorted list insert	12	8	0.12	0.25
	list rm adjacent dupl.	13	5	0.07	1.33
	BST insert	20	8	0.37	0.91
λ^2	list remove duplicates	7	13	231	0.36
	list drop	6	11	316.4	0.1
	tree find	12	6	4.7	0.29
ESC	list rm adjacent dupl.	n/a	5	1	1.33
	tree create balanced	n/a	7	0.24	0.14
	list duplicate each	n/a	7	0.16	0.05
MYTH2	BST insert	n/a	8	1.81	0.91
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	tree count nodes	n/a	4	0.45	0.20

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… which is fundamentally a problem for any inductive synthesis tool

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  - Good examples are not always easy to provide
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  - For safety critical domains, inductive specifications (alone) may not be a good idea
- Use complete specifications
  - To fully characterize function behavior

Pre and Postconditions

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- Post is a promise made by the program, assuming precondition holds
  - After P terminates, its output satisfies the postcondition

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  - $(out = x \vee out = y) \wedge out \geq x \wedge out \geq y$?

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    - Not a full spec. Consider input [5,4,3,2,1] and output [0,0,0,0,0]

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Essentially, out is a permutation of arr

- p maps each element in out to some element in arr
- I.e., i-th element in out maps to $p(i)$-th element in arr

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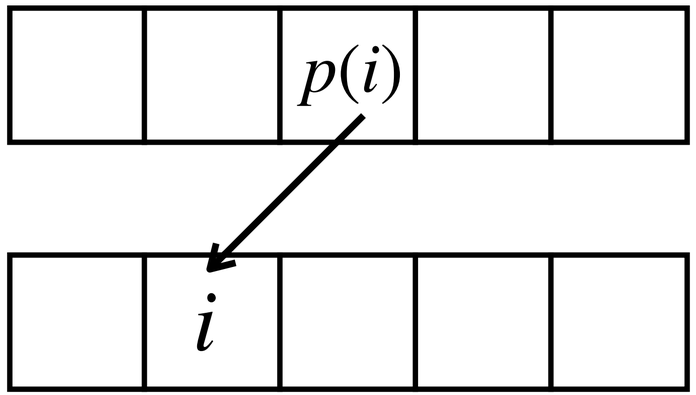

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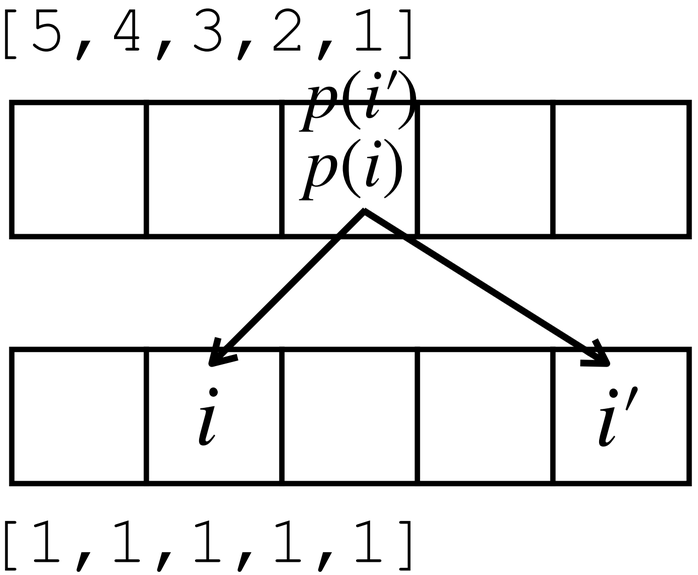
But this alone is not enough, because multiple elements in output may be mapped from the same input



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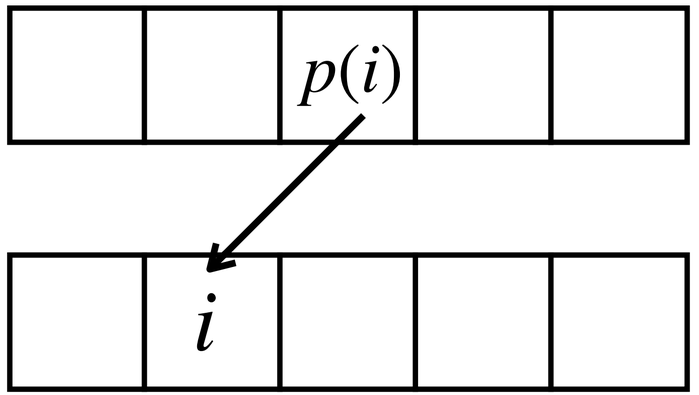

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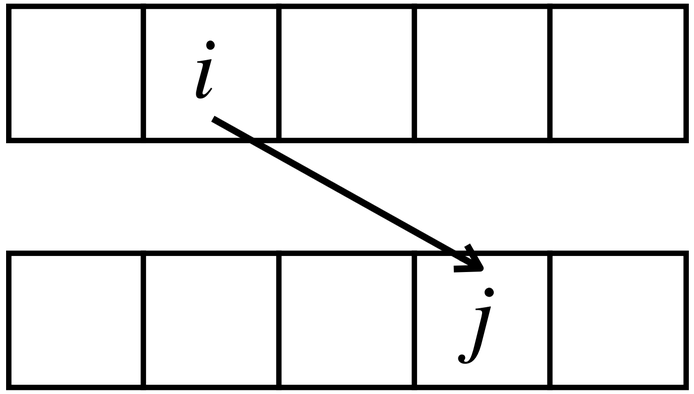
Every element in input maps to some element in output

$i = p(j)$



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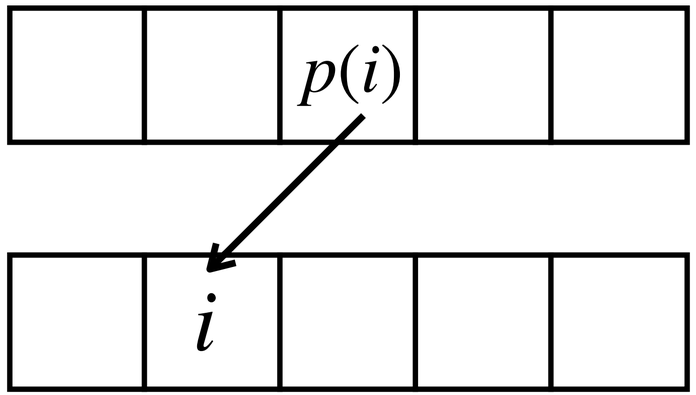

Pre and Postconditions Recap

- Take-away:
  - Pre/post can fully specify a program
  - But it’s not always easy to write pre and post

Program Synthesis From Pre/Postconditions

- Once we can specify program behaviors using pre and post
  - Verification: given a program and a spec, check if program satisfies spec
  - Synthesis: given a spec, generate program that satisfies spec

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- Today's lecture: synthesis
  - Counterexample Guided Inductive Synthesis (CEGIS)
  - CEGIS relies on verification

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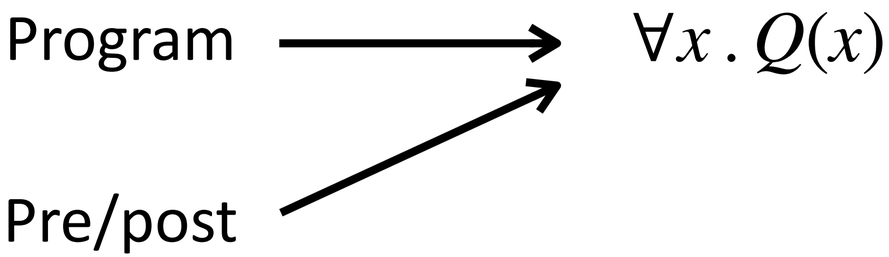
- One popular approach: constraint-based approach

Constraint-based Program Verification

- Goal: given program P, a precondition, and a postcondition, prove for that all inputs x satisfying pre, $P(x)$ satisfies post
- Basic idea: convert P, pre, and post into a logical formula $\phi : \forall x \,.\, Q(x)$



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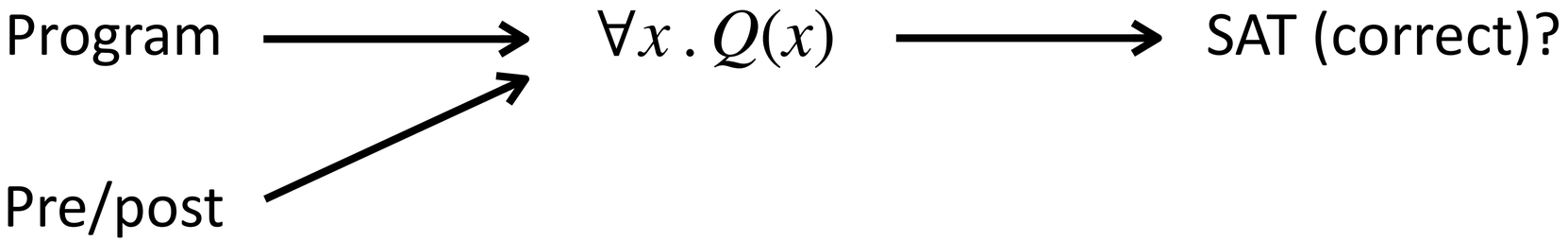

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- We have pretty good SMT solvers for solving formulas of the form $\forall x \,.\, Q(x)$
- Many techniques are based on this idea: model checking, symbolic execution, …
- We will not go into details

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From Program Verification to Program Synthesis

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  - Solving formula: $\exists P \,.\, \forall x \,.\, Q(P, x)$
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  - Can we solve synthesis just like we solve program verification?

Solving Program Synthesis By Solving Quantifier Alternation

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$$\exists P \,.\, \forall x \,.\, Q(P, x)$$

“program” “inputs” “P behaves correctly on x”

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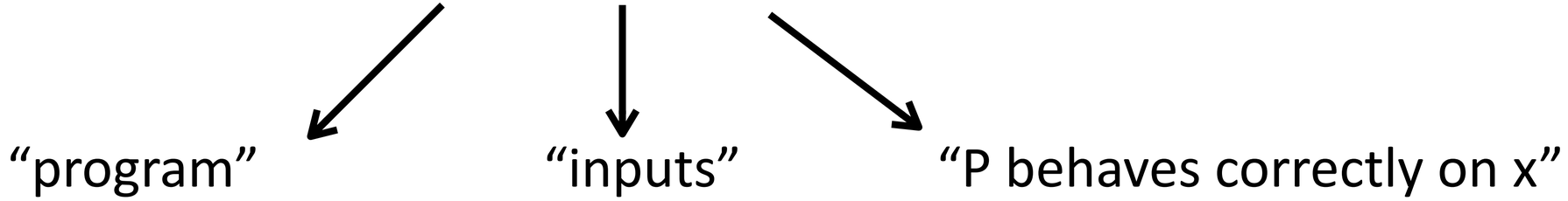

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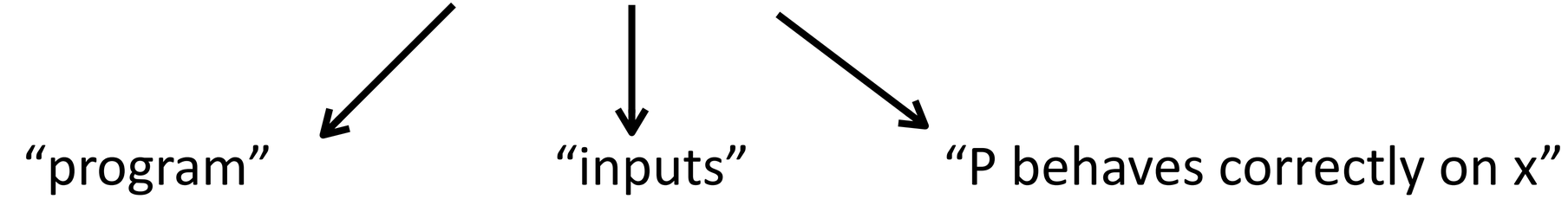

- Yes, if one can solve this formula
- But this is significantly more challenging compared to solving $\forall x \,.\, Q(P, x)$
  - Because it involves quantifier alternation
  - CEGIS comes to rescue!

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  - Would this work (and why)? What do we need for it to work?

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- CEGIS idea: use a checker that can produce counterexamples!

Counterexample Guided Inductive Synthesis (CEGIS)

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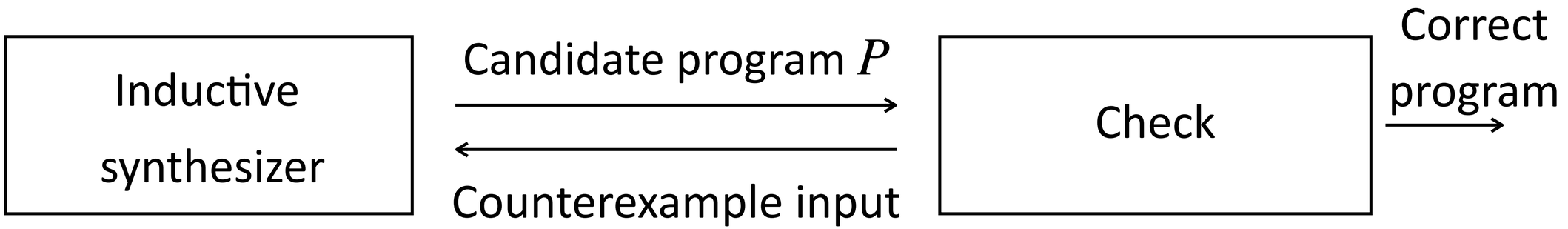

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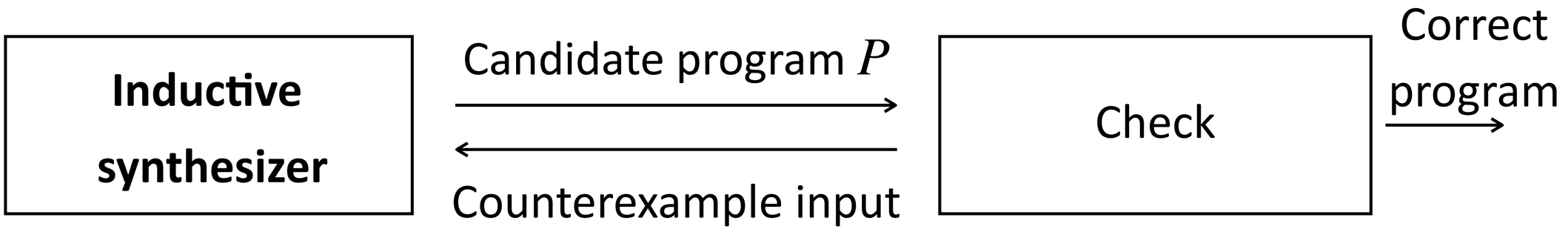

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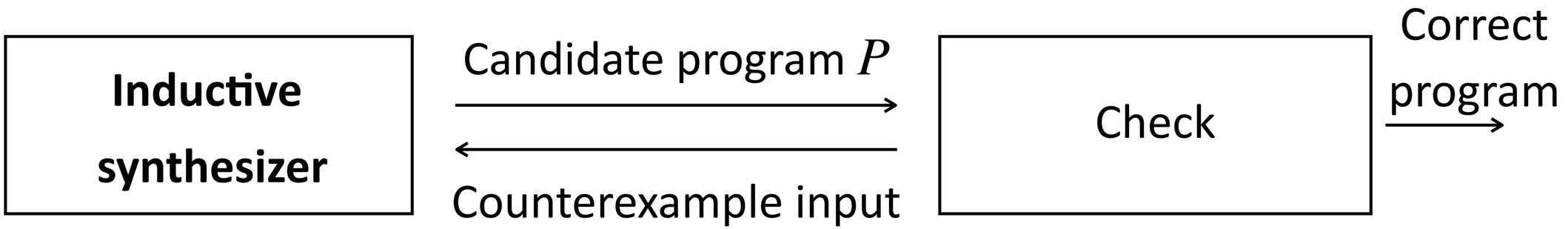

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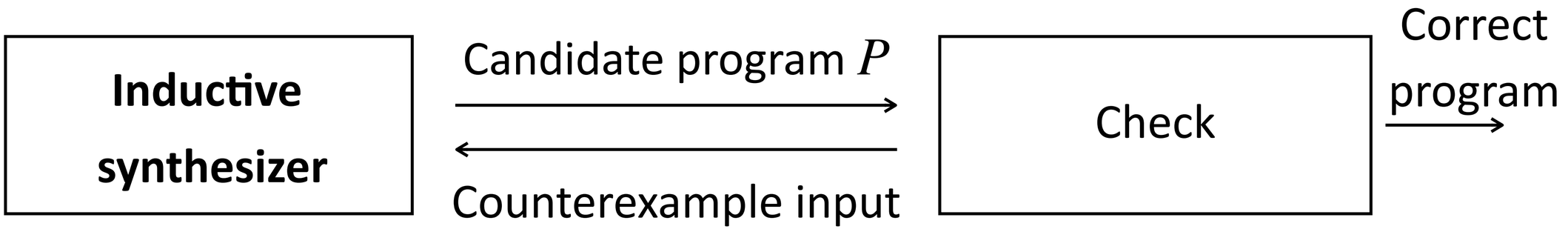

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  - Initially, no examples —> randomly guess one

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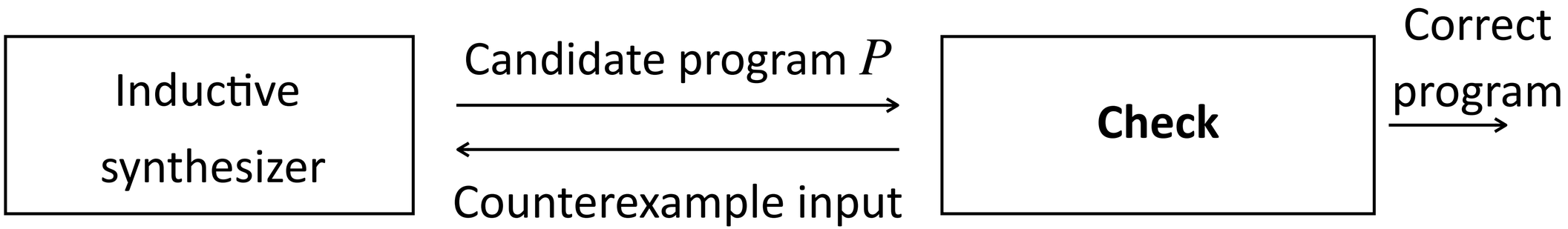

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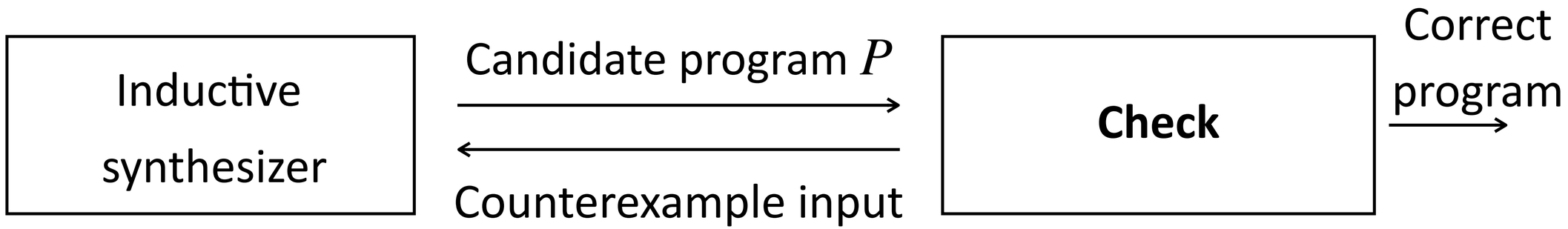

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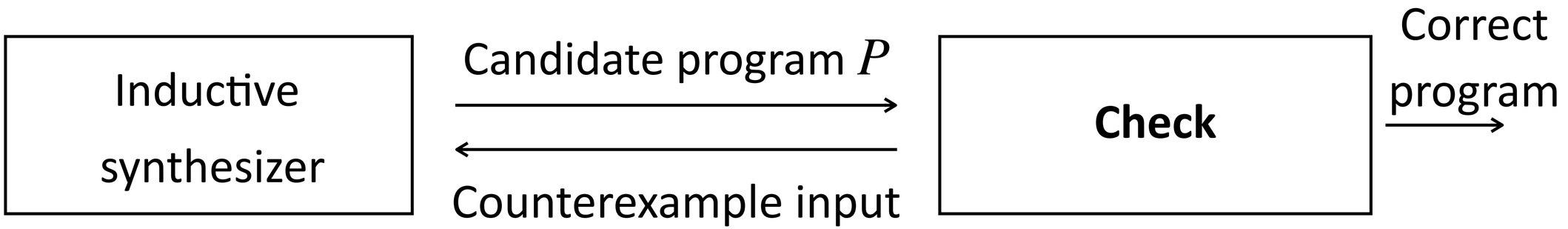
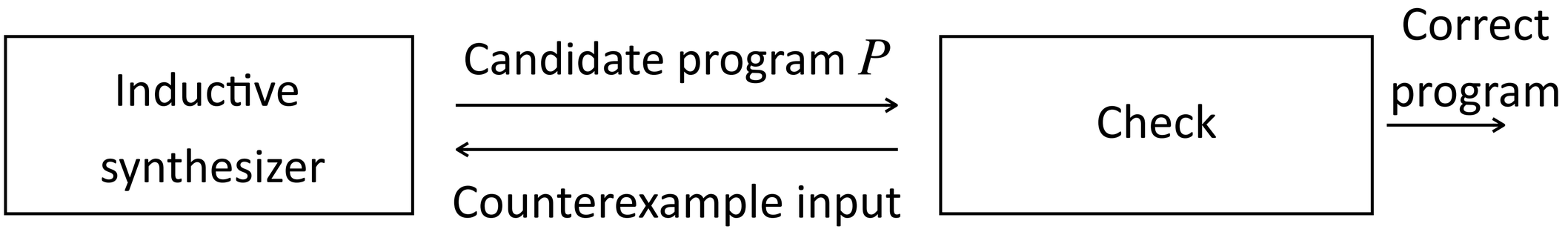


- Check whether P_n satisfies spec, if not, produce a **counterexample input**
  - Check validity: $\forall x \,.\, Q(P_n, x)$
  - If valid, P_n is solution; otherwise, P_n is wrong, produce a counterexample input x_{n+1}
    - Counterexample input: P fails but desired program should pass
    - $Q(P_n, x_{n+1}) = \bot$

Counterexample Guided Inductive Synthesis (CEGIS)

$$\exists P \,.\, \forall x \,.\, Q(P, x)$$



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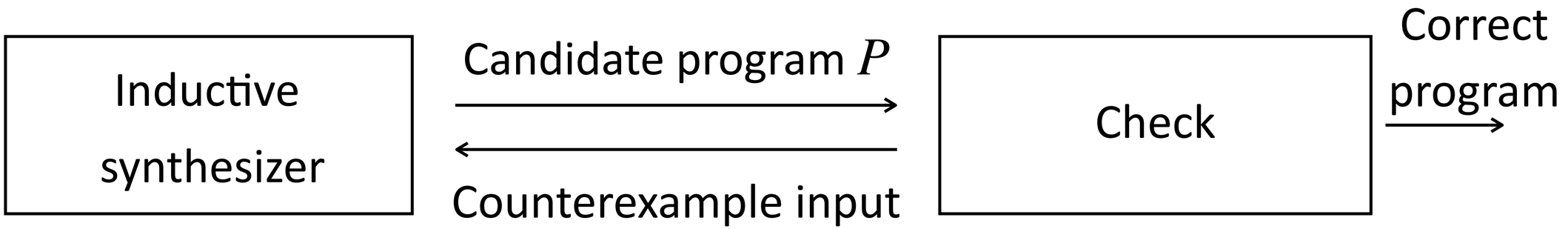

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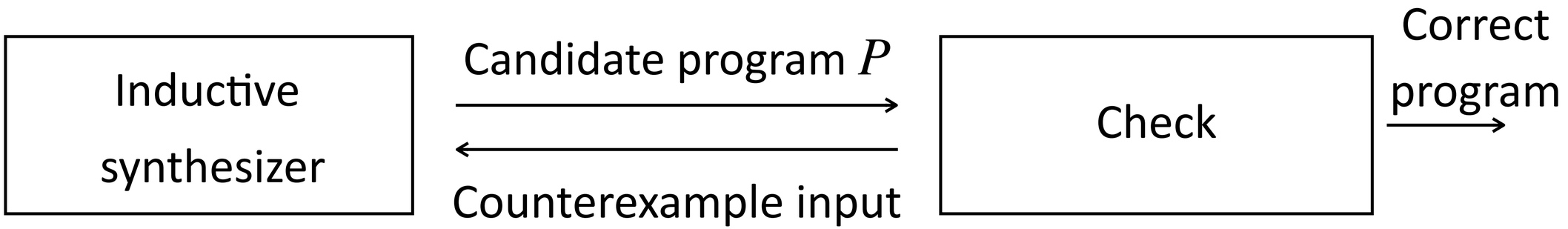

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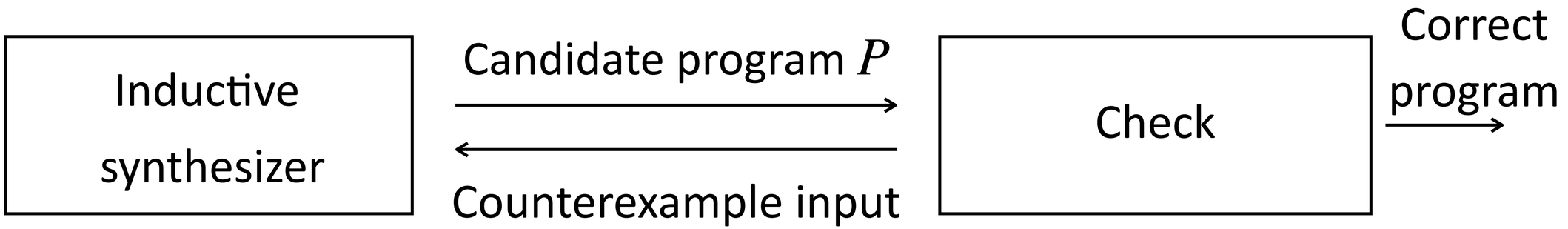

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- … or you run out of patience

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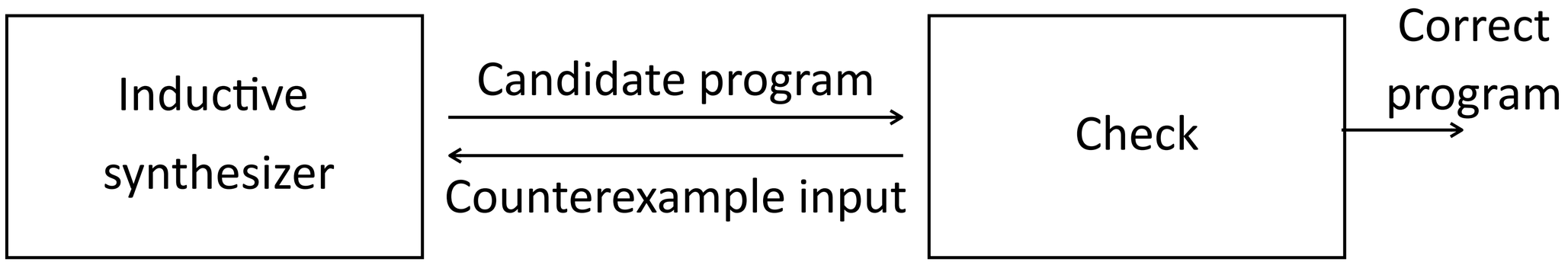

- $P(x, y)$ such that $\forall x\,.\,y\,.\;out \geq x \wedge out \geq y \wedge \left(out = x \vee out = y\right)$
- Target: $max(x, y)$

	Counterexample inputs	Candidate program
• Iteration 1	$\{\ \}$	x
• Iteration 2	$\{(1,2)\}$	y
• Iteration 3	$\{(1,2),(2,1)\}$	$max(x, y)$

CEGIS Recap

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- Use counterexamples to guide inductive synthesis
  - Avoid producing programs that fail in similar ways from previous rejected programs

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- Allow to mix and match different inductive synthesizers with different checkers
  - Inductive synthesizers: search-based, representation-based, …
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- In many problems, converge to correct program with a few iterations
- However, there are known cases where CEGIS fails badly
- If search space is unbounded, may not terminate

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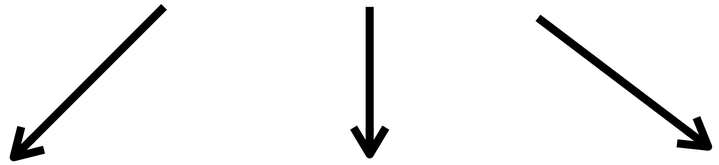

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- Think about CEGIS broadly

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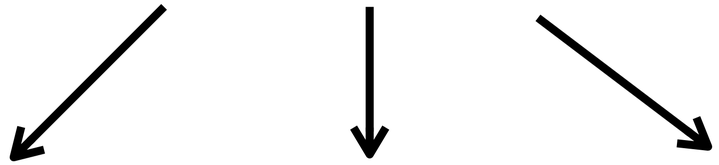

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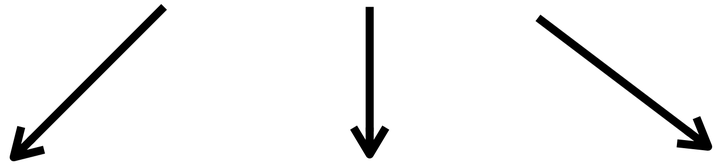

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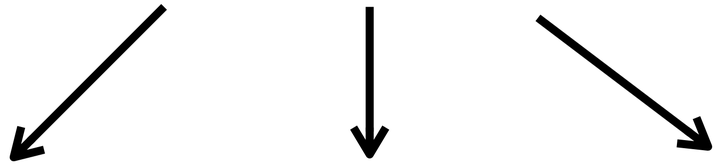

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  - Checker can be testing-based
  - Programs can be SQL queries, etc.