Circuit Design for FPGAs in Sub-threshold Ultra-low Power Systems

Master of Science Thesis Defense of Yu Huang

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Motivation

- Requirements of ubiquitous computing
  - Design cost
  - Small form-factor
  - Long-lasting
  - Energy efficient
  - Flexibility
- FPGA interconnect
  - Consumes 60%-70% power
  - Dominates delay and area
  - Further energy efficiency in an ultra-low power (ULP) system
Outline

- Motivation
- Background of FPGA
- Optimization of the energy efficient low-swing interconnect for sub-threshold (SubVt) FPGAs
- Further energy reduction of FPGA interconnect: a voltage scaling technique
- An ultra-low swing single ended level converter design
- Conclusion and contribution
Background of FPGA

- Island-style FPGA architecture
  - CLB: Configurable (complex) logic block (or LB)
  - SB: Switch box
  - CB: Connection box
Background of FPGA

- Island-style FPGA architecture
Optimization of subVt FPGA interconnect

- **Traditional options**
  - Switch point
    - Bi-directional: tri-state buffers
    - Uni-directional: Mux and buffer
  - Connection box (will be compared)
    - Full mux
    - 1-stage mux
    - 2-stage mux
Optimization of subVt FPGA interconnect

- Basic structure of low-swing interconnect
  - Switch point: Pass Gate/Transmission Gate
  - Sense amplifier: pull the signal back to nominal voltage
    - Weaken PUN
    - Sensitive for low-swing input
  - Connection box: Still mux-based
Optimization of subVt FPGA interconnect

- Global interconnect model
  - Based on MCNC benchmarks: 20 applications
  - MCNC benchmarks path distribution
    - Length: number of switches of the path
  - Observation:
    - Shorter than 40: occupy 98% of the total switch count, 94% of the total global interconnect energy few branches.
Optimization of subVt FPGA interconnect

- Global interconnect model
  - Length: 40 switch points (5 switches each)
  - No branches: worst case
  - Wire segment: pi model
  - Dual-VDD scheme: VDDC>VDD (previous work)
Optimization of subVt FPGA interconnect

- Redefine the problem
  - Dual-VDD: optimal combination?
  - Connection box
  - Driver
  - Switch point
Optimization of subVt FPGA interconnect

- Optimization: Connection box (simulation)
  - @VDD=0.4V, VDDC=0.6V.
  - Connection box
    - Full mux
    - 1-stage
    - 2-stage
  - Decision
    - 2-stage
  - Best: energy & variation
  - Overhead: area (2.6X than full mux structure)
Optimization of subVt FPGA interconnect

- Optimization: Driver, switch point (simulation)
  - @VDD=0.4V, VDDC=0.6V.
  - Driver size
    - 5X, 10X, 20X
    - Decision: 10X
  - Switch size
    - 1X, 2X, 4X, 8X
    - Decision: 4X

* Decision is made considering measurement results too.
Optimization of subVt FPGA interconnect

- **Optimization: Measurement of the chip**
  - Dual-VDD scheme
    - VDD: 0.4V
    - VDDC: 0.6V
  - Switch point
    - Size: 4X
  - Topology: PG
  - Driver
    - Size: 10X
Optimization of subVt FPGA interconnect

- Comparison
  - Optimized, un-optimized, traditional (uni-directional)
  - Vs. traditional design:
    - 97.7% smaller delay
    - 42.7% smaller energy
Optimization of subVt FPGA interconnect

- Layout photo of the 130 nm CMOS chip
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- Conclusion and contribution
Further energy reduction of interconnect: voltage scaling

- Basic idea
  - Trade: delay & energy??

https://buffy.eecs.berkeley.edu/PHP/resabs/resabs.php?f_year=2004&f_submit=chapgrp&f_chapter=10
Further energy reduction of interconnect: voltage scaling

- Programmable header structure
Further energy reduction of interconnect: voltage scaling

- Interconnect circuit models: based on MCNC benchmarks
  - Average model (AM)
  - Long net model (LM)
    - Worst case
Further energy reduction of interconnect: voltage scaling

- Voltage scaling pre-exploration using AM and LM
Further energy reduction of interconnect: voltage scaling

- Paths distribution of MCNC benchmarks compared with AM
  - Observations: similar distribution, short paths are the major part

Percentage of paths whose longest net is shorter than AM circuit in 20 MCNC benchmarks

Percentage of the paths whose switch count is less than AM circuit in 20 MCNC benchmarks
Further energy reduction of interconnect: voltage scaling

- Voltage scaling: a case study of ALU4
  - VDDH=0.8V, VDDL=0.4V
  - Applicable factor: 60%

<table>
<thead>
<tr>
<th>No voltage scaling</th>
<th>Voltage scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay distribution</td>
<td></td>
</tr>
<tr>
<td>Energy distribution</td>
<td></td>
</tr>
</tbody>
</table>

- No performance penalty
- Energy decreases by 17.3%
Further energy reduction of interconnect: voltage scaling

- Voltage scaling: a case study of ALU4
  - Applicable factor: sweeping from 0 to maximum (the max AF is 99% for ALU4)

![Graph showing energy trend of ALU4 using different voltage scaling factors]

REDUCED: 71.43%
Further energy reduction of interconnect: voltage scaling

- Voltage scaling:
  - For 7 representatives of MCNC benchmarks

![Maximum applicable factors](image1)

**Average: 98%**

![Percentage of the energy saving](image2)

**Average: 68.6%**

Maximum applicable factors

Energy reduction with maximum applicable factors
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- Conclusion and contribution
A single ended low-swing level converter design

- Lowering system threshold voltage
- Increasing energy utilization of SoCs: energy harvesting system
A single ended low-swing level converter design

- Traditional level converter
  - Switching ability: ~ 300mV – 400mV
A single ended low-swing level converter design

- Proposed design idea: using subthreshold 2X charge pump
A single ended low-swing level converter design

- Architecture of the proposed level converter

Can be any dual-input level converter design
A single ended low-swing level converter design

- Functional waveform of the proposed CPBULS (charge pump based ultra low swing) level converter
A single ended low-swing level converter design

- Simulation and measurement
  - Monte carlo simulations, iteration=100
  - CPBULS: 128mV
  - CPBLC: 171mV
  - ULS: 197mV
A single ended low-swing level converter design

- Simulation and measurement
  - Measurement results: 130nm CMOS technology
  - CPBULS: 157mV
  - CPBLC: 198mV
  - ULS: 205mV
A single ended low-swing level converter design

- Die photo
A single ended low-swing level converter design

- Conclusion and comparison
  - Compared with [6]
    - 1.5X worse energy/conversion
    - 2X higher switching capability

Table 2: Comparison between prior work and the proposed work

<table>
<thead>
<tr>
<th></th>
<th>[31]</th>
<th>[23]</th>
<th>[10]</th>
<th>[6]</th>
<th>This Work</th>
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<tbody>
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<td>188mV</td>
<td>200mV</td>
<td>400mV</td>
<td>300mV</td>
<td>145mV</td>
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<td>Energy/bit</td>
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<td>10fJ</td>
<td>327fJ</td>
<td>850fJ</td>
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<td>Area ($\mu m^2$)</td>
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* All the numbers in green squares are referenced work in the paper and thesis
Conclusion and contribution

- Optimized the subthreshold FPGA interconnect
  - Dual-VDD scheme
  - Switch box, connection box, driver
  - Signal degradation
  - Compared with the traditional design
    - 97.7% less delay
    - 42.7% less energy

- Voltage scaling technique to further reduce the energy consumption of FPGA interconnect
  - Programmable header structure
  - Explored the potentials of voltage scaling of the interconnect
    - 98% of the paths can be applied with lower driving voltage
    - 68.6% energy reduction without any performance penalty
Conclusion and contribution

- Ultra-low swing low power level converter design
  - Further extends system threshold voltage
  - Take more use of the energy in ultra-low power system: e.g. energy harvesting system
  - 145 mV switching ability from measurement results, potentially 99.6mV switching ability from simulation results
Publications

- **Yu Huang**, Aatmesh Shrivastava, Benton H. Calhoun. “A 145mV to 1.2V single ended level converter circuit for ultra-low power low voltage ICs.” In S3S Conference. **Accepted**

- He Qi, Oluseyi Ayorinde, **Yu Huang**, Benton H. Calhoun. “Optimizing energy efficient low-swing interconnect for sub-threshold FPGAs.” In Field-programmable Logic and Applications (FPL). **Accepted**

- Oluseyi Ayorinde, He Qi, **Yu Huang**, Benton H. Calhoun. “Using island-style bi-directional intra-CLB routing in low-power FPGAs.” In Field-programmable Logic and Applications (FPL). **Accepted**
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Questions?

Thank you.
Optimization of subVt FPGA interconnect

- Signal degradation
Further energy reduction of interconnect: voltage scaling

- Path information of MCNC benchmarks

<table>
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<tr>
<th>Benchmark</th>
<th>Total Switch #</th>
<th>Length of Longest Path</th>
<th>Average Switch#</th>
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Further energy reduction of interconnect: voltage scaling

- Header size exploration
  - 20X: the balance of energy, delay, area