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Thomas F. Wenisch

Curriculum Vitae – August 2012

Research Interests

High-performance computer architecture, server and data center energy efficiency, smartphone platforms, multiprocessor systems, performance evaluation methodology

Education

PhD in Electrical and Computer Engineering, Dec. 2007
Carnegie Mellon University, Pittsburgh, PA

- Dissertation title: Temporal Memory Streaming

MS in Electrical and Computer Engineering, May 2003
Carnegie Mellon University, Pittsburgh, PA

Bachelor of Science in Computer Engineering, Dec. 2000
Bachelor of Arts in German, Dec. 2000
University of Rhode Island, Kingston, RI

- Studied abroad at the Technische Universitaet Braunschweig, Germany in the Fall of 1999.

Honors and Awards

Named the **Morris Wellman Faculty Development Assistant Professor of EECS** at the University of Michigan, 7/2011

Selection of "Computational Sprinting." for **HPCA 2012 Best Paper Award.**

Selection of "BigHouse: A Simulation Infrastructure for Data Center Systems." for **ISPASS 2012 Best Paper Award**

Recognized in International Symposium of Computer Architecture **ISCA Hall of Fame**, 2011.

Selection of "MemScale: Active Low-Power Modes for Main Memory." for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2011."

Selection of "Practical Off-chip Meta-data for Temporal Memory Streaming" for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2009."

National Science Foundation **CAREER** Award, 2009-2013.
Proposal Title: Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture.

Lamme/Westinghouse Graduate Fellowship (1 yr. full Ph.D. tuition/stipend), 2004.

Intel Ph.D. Research Fellowship (1 yr. full Ph.D. tuition/stipend), 2003.

Honorable Mention, National Science Foundation Graduate Research Fellowship, 2002.

Laboratory for Computer Systems Fellowship, Carnegie Mellon University (1 yr. full Ph.D. tuition/stipend), 2001.

President's Award in Computer Engineering, University of Rhode Island, 2000.

Centennial Scholarship, University of Rhode Island, 1996-2000.

Refereed Conference Papers

F. Sleiman, R. Dreslinski, T. F. Wenisch. "Embedded Way Prediction for Large Last-Level Caches." (to appear) *Proceedings of the International Conference on Computer Design (**ICCD**)*, Oct 2012.

Q. Deng, D. Meisner, A. Bhattacharjee, T. F. Wenisch, R. Bianchini. "MultiScale: Memory System DVFS with Multiple Memory Controllers." *Proc. of the International Conference on Low Power Electronic Design (**ISLPED**)*, Aug. 2012.

D. Meisner, J. Wu, T. F. Wenisch. "BigHouse: A Simulation Infrastructure for Data Center Systems" *Proceedings of the International Symposium on Performance Analysis of Systems and Software (**ISPASS**)*, Apr. 2012 (**Best Paper Award**).

D. Meisner, T. F. Wenisch. "DreamWeaver: Architectural Support for Deep Sleep." *Proc. of the 16th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2012.

A. Raghavan, Y. Luo, A. Chandawalla, M. Papaefthymiou, K. Pipe, T. F. Wenisch, M. M. K. Martin. "Computational Sprinting." *Proc. of the 18th International Symposium on High Performance Computer Architecture (**HPCA**)*, Feb. 2012 (**Best Paper Award**).

K. Lim, Y. Turner, J Renato Santos, A. AuYoung, J. Chang, T. F. Wenisch, P. Ranganathan. "System-level Implications of Disaggregated Memory." *Proc. of the 18th International Symposium on High Performance Computer Architecture (**HPCA**)*, Feb. 2012.

A. Gutierrez, R. Dreslinski, T. F. Wenisch, T Mudge, A. Saidi, C. Emmons, N. Paver. " Full-System Analysis and Characterization of Interactive Smartphone Applications." *Proc. of the International Symposium on Workload Characterization (**IISWC**)*, Nov. 2011.

D. Meisner, T. F. Wenisch. "Does Low-power Design Imply Energy Efficiency for Data Centers?." *Proc. of the International Conference on Low Power Electronic Design (**ISLPED**)*, Aug. 2011.

D. Meisner, C. Sadler, L. Barroso, W-D. Weber, T. F. Wenisch. "Power Management of On-line Data Intensive Services." *Proc., of the 38th International Symposium on Computer Architecture (**ISCA**)*, Jun. 2011.

D. Meisner, J. Wu, T. F. Wenisch. "Stochastic Queuing Simulation: A Scalable Data Center-level Evaluation Methodology" (short paper) *Proceedings of the International Symposium on Performance Analysis of Systems and Software (**ISPASS**)*, Apr. 2011.

Q. Deng, D. Meisner, L. Ramos, T. F. Wenisch, R.Bianchini. "MemScale: Active Low-Power Modes for Main Memory." *Proc. of the 16th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2011 (**IEEE Micro Top Picks**).

D. Meisner and T. F. Wenisch. "Peak Power Modeling for Data Center Servers with Switched-Mode Power Supplies." *Proc. of the International Conference on Low Power Electronic Design (**ISLPED**)*, Aug. 2010.

S. Pelley, D. Meisner, P. Zandevakili, T. F. Wenisch, and J. Underwood. "Power Routing: Dynamic Power Provisioning in the Data Center." *Proc. of the 15th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2010.

C. Blundell, M. M. K. Martin, T. F. Wenisch. "InvisiFence: Performance-Transparent Memory Ordering in Conventional Multiprocessors." *Proc., of the 36th International Symposium on Computer Architecture (**ISCA**)*, Jun. 2009.

K. Lim, J. Chang, T. Mudge, P. Ranganathan, S. K. Reinhardt, T. F. Wenisch. "Disaggregated Memory for Expansion and Sharing in Blade Servers." *Proc., of the 36th International Symposium on Computer Architecture (**ISCA**)*, Jun. 2009.

S. Somogyi, T. F. Wenisch, A. Ailamaki, and B. Falsafi. "Spatio-Temporal Memory Streaming." *Proc. 36th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2009.

D. Meisner, B. T. Gold, and T. F. Wenisch. "PowerNap: Eliminating Server Idle Power." *Proc. of the 14th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2009.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi and A. Moshovos. "Practical Off-chip Meta-data for Temporal Memory Streaming." *Proc. of the 15th International Syposium on High-Performance Computer Architecture (**HPCA**)*, Feb. 2009 (**IEEE Micro Top Picks**).

M. Ferdman, T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Temporal Instruction Fetch Streaming." *Proc. of the 41st Annual International Syposium on Microarchitecture (**MICRO**)*, Dec. 2008.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi and A. Moshovos. "Temporal Streams in Commercial Server Applications." *Proc. of the IEEE International Syposium on Workload Characterization (**IISWC**)*, 2008.

T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Mechanisms for Store-wait–free Multiprocessors." *Proc. of the 34th International Symposium on Computer Architecture (**ISCA**)*, Jun. 2007.

S. Somogyi, T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Spatial Memory Streaming." *Proc., of the 33rd International Symposium on Computer Architecture (**ISCA**)*, Jun. 2006.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi and J. C. Hoe. "Simulation Sampling with Live-Points." *Proceedings of the International Symposium on Performance Analysis of Systems and Software (**ISPASS**)*, Mar. 2006.

T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki, and B. Falsafi. "Store-Ordered Streaming of Shared Memory." *Proc. of the 14th International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, Sep. 2005.

T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, A. Ailamaki, and B. Falsafi. "Temporal Streaming of Shared Memory." *Proc. of the 32nd International Symposium on Computer Architecture (**ISCA**)*, Jun. 2005.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, and J. C. Hoe. "TurboSMARTS: Accurate Microarchitecture Simulation Sampling in Minutes." (Short paper) *Proc. of the International Conference on Measurement and Modeling of Computer Systems (**SIGMETRICS**),* Jun. 2005.

R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "SMARTS: Accelerating Microarchitecture Simulation via Rigorous Statistical Sampling." *Proc. of the 30th International Symposium on Computer Architecture (**ISCA**)*, Jun. 2003.

T. F. Wenisch, P. F. Swaszek and A. K. Uht. "Combined Error Correcting and Compressing Codes." *Proc. of the International Symposium on Information Theory (**ISIT**)*, Jun. 2001.

Journal Articles

K. Sewell, R. G. Dreslinski, T. Manville, S. Satpathy, N. Pinckney, G. Blake, M. Cieslak, R. Das, T. F. Wenisch, D. Sylvester, D. Blaauw, and T. Mudge. "2D and 3D Swizzle-Switch Network Design" *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (**JETCAS**),* June 2012

Q. Deng, D. Meisner, L. Ramos, T. F. Wenisch, R.Bianchini. "Active Low-Power Modes for Main Memory with MemScale." ***IEEE MICRO** Special Issue on **Top Picks** in Computer Architecture 2011,* vol. 32 no. 3, May/Jun. 2012 (to appear).

D. Meisner, B. T. Gold, and T. F. Wenisch. "The PowerNap Server Architecture." *ACM Transactions on Computer Systems (**TOCS**)*. Vol. 29, No. 1, Feb. 2011.

S. Somogyi, T. F. Wenisch, M. Ferdman, B. Falsafi. "Spatial Memory Streaming." *Journal of Instruction-Level Parallelism (**JILP**),* 13 (2011) 1-26.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi, and A Moshovos. "Making Address Correlated Prefetching Practical." ***IEEE MICRO** Special Issue on **Top Picks** in Computer Architecture 2009,* vol. 30 no. 1, Jan./Feb. 2010.

T. F. Wenisch, R. E. Wunderlich, M. Ferdman, A. Ailamaki, B. Falsafi, and J. C. Hoe. "SimFlex: Statistical Sampling of Computer System Simulation." ***IEEE MICRO** Special Issue on Computer Architecture Simulation and Modeling,* vol. 26, no. 4, Jul./Aug. 2006.

R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "Statistical Sampling of Microarchitecture Simulation." *ACM Transactions on Modeling of Computer Systems (**TOMACS**),* vol. 16, no. 3, Jul. 2006.

N. Hardavellas, S. Somogyi, T. F. Wenisch, R. E. Wunderlich, S. Chen, J. Kim, B. Falsafi, J. C. Hoe, A. Nowatzyk. "SimFlex: A Fast, Accurate, Flexible Full-System Simulation Framework for Performance Evaluation of Server Architecture." *ACM SIGMETRICS Performance Evaluation Review (PER)*, Vol. 31, No. 4, Mar. 2004.

A. K. Uht, D. Morano, A. Khalafi, M. de Alba, T. F. Wenisch, M. Ashouei and D. Kaeli. "Levo: IPC in the 10's via Resource Flow Computing." *IEEE Technical Committee on Computer Architecture Newsletter*, Special Issue: Oct. 2001.

Workshop Papers

P. Tandon, J. Chang, R. Dreslinski, P. Ranganathan, T. Mudge, T. F. Wenisch. "PicoServer Revisited: On the Profitability of Eliminating Intermediate Cache Levels." *Proc. of the Workshop on Duplicating, Deconstructing, and Debunking (WDDD),* Jun. 2012.

S. Pelley, T. F. Wenisch, K. LeFevre, " Do Query Optimizers Need to be SSD-aware?" *Proc. of the Second International Workshop on Accelerating Data Management Systems using Modern Processor and Storage Architectures (ADMS),* Jun. 2011.

R. Sampson, T. F. Wenisch, "ZCache Skew-ered." *Proc. of the 9th Workshop on Duplicating, Deconstructing, and Debunking (WDDD),* Jun. 2011.

D. Meisner, T. F. Wenisch, "Stochastic Queuing Simulation for Data Center Workloads." *Proc. of the Exascale Evaluation and Research Techniques Workshop,* Mar. 2010.

S. Pelley, D. Meisner, T. F. Wenisch, J. VanGilder. "Understanding and Abstracting Total Data Center Power." *Proc. of the Workshop on Energy Efficient Design (WEED),* Jun. 2009.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, and J. C. Hoe. "Statistical Sampling of Microarchitecture Simulation." *Proc. of the 2006 Workshop on the NSF Next Generation Software Program (NGS),* Apr. 2006.

S. Somogyi, T. F. Wenisch, N. Hardavellas, J. Kim, A. Ailamaki, and B. Falsafi. "Memory Coherence Activity Prediction in Commercial Workloads." *Proc. of the 3rd Workshop on Memory Performance Issues (WMPI)*, Jun. 2004.

R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "An Evaluation of Stratified Sampling of Microarchitecture Simulations." *Proc. of the 3rd Workshop on Duplicating, Debunking, and Deconstructing (WDDD),* Jun. 2004.

Technical Reports

Computing Community Consortium. "21st Century Computer Architecture." A community white paper. http://cra.org/ccc/docs/init/21stcenturyarchitecturewhitepaper.pdf, Mar. 2012.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. C. Hoe, "TurboSmarts: Accurate Microarchitecture Simulation Sampling in Minutes," Technical Report 2004-3, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Nov. 2004.

T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki, and B. Falsafi. "SORDS: Just-In-Time Streaming of Temporally-Correlated Shared Data," Technical Report 2004-2, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Nov. 2004.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. C. Hoe, "Applying SMARTS to SPEC CPU2000," Technical Report 2003-1, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Jun. 2003.

Patents

F. Sleiman, R.G. Dreslinski, and T. F. Wenisch. "A Data Processing Apparatus Having a Cache Configured to Perfom Tag Lookup and Data Access in Parallel, and a Method of Operating the Data Processing Apparatus". US Patent Pend., Filed 11/22/11.

A. Raghavan, M. Papaefthymiou, K. Pipe, T.F. Wenisch, M.M.K. Martin. "Computational Sprinting Using Multiple Cores." US Patent Pend., Filed 11/18/11.

D. Roberts, T. Mudge, and T. F. Wenisch. "Memory Control". US Patent Pend., Filed 10/16/2009.

D. Meisner, T. F. Wenisch. "Computer Energy Conservation with a Scalable PSU Configuration". US Patent Pend., Filed 12/16/2008.

T. F. Wenisch, S. R. Berard, D. J. Smith. "Computer Network Security System". US Patent No. 7,100,054. Issued 8/29/2006.

T. F. Wenisch. "Software-based Watchdog Method and Apparatus." US Patent No. 7,162,714. Issued 1/9/2007.

C. Kuiawa, D. Cardimino, T. Giaquinto, T. F. Wenisch. "Uninterruptible Power Supply Management Network System". US Patent Pend., Appl. No. 20030033548. Filed 8/9/2001.

Presentations

"Power Management from Smartphones to Data Centers." Facebook, July 2012.

"Power Management from Smartphones to Data Centers." Oracle, July 2012.

"Efficiency Challenges in Warehouse-Scale Computers." UIUC, Mar. 2012.

"Efficiency Challenges in Warehouse-Scale Computers." Washington U., Mar. 2, 2012.

"Efficiency Challenges in Warehouse-Scale Computers." U. Edinburgh, Mar. 2012.

"Efficiency Challenges in Warehouse-Scale Computers." Wayne State U., Jan. 2012.

"Power Management of On-line Data Intensive Services." (**Invited Plenary Talk**) Dasan Conference, Korean Federation of Science and Technology Society, Nov. 2011.

"Power Management of On-line Data Intensive Services." POSTECH, Korea, Nov. 2011.

"Making Enterprise Computing Green." Princeton University, Oct. 2011.

"Making Enterprise Computing Green." Yahoo!, Jul. 2011.

"Architectures and Evaluation Methods for On-line Data Intensive Services Running on Warehouse Scale Computers." NSF Workshop on Sustainable Energy-Efficient Data Management, May 2011.

"Server/data center energy efficiency challenges." ASPLOS PC Symposium, Oct. 2010.

"Making Enterprise Computing Green." IBM Austin Research Lab, Aug. 2010.

"Making Enterprise Computing Green." Microsoft Research, Feb. 2010.

"Making Enterprise Computing Green." U. Washington, Feb. 2010.

"Making Enterprise Computing Green." Wayne State University, Oct. 2009.

"Thinking Outside the Box: Power Management at the System Level & Beyond." (**Invited Plenary Talk**) Int'l Symp. on Low Power Electronic Design (ISLPED), Aug. 2009.

"Making Enterprise Computing Green." Yahoo! HKN Seminar Series, Mar. 2009.

"Making Enterprise Computing Green." Merit Member Conference, Jun. 2009.

"Making Enterprise Computing Green." Tutorial at the International Conference on High-Performance Computing (HiPC), Dec. 2008.

"Improving Memory System Performance and Eliminating Idle-power Waste in Commercial Servers." Intel Research Bangalore, Dec. 2008.

"Hiding Memory Latency in Commercial Server Application." Indian Inst. of Sci., Dec. 2008.

"Mechanisms for Store-Wait-Free Multiprocessors." ARM, Nov. 2008.

"Making Enterprise Computing Green: Energy-efficiency Challenges in Enterprise Data Centers." Carnegie Mellon University, Oct. 2008.

"Hiding Memory Latency in Commercial Server Application." IBM TJ Watson, Jul. 2008.

"Mechanisms for Store-Wait-Free Multiprocessors." 34th International Symposium on Computer Architecture (ISCA), Jun. 2007.

"Temporal Memory Streaming." University of Toronto, University of Michigan, MIT, Columbia University, UT-Austin, Microsoft Research-Silicon Valley, Microsoft Research-Redmond, HP Labs in Feb.-Apr. 2007.

"Improving the Simulation and Programmability of Future Multiprocessor Systems." Brown University, Jan 2007.

"SimFlex: Simulation Sampling Theory and Practice." University of Pittsburgh, Feb. 2006.

"Store-Ordered Streaming of Shared Memory." 14th International Conference on Parallel Architectures and Compilation Techniques (PACT), Sep. 2005.

"Temporal Streaming of Shared Memory." 32nd International Symposium on Computer Architecture (ISCA), Jun. 2005.

"TurboSMARTS: Accelerating Microarchitecture Simulation Sampling in Minutes." Princeton, Sep. 2004.

"Breaking the Memory Wall." Intel, Santa Clara, CA, Oct. 2003.

"SMARTS: Accelerating Microarchitecture Simulation via Rigorous Statistical Sampling." 30th International Symposium on Computer Architecture (ISCA), Jun. 2003.

"Combined Error Correcting and Compressing Codes" International Symposium on Information Theory (ISIT), Jun. 2001.

Press Coverage

"'Sprinting' chips could push phones to the speed limit," *New Scientist* #2852, 2/20/12.

"Could 'Computational Sprinting' Speed Up Smart Phones without Burning Them Out?," *Scientific American*, 2/29/12.

"Researchers Propose 'Computational Sprinting' To Speed Up Chips By 1000% – But Only For A Second," *TechCrunch*, 2/28/12.

"Researchers propose 'overclock' scheme for mobiles; Processing at a sprint to overcome tech limitations," *The Register*, 2/21/12.

"Study explores computing bursts for smartphones," *PhysOrg.com*, 2/21/12.

"Green Data Centers." WEMU 89.1 FM **Radio Interview.** 7/27/2011.

"PowerNap plan could save 75 percent of data center energy." *U-M News Service*, 3/5/09.

"'Napping' data centers could cut energy use by 75 percent." *ZDNet Asia*, 3/6/09.

"Optimizing The Sleep Cycle." *Processor.com*, 6/5/09.

"Merit Member Conference Covers Cool Learning Technology." *WWJ Radio*, 6/11/09.

Grants

CCF/SHF: Medium: Collaborative Research: Ultra-Responsive Architectures for Mobile Platforms (NSF; CCF-1161505; $900,000; M. Martin (U. Penn), T. Wenisch, M. Papaefthymiou, K. Pipe; 2012-2016)

RunDMC: Durable Memory Consistency (Oracle; $150,000; 2012)

A Data-Centric Approach to Energy Proportionality (Google; $1,500,000; R. Bianchini (Rutgers), S. Gurumurthi (U. Virginia), F. Chong (UCSB), T. Wenisch; $375,000 to Wenisch; 2010-2012)

Re-architecting Memory and Processors for Energy Efficiency (Google; $100,000; T. Wenisch-PI, T. Mudge–Co-PI, D. Blaauw–Co-PI, D. Sylvester–Co-PI, 2010)

Toward Energy-Proportional Web Search Clusters (Google; $65,000; 2010)

CAREER: Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture (NSF; CCF-0845157; T. Wenisch–PI; $400,000; 2009-2013)

Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture (Intel; $120,000; 2009-2011)

CSR-DMSS,SM: Beyond Solid State Disks: Using FLASH to save energy in Enterprise Systems (NSF; CSR-0834403; T. Wenisch–PI, T. Mudge–Co-PI; $280,000; 2008-2011)

CPA-CSA: Virtualization Mechanisms for Zero-Idle-Power and Thermally-Efficient Data Centers (NSF; CCF-0811320; T. Wenisch–PI; $275,000; 2008-2011)

Disaggregated Memory for Energy-Efficient Data Centers (HP Labs; T. Mudge–PI, T. Wenisch–Co-PI; $145,000; 2008-2009)

FloVent License Grant (Flomerics; $9,600; 2008-2009)

Equipment Donation (Intel; $30,000; 2008)

Professional Activities

Program Committee Chair, IEEE International Symposium on Workload Characterization (IISWC), 2012.

Co-Chair, HotPower 2012.

Guest Editor, IEEE Micro Special Issue on Power (planned for Sep-Oct. 2012).

Panelist: "Collaborative Tools and Reproducibility of Research Experiments in Exascale Computer Systems." EXADAPT Workshop held with ASPLOS (2012).

Program Track Co-Chair, Architecture for the Networking, Architecture & Storage Conference (NAS) 2011.

Invited Delegate to NSF Workshop on Sustainable Energy Efficient Data Management (SEEDM), May 2011.

Co-organizer of the Exascale Evaluation and Research Techniques (EXERT) Workshop held in conjunction with ASPLOS 2010, 2011.

Co-organizer of the Annual Workshop on Modeling, Benchmarking, and Simulation (MoBS), held in conjunction with ISCA 2009, 2010, 2011.

Tutorial presentation: T. F. Wenisch. "Making Enterprise Computing Green". Held in conjunction with HiPC 2008 (Bangalore, India).

Tutorial presentation: T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. Hoe. "SimFlex: Fast, Accurate and Flexible Simulation of Computer Systems". Held in conjunction with: 38th Annual International Symposium on Microarchitecture (MICRO), Nov. 2005 33rd International Symposium on Computer Architecture (ISCA), Jun. 2006.

Panelist: "Cycle-Accurate Simulators: Knowing When to Say When." held with ISCA (2008).

Principal developer of the Flexus full-system multiprocessor computer architecture simulation framework, publicly available at http://www.ece.cmu.edu/~simflex.

Principal developer of the TurboSmartsim simulation sampling & checkpointing extensions to SimpleScalar, publicly available at http://www.ece.cmu.edu/~simflex.

Workshops Chair for PACT (2012).

Workshops & Tutorials chair for IISWC (2010).

Publications chair for PACT (2010).

Publications chair for MICRO (2009).

Finance chair for PACT (2008).

National Science Foundation Panelist 2009, 2010, 2011, 2012.

Technical Program Committee Member for ISCA (2013), HPCA (2013), ASPLOS (2011, 2013), SIGMETRICS (2013), ISPLED (2010,2011,2012), IGCC (2012), ICPP (2010, 2012), HiPEAC (2011, 2012), ISPASS (2009, 2010, 2012), HotPower (2009, 2011, 2012), WEED (2009, 2010, 2011, 2012), MICRO (2011), ICS (2009, 2011), PACT (2009, 2010), HotMetrics (2010), eEnergy (2010), DATE (2008, 2009), WISH (2009), IEEE MICRO Top Picks (2009), TRANSACT (2008), MOBS (2008), CMP-MSI (2008).

Member of the ACM and IEEE.

Employment History

7/2011 - University of Michigan Ann Arbor, MI

Morris Wellman Faculty Development Assistant Professor of EECS

9/2007 – 6/2011 University of Michigan Ann Arbor, MI

Assistant Professor, Computer Science & Engineering

9/2006 AuthenTec Melbourne, FL

Security Consultant

- Provided independent review of a proposed biometric authentication system architecture.

9/2000 – 9/2006 American Power Conversion West Kingston, RI

Software Developer

- Developed network management software for uninterruptible power supplies.
- Designed novel security mechanisms for web-based user interfaces (US patent 7,100,054).

2/2000 – 8/2000 Siemens AG Munich, Germany

Test Engineer (intern)

- Created test hardware and software for subscriber line modules for ISDN switching systems.
- Developed a PC expansion card and accompanying device drivers for controlling custom measurement hardware.

Teaching

EECS 370 – Computer Organization (Fall 2009)
EECS 470 – Computer Architecture (Fall 2007, Winter 2009, Winter 2010, Fall 2011)
EECS 570 – Parallel Computer Architecture (Winter 2011, Winter 2012)
EECS 598 – Enterprise Systems (Winter 2008)