A New Design of an n-bit Reversible Arithmetic Logic Unit

Subhankar Pal, Chetan Vudadha, Sai Phaneendra P., V. Sreehari, M. B. Srinivas
Birla Institute of Technology and Science - Pilani, Hyderabad Campus

Introduction

This poster introduces the design of a cost-optimized reversible ALU using a mix of the well-known NCV library and the NCV-$|v_1\rangle$ library, with the assumption of a four-level quantum system. First, a cost-optimized reversible adder is presented, which is used to design the proposed ALU.
Quantum gates are the building blocks of reversible circuits. The basic quantum gates constituting the NCV library are shown in Fig. 1.

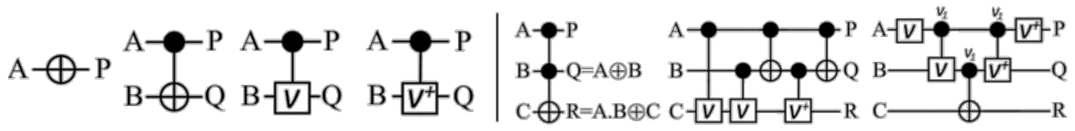

Figure 1 : NOT, CNOT, CV and CV$^+$ (NCV) — Toffoli gate (NCV and NCV-$|v_1\rangle$)

NOT is the complement operation ($\mathbf{0} \rightarrow \mathbf{1} \rightarrow \mathbf{0}$), V is the cyclic operation ($\mathbf{0} \rightarrow v_0 \rightarrow \mathbf{1} \rightarrow v_1$), and V$^+$ is the inverse cyclic operation. The controlled gates are only activated when the control line is set to 1.

The NCV-$|v_1\rangle$ Quantum Gate Library

The library used in this work, introduced in [1], uses *qudits* instead of *qubits*, i.e. a basic building block which relies on a *four*-level quantum system instead of a two-level quantum system. Any state of this qudit may be written as:
$|\Psi\rangle = c_0|0\rangle + c_1|v_0\rangle + c_2|1\rangle + c_3|v_1\rangle \qquad (|c_0|^2 + |c_1|^2 + |c_2|^2 + |c_3|^2 = 1)$
So, the assumption in this model is that v_0 and v_1 are not states in superposition, as in the NCV library, but basic states, in the new library. The new library consists of three unitary gates (NOT, V and V$^+$) and their single-controlled versions. These gates transform the target qudit according to:

$$\text{NOT} = \begin{pmatrix} 0&0&1&0 \\ 0&0&0&1 \\ 1&0&0&0 \\ 0&1&0&0 \end{pmatrix},\ \text{V} = \begin{pmatrix} 0&0&0&1 \\ 1&0&0&0 \\ 0&1&0&0 \\ 0&0&1&0 \end{pmatrix} \text{ and } \text{V}^+ = \begin{pmatrix} 0&1&0&0 \\ 0&0&1&0 \\ 0&0&0&1 \\ 1&0&0&0 \end{pmatrix}$$

Unlike the NCV library, the controlled gates in the NCV-$|v_1\rangle$ library perform the respective operations when the control line is set to v_1, not when it is 1.
Fig. 1 shows the NCV and NCV-$|v_1\rangle$ quantum equivalents of a Toffoli gate.
Two important assumptions for the mixed-library designs in this work are:

- NCV states in superposition, $|v_0\rangle$ and $|v_1\rangle$, can be treated as basis states for the NCV-$|v_1\rangle$ library gates.
- All quantum gates have equal cost, independent of the library they belong.

The terms *bit* and *qudit* are used interchangeably in this poster.

n-Bit Reversible Ripple-Carry Adder

The adder shown in Fig. 2 is obtained by modifying the basic design of [2], with references from the ADD$_5$ circuit and SUM$_5$ gate in Sec. 2.2 and 3.2 of [2].

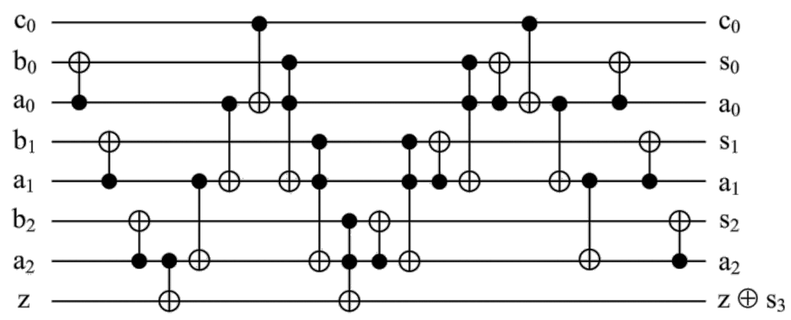

Figure 2 : The proposed 3-bit ripple-carry adder circuit.

This circuit is expanded using a combination of the NCV and NCV-$|v_1\rangle$ libraries. The CNOT gates used here are NCV gates. The bottom-most Toffoli gate is merged with the adjacent CNOT gate to form an NCV Peres gate. All the other Toffoli gates are expanded using the NCV-$|v_1\rangle$ model of Fig. 1. The quantum equivalent circuit of the adder is shown in Fig. 3. c_0 is the carry-in bit, a_i and b_i are the inputs, and s_3 is the carry-out bit (z=0).

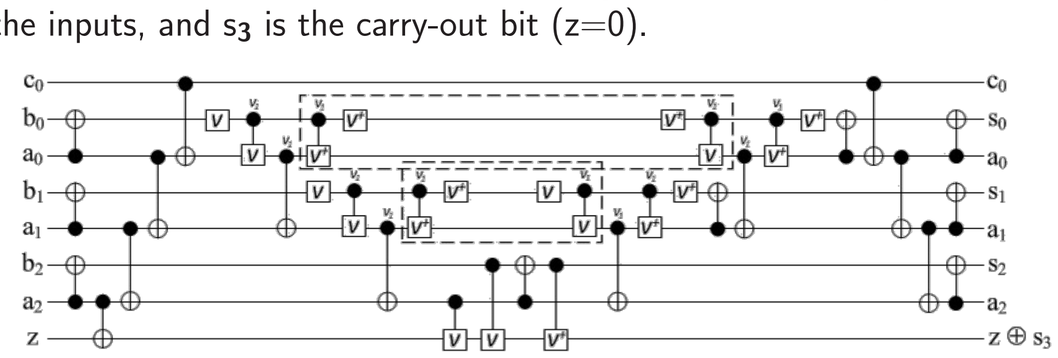

Figure 3 : Quantum equivalent circuit of proposed adder design.

The V and V$^+$ gates enclosed within boxes in Fig. 3 can be removed since they form *identity* gates.
The quantum cost and delay of the circuit are **31** and **25** respectively. For an n-bit version, the cost and delay turn out as $\mathbf{11n - 2}$ and $\mathbf{8n + 1}$ respectively.
Table 1 compares the no. of ancillary inputs, no. of garbage outputs, cost and delays of a few reversible ripple-carry adder designs.

n-Bit Reversible Arithmetic Logic Unit

The 3-bit ALU in Fig. 4 is constructed using the previous adder. CNOT gates are used as XORs to negate the lines wherever necessary, and Fredkin gates are used as MUXes. Five control signals, w_i ($i = 0, \ldots 4$), define the opcodes for the ALU (see Table 2). The resultant qudits are designated r_i for $i = 0, 1, 2$. CNOT gates are also used to fan-out w_0 and w_1 to create 3 copies for the 3-bit ALU (fan-out gates not shown in Fig. 4).

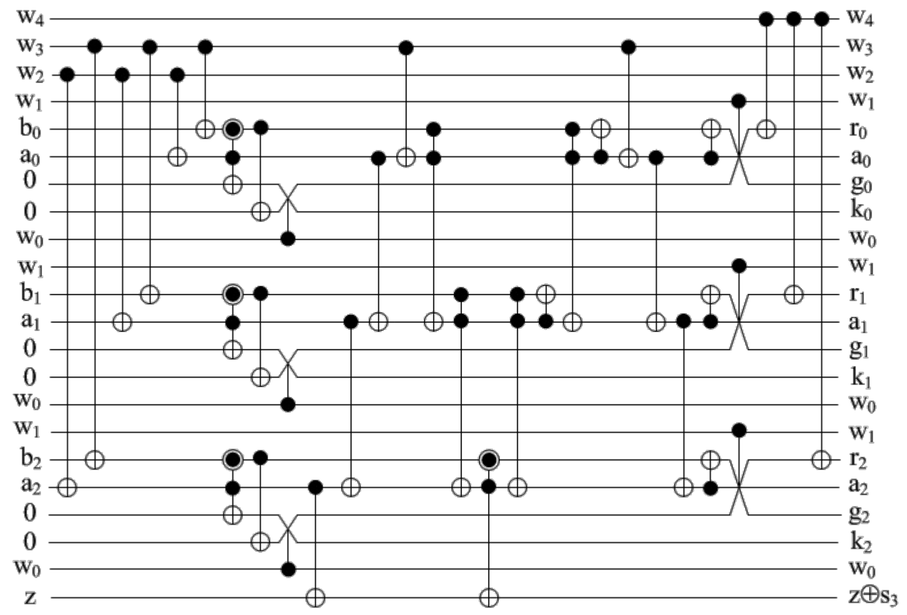

Figure 4 : Proposed design of 3-bit ALU circuit.

The circuit of Fig. 4 is expanded such that only the Toffoli gates are replaced with their NCV-$|v_1\rangle$ versions. Other gates are expanded using the NCV library. Redundant V and V$^+$ gates that evaluate to identities are removed, as discussed in the previous section. The quantum equivalent circuit is not shown here.

Design	AIs	GOs	QC	Delay Δ
[3]	0	n+1	17n-6	10n+2
[3]	0	n+1	17n-22	10n-8
[4]	0	n	15n-6	9n+5
Proposed	0	n	11n-2	8n+1

Table 1 : A comparison of ripple-carry adders with input carry.
(AI: Ancilla Input; GO: Garbage Output; QC: Quantum Cost)

w_0	w_1	w_2	w_3	w_4	RESULT
×	0	0	0	0	ADD
×	0	0	1	0	SUB
1	1	0	0	0	A ⊕ B
1	1	0	0	1	A ⊙ B
0	1	1	1	1	A + B
0	1	1	1	0	(A + B)'
0	1	0	0	0	A . B
0	1	0	0	1	(A . B)'

Table 2 : Opcodes and corresponding operations for the proposed ALU.

The quantum cost and delay of the proposed 3-bit ALU are calculated to be 86 and 42 respectively. By extrapolating the design for n-bits, the cost can be calculated to be $\mathbf{30n - 4}$ and the delay to be $\mathbf{10n + 12}$.
The proposed n-bit ALU uses $\mathbf{4n - 2}$ ancilla including those required to duplicate the signals w_0 and w_1. The ALU in Fig. 6.3 of [5] employs $\mathbf{6n}$ ancilla qubits to duplicate the 6 select signals (excluding the select signal for SLT), plus $\mathbf{2n}$ additional ancilla. The proposed ALU produces $\mathbf{5n + 3}$ garbage outputs, as compared to at least $\mathbf{8n}$ in [5]. For n=32, it has a quantum cost of **956** and a worst-case delay of **332**. There is a cost reduction of **39.0%** as compared to the design in [5] having a cost of **1568**. However, the proposed circuit is almost 3 times slower than the 32-bit ALU in [5], which has a delay of **108**.

Conclusions

This paper explored the possibility of using a combination of gates from the NCV and the NCV-$|v_1\rangle$ libraries. This can lead to circuits with lower quantum costs, whenever Toffoli gates are in series. This is also applicable for multiple-control Toffoli gates in series, as elaborated in [1]. However, in some cases, such as a Toffoli gate and a CNOT gate in series, it is more cost-effective to combine them into an NCV Peres gate rather than to use the NCV-$|v_1\rangle$ equivalents (as has been done for the adder design of Fig. 3).

References

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Presenter: Subhankar Pal LinkedIn Profile: http://tinyurl.com/linkedin-spal E-Mail: spal0993@gmail.com