A New Design of an n-bit Reversible Arithmetic Logic Unit

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***Abstract*—With the advent of nanotechnology, transistors are getting smaller and growing in number according to Moore's Law. With this, the issue of heat dissipation is becoming of greater concern to researchers as the transistor heat dissipation reaches the Landauer limit. Reversible logic is predicted to be an alternative to conventional computing due to lesser energy dissipation and exponentially faster problem-solving capacity. This paper introduces the design of a reversible ripple-carry adder using a mix of the well-known NCV library and the recently introduced NCV-$|v_1\rangle$ library, with the assumption of a four-level quantum system. The results for the proposed adder are compared with previous ripple-carry adder designs. It then explores the design of a cost-optimized reversible ALU by modifying the above adder. Finally, a comparison of the proposed ALU is made with one of the latest reversible ALU designs.**

***Keywords*—Reversible Logic; Quantum Gates; Adder; ALU;**

I. Introduction

Reversible computing is predicted to offer the only potential way to improve the energy efficiency of computers by surpassing the von Neumann-Landauer "kT barrier" .

Quantum gates are the building blocks of reversible circuits. The basic quantum gates are shown in Fig. 1.

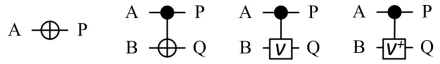

Fig. 1. Basic quantum gates in the *NCV* library: NOT, CNOT, CV and CV$^+$.

These gates constitute the NCV library. The controlled gates are activated when the control line is set to 1, otherwise the inputs appear as outputs. The gates transform the target qubit as: *NOT* $= \left(\begin{smallmatrix} 0 & 1 \\ 1 & 0 \end{smallmatrix}\right)$, $V = \frac{1+i}{2}\left(\begin{smallmatrix} 1 & -i \\ -i & 1 \end{smallmatrix}\right)$ and $V^+ = \frac{1-i}{2}\left(\begin{smallmatrix} 1 & i \\ i & 1 \end{smallmatrix}\right)$.

Circuits using the NCV library involve qubits restricted to one of $\{0, v_0, 1, v_1\}$, where $v_0 = \frac{1}{2}\left(\begin{smallmatrix} 1+i \\ 1-i \end{smallmatrix}\right)$ and $v_1 = \frac{1}{2}\left(\begin{smallmatrix} 1-i \\ 1+i \end{smallmatrix}\right)$.

Note that *NOT* is the complement operation ($0 \rightarrow 1 \rightarrow 0$), V is the cyclic operation ($0 \rightarrow v_0 \rightarrow 1 \rightarrow v_1$), and V^+ is the inverse cyclic operation.

II. The NCV-$|v_1\rangle$ Quantum Gate Library

The library used in this work, introduced in [1], is called the NCV-$|v_1\rangle$ library. Here, *qudits* instead of *qubits* are assumed, i.e. a basic building block which does not rely on a two-level quantum system, but a *four*-level quantum system. Any state of this qudit may be written as $|\Psi\rangle = c_0|0\rangle + c_1|v_0\rangle + c_2|1\rangle + c_3|v_1\rangle$ (c_i satisfy $|c_0|^2 + |c_1|^2 + |c_2|^2 + |c_3|^2 = 1$). So, the assumption in this model is that v_0 and v_1 are not states in superposition, as in the NCV library, but basic states, in the new library.

The new library consists of the three unitary gates performing the *NOT*, V and V^+ operations, and their single-controlled versions. These gates transform the target qudit according to: *NOT* $= \left(\begin{smallmatrix} 0&0&1&0 \\ 0&0&0&1 \\ 1&0&0&0 \\ 0&1&0&0 \end{smallmatrix}\right)$, $V = \left(\begin{smallmatrix} 0&0&0&1 \\ 1&0&0&0 \\ 0&1&0&0 \\ 0&0&1&0 \end{smallmatrix}\right)$ and $V^+ = \left(\begin{smallmatrix} 0&1&0&0 \\ 0&0&1&0 \\ 0&0&0&1 \\ 1&0&0&0 \end{smallmatrix}\right)$

However, these controlled gates perform the respective operations not when the control line is 1, but when it is v_1.

Fig. 2 shows the NCV and NCV-$|v_1\rangle$ quantum equivalents of a single-control Toffoli gate.

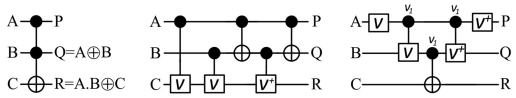

Fig. 2. The Toffoli gate and its NCV and NCV-$|v_1\rangle$ equivalent circuits.

An important assumption followed in the rest of the paper is that the NCV states in superposition, $|v_0\rangle$ and $|v_1\rangle$, can be treated as basis states for the NCV-$|v_1\rangle$ gates. It is also assumed that all quantum gates, independent of the library they belong to, have equal cost. Considering our mixed design approach, we will be using *qudits* instead of *qubits* further on.

III. n-Bit Reversible Ripple-Carry Adder

A. The Proposed Design

In a ripple-carry adder, the sum bits s_i are computed as:

$$s_i = \begin{cases} a_i \oplus b_i \oplus c_i & \text{if } 0 \leq i \leq n-1, \\ c_i & \text{if } i = n. \end{cases}$$

Defining MAJ as the majority function for three bits (refer Sec. 2.1 in [2]), the carry bit c_i is defined as:

$$c_i = \begin{cases} 0 & \text{if } i = 0, \\ \textit{MAJ}(a_{i-1}, b_{i-1}, c_{i-1}) & \text{if } 1 \leq i \leq n. \end{cases}$$

As in [2], MAJ and UMA gates are connected together to form a basic ripple carry adder. The proposed adder shown in Fig. 3 is obtained by modifying the basic design, analogous to the ADD_5 circuit and SUM_5 gate in Sec. 2.2 and 3.2 of [2].

B. Quantum Equivalent Circuit

This section expands the circuit of Fig. 3 using a combination of the NCV and NCV-$|v_1\rangle$ libraries.

The CNOT gates in the circuit are NCV gates. The bottommost Toffoli gate in Fig. 3 is merged with the adjacent CNOT

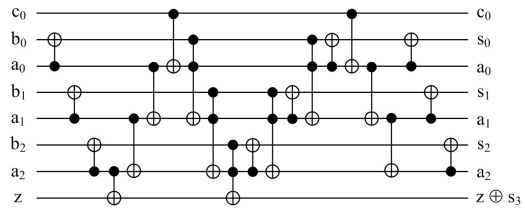

Fig. 3. The proposed 3-bit ripple-carry adder circuit.

gate to form an NCV *Peres* gate. However, all the other Toffoli gates are expanded using the NCV-$|v_1\rangle$ model (see Fig. 2). Fig. 4 shows the quantum equivalent circuit of the proposed adder.

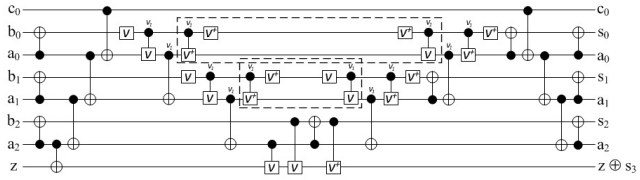

Fig. 4. Quantum equivalent circuit of proposed design.

A V and a V^+ (unitary/controlled) gates in series form an *identity*, rendering them redundant. Hence, the"boxed" gates in Fig. 4 are as good as non-existent.

C. Results and Comparison - Quantum Cost and Delay

From Fig. 4, one can calculate the cost and delay of the proposed adder to be 31 and 25 respectively. By extrapolating the design, for an *n*-bit version, the cost and delay turn out as $11n - 2$ and $8n + 1$ respectively.

Table I compares the no. of ancillary inputs, no. of garbage outputs, cost and delays of a few reversible ripple-carry adders.

TABLE I
A COMPARISON OF RIPPLE-CARRY ADDERS WITH INPUT CARRY.

Design	AIs	GOs	QC	Delay Δ
[3]	0	$n+1$	$17n-6$	$10n+2$
[3]	0	$n+1$	$17n-22$	$10n-8$
[4]	0	n	$15n-6$	$9n+5$
Proposed	0	n	$11n-2$	$8n+1$

IV. n-BIT REVERSIBLE ALU

A. The Proposed Design

The 3-bit ALU in Fig. 5 is constructed using the adder of Fig. 3. CNOT gates are used as XORs to negate the inputs/outputs wherever necessary, and Fredkin gates are used as MUXes. Five control signals, w_i (*i* = 0, 1, 2, 3, 4), define the *opcodes* for the ALU (see Table II). The resultant qudits are designated r_i for *i* = 0, 1, 2. CNOT gates are also used to fan-out the signals w_0 and w_1 (not shown in figure).

In Fig. 5, only the Toffoli gates are replaced with their NCV-$|v_1\rangle$ versions. Other gates are expanded using the NCV library. Redundant gates are removed, as discussed in Sec. III-B.

B. Results and Comparison - Quantum Cost and Delay

The total cost and delay of the proposed 3-bit ALU are calculated as 86 and 42 respectively. For an n-bit ALU, the cost is found to be $30n - 4$ and the delay to be $10n + 12$.

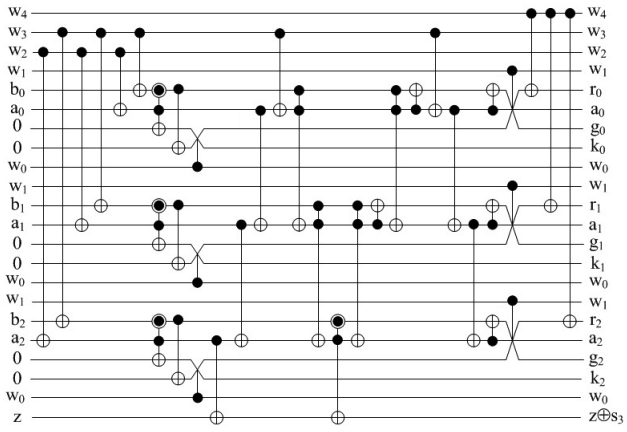

Fig. 5. Proposed design of 3-bit ALU circuit.

TABLE II
OPCODES AND CORRESPONDING OPERATIONS FOR THE PROPOSED ALU.

w_0	w_1	w_2	w_3	w_4	RESULT
×	0	0	0	0	*ADD*
×	0	0	1	0	*SUB*
1	1	0	0	0	$A \oplus B$
1	1	0	0	1	$A \odot B$
0	1	1	1	1	$A + B$
0	1	1	1	0	$(A + B)'$
0	1	0	0	0	$A.B$
0	1	0	0	1	$(A.B)'$

The proposed n-bit ALU uses $4n-2$ ancilla including those required to duplicate the signals w_0 and w_1. The ALU in Fig. 6.3 of [5] employs $6n$ ancilla qubits to duplicate the six select signals (excluding the select signal for SLT), plus $2n$ additional ancilla. The proposed ALU produces $5n + 3$ garbage outputs, as compared to at least $8n$ in [5]. For $n = 32$, it has a quantum cost of 956 and a worst-case delay of 332. There is a cost reduction of 39.0% as compared to the design in [5] having a cost of 1568. However, the proposed circuit is almost 3 times slower than the 32-bit ALU in [5], which has a delay of 108.

V. CONCLUSIONS

This paper explored the possibility of reducing quantum cost using a combination of NCV and NCV-$|v_1\rangle$ libraries, whenever Toffoli gates are in series. This is also applicable for multiple-control Toffoli gates in series. However, in some cases, such as a Toffoli and a CNOT in series, it is better to combine them into an NCV Peres gate rather than to use the NCV-$|v_1\rangle$ gates.

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