Subhankar Pal | Curriculum Vitae

2260 Hayward Avenue, Ann Arbor, MI 48109

subh@umich.edu • web.eecs.umich.edu/~subh

Graduate student in Computer Science and Engineering, currently in the third year of PhD. Research interests include hardware-software co-design for specialized applications, microarchitecture and emerging technologies.

Education

- **University of Michigan** — **Ann Arbor, MI, USA**
  Doctor of Philosophy in Computer Science and Engineering — *2018–2021 (expected)*
  Research area: *'Reconfigurable Software-Defined Hardware Architectures'*
  Advisor: *Prof. Ronald G. Dreslinski, Jr.*

- **University of Michigan** — **Ann Arbor, MI, USA**
  Master of Science in Computer Science and Engineering — *2016–2018*
  CGPA: 4.0/4.0
  Relevant coursework: Computer Architecture (EECS 470), Microarchitecture (EECS 573), Data-Centric Systems (EECS 598), Parallel Computer Architecture (EECS 570), Special Topics in Computer Architecture (EECS 670), Operating Systems (EECS 482), Advanced Compilers (EECS 583), Machine Learning (EECS 545)

- **Birla Institute of Technology and Science – Pilani** — **Hyderabad, TS, India**
  Bachelor of Engineering in Electrical and Electronics Engineering, graduated with Distinction — *2010–2014*
  CGPA: 9.6/10.0
  Relevant coursework: Digital Electronics and Computer Organization, Microprocessor Programming and Interfacing, Machine Learning, Image Processing, Analog and Digital VLSI Design

Research Experience

- **University of Michigan** — **Ann Arbor, MI, USA**
  Graduate Student Research Assistant, CADRe Group — *September 2016–Present*
  I am currently leading the DARPA Software-Defined Hardware (SDH) program efforts for Michigan, which involves building a flexible, reconfigurable architecture for a multitude of applications in linear algebra, graph/signal processing, etc. I am also a part of the Domain-Specific System-on-Chip (DSSoC) program, which uses the same architecture as one of its IP blocks and is targeted towards wireless and other communication applications. Prior to this, I was the primary architect of `OuterSPACE` [HPCA '18], a novel sparse matrix multiplication accelerator, which formed the foundation of our SDH/DSSoC proposals. I also led the frontend development effort and testing of a scaled-down version of this chip in 40 nm. In addition, I have been involved in a characterization study to evaluate how software has evolved to harness the parallelism offered by contemporary hardware, targeting traditional and emerging desktop applications.

- **University of Bremen** — **Bremen, HB, Germany**
  Research Assistant, Institut für Theoretische Elektrotechnik und Mikroelektronik (ITEM) — *May 2013–July 2013*
  I was involved in a project titled "Coding and Characterization of Low-Power Encoders & Decoders for Very Deep Sub-Micron Buses". I conducted literature survey and implemented various bus encoding and decoding techniques in hardware using Verilog. I validated them functionally and analyzed their power, area, latency using Synopsys DC & Cadence Analog Design Environment, revealing a trade-off between these parameters. My results would allow a designer to select the best bus coding technique depending on the choice of their compromise.

- **Bhabha Atomic Research Centre** — **Mumbai, MH, India**
  Research Intern, Division of Remote Handling and Robotics — *May 2012–July 2012*
  I worked towards developing a drive mechanism for a piezoelectric transducer based dispenser used for the manufacture of bio-chips. My first task was to program a C167CR microcontroller to generate pulses meeting the specs of the dispenser. I further developed a GUI to generate and control the pulse through the UART interface. Lastly, I designed and implemented a circuit to amplify and feed the pulse to the transducer.

Industry Experience

- **IBM Corporation** — **Yorktown Heights, NY, USA**
  Research Intern, Software Architecture — *May 2019–August 2019*
  Currently working with Dr. Viji Srinivasan on a runtime system for a custom DNN accelerator.

- **Advanced Micro Devices, Inc.** — **Boxborough, MA, USA**
  Co-Op Engineer, Architecture Research — *May 2017–September 2017*
  I worked with Dr. Kalamatianos as a part of AMD's exascale computing group, on improving the performance and energy efficiency of the Instruction Fetch pipeline front-end for next-generation AMD cores. My initial task was to understand the CPU simulation infrastructure and embed code to do fine-grained profiling of the Branch Target Buffer (BTB) access patterns for a variety of workloads. I also performed upper-bound studies and literature survey to develop a two-point solution for performance/power enhancement. The first targeted at reducing BTB misses and enhanced the overall micro-instructions per cycle. The next solution reduced the power consumed by the BTB structure by reducing number of lookups. We have a patent pending based on this work.

- **NVIDIA Corporation** — **Bangalore, KA, India**
  ASIC Design Verification Engineer — *July 2014–July 2016*
  I worked on pre-silicon verification of GPUs that involved running full-chip tests and debugging issues in the domain of PCI-Express, clocks and resets, and enhancement and maintenance of full-chip testbench covering these features. I also worked actively on the bring-up of Maxwell and Pascal line of GPUs, focusing on testing and validation of new features. Further, I collaborated with the post-silicon validation team to redesign a post-silicon utility widely used internally for debug of issues during the post-silicon validation and bring-up phases. I was also responsible for automating the GPU power measurement and analysis flow by implementing a wrapper around their existing infrastructure.

- **NVIDIA Corporation** — **Bangalore, KA, India**
  ASIC Engineering Intern — *January 2014–June 2014*
  I developed two GUI-based tools to assist post-silicon debug of GPUs. I also used a PCI Express logic analyzer to help in debugging PCIe issues encountered with the chips, and enhanced post-silicon debug tools that assisted in quicker and more convenient debug.

Teaching Experience

- **University of Michigan** — **Ann Arbor, MI, USA**
  Graduate Student Instructor — *January 2018–April 2018*
  I was the Graduate Student Instructor (GSI) with Prof. Satish Narayanasamy for EECS 570, which is an advanced graduate-level course in Computer Architecture. I was responsible for teaching a discussion section, answering student questions online and in-person, tutoring students on parallel programming paradigms, designing exam questions and grading exams/assignments/projects.

Conference Publications

- **S. Pal**, D.-h. Park, S. Feng, P. Gao, J. Tan, A. Rovinski, S. Xie, C. Zhao, A. Amarnath, T. Wesley, J. Beaumont, K.-Y. Chen, C. Chakrabarti, M. Taylor, T. Mudge, D. Blaauw, H.-S. Kim and R. Dreslinski, "A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator Using Memory Reconfiguration in 40 nm", 2019 Symposia on VLSI Technology and Circuits (VLSI), Kyoto, 2019, *to appear*.
- S. Feng, **S. Pal**, Y. Yang, R. Dreslinski, "Parallelism Analysis of Prominent Desktop Applications - An 18-year Perspective", 2019 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Madison, 2019, pp. 202-211.
- **S. Pal**, J. Beaumont, D. H. Park, A. Amarnath, S. Feng, C. Chakrabarti, H. S. Kim, D. Blaauw, T. Mudge, R. Dreslinski, "OuterSPACE: An Outer Product based Sparse Matrix Multiplication Accelerator", 2018 IEEE International Symposium on High-Performance Computer Architecture (HPCA), Vienna, 2018, pp. 724-736.
- A. Amarnath, S. Feng, **S. Pal**, T. Ajayi, A. Rovinski and R. Dreslinski, "A Carbon Nanotube Transistor based RISC-V Processor using Pass Transistor Logic", 2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), Taipei, 2017, pp. 1-6.
- **S. Pal**, C. K. Vudadha, P. S. Phaneendra, S. Veeramachaneni and S. Mandalika, "A New Design of an N-Bit Reversible Arithmetic Logic Unit," 2014 Fifth International Symposium on Electronic System Design, Surathkal, 2014, pp. 224-225

Patents

- Kalamatianos, J., Yalavarti, A., Agrawal, V., **Pal, S.**, Srinivasan, V., "Filtered Branch Prediction Structures of a Processor", filed August 22, 2018.

Notable Projects

- *'Development of Components of a Basic Operating System'*

  This comprised of four projects spanning a month each. The components independently developed, using C++, were – a multi-threaded disk scheduler, a thread management library, a virtual memory manager and a networked file system.

- *'Compiler Support for a High-Bandwidth, Fixed-Throughput Regular Expression Accelerator'*

  Our group worked on adding support for processing nested Kleene operators (*/+/x) in HARE [MICRO '16], a hardware accelerator for matching regular expressions against large in-memory logs. HARE scans input data at a fixed rate and provides a constant throughput, but does not support all types of queries, since some regular expressions require backtracking or serialization to be able to identify strings. Our proposed extension to HARE, improved the coverage of regular expressions supported by HARE, while keeping the changes in throughput and area minimal.

- *'Formal Verification of the MSI Cache Coherence Protocol'*

  This was an individual project to implement and formally verify the MSI cache coherence protocol using Murphi. I primarily implemented spontaneous self-downgrading, which involved the processor spontaneously choosing to downgrade from Modified to Shared. The second optimization was cruise-missile invalidation, which caused the Home to send invalidation to one sharer, which would forward it to the next, and so on. The implementation was validated to be bug-free for upto 4 processors.

- *'Design and Implementation of a 2-Way Out-of-Order Superscalar Processor'*

  As part of a group, I implemented a MIPS R10K-style, 2-way superscalar, out-of-order processor based on the Alpha ISA using SystemVerilog. The overall features of the system were: 2-way with 2 ALU functional units and 2 fully-pipelined, 2-stage multiplier units, store-to-load forwarding in a load-store queue, loads issue non-speculatively past pending stores, multiple outstanding load misses, N-way set-associative, multi-ported, write-back data cach, fully-associative victim cache, branch history table with bimodal branch predictors and next N-line prefetching in the instruction cache.

- *'Bacterial Colony Detection for Testing Antibiotic Sensitivity'*

  The project involved writing a MATLAB codebase for the detection of different types of bacterial colonies which grow in an agar culture from their images. As high magnification was required, a macro lens was procured from an old DVD drive and mounted on a standard camera phone. Statistical image processing techniques were employed to match pixels of the colored colonies in the images with a database of colors obtained from fresh cultures of several types of bacterial colonies.

Technical and Personal skills

- **Programming Languages/Tools:** C, C++, Verilog, Python, Tk, Perl, Shell, gem5, LLVM, MATLAB
- **Operating Systems:** Linux, Windows, MacOS
- **CAD/EDA Tools:** Verdi, Design Compiler, Virtuoso, Analog Design Environment, MultiSim, LabVIEW, PSpice, Keil μVision, AutoDesk 123D, AutoCAD
- **Version Control Tools:** Git, Perforce, Subversion

Awards and Honors

- **Rackham Travel Grant** (2019): Financial award for presenting at VLSI Symposium in Kyoto, Japan.
- **U-M Financial Aid** (2016–present): Full tuition waiver with benefits working as Graduate Student Research Assistant with Prof. Dreslinski
- **Top Contributor** (2015): Honored by NVIDIA for excellent performance as an employee for 2014-2015
- **Merit-Cum-Need Scholarship** (2014): Issued by BITS-Pilani for merit and financial need
- **DAAD-WISE Scholarship** (2013): Selected among 163 students from India by the German Academic Exchange Service (DAAD) for a funded internship in Germany during the summer of 2013

- **"Best Student" Scholarship** (2012): Awarded by the Angiras foundation, TX for merit and financial need
- **Certificate of Merit** (2010): Issued by CBSE for outstanding performance in Computer Science in All India Senior School Certificate Examination

Mentorship

- Mentored undergraduate students as part of Michigan's *Lunch and Lab* Mentorship Program from Sep-Nov 2018
- Worked closely with and mentored a Senior undergraduate student, mainly for the SDH program, over a period of three academic terms
- Mentored an intern in the ASIC Verification team while working full-time at NVIDIA, for a period of 4 months