Reetuparna Das

3624 BBB Building, 2260 Hayward Street, Ann Arbor, 48109.
email: reetudas@umich.edu phone: 814-404-6677
http://web.eecs.umich.edu/∼reetudas

Research Interests

I am interested in all aspects of computer architecture and systems. My specialized interests include In-Memory computing for big data applications, custom system stack for precision medicine and AI, energy efficient and mobile architectures, on-chip interconnection networks, 3D integration, and impact of future technologies on computer architecture.

Professional Experience

- **University of Michigan**, Ann Arbor, MI — Sep 2020 - Present
  Associate Professor
- **University of Michigan**, Ann Arbor, MI — Jan 2016 - Aug 2020
  Assistant Professor
- **University of Michigan**, Ann Arbor, MI — Aug 2011 - Dec 2015
  Assistant Research Scientist
- **Center for Future Architectures Research**, Ann Arbor, MI — Jan 2014 - Dec 2015
  Researcher in Residence
- **Microsoft Research**, Redmond, WA — June 2013 - Aug 2013
  Visting Researcher; Manager: Doug Burger
- **Intel Labs**, Santa Clara, CA — June 2010 - July 2011
  Research Scientist
- **Pennsylvania State University**, University Park, PA — Aug 2005 - May 2010
  PhD Candidate; Advisor: Chita Das
- **Microsoft Research**, Redmond, WA — May-Aug 2008
  Research Intern; Manager: Onur Mutlu
- **Intel Corporation**, Hillsboro, OR — May-Aug 2007, 2006
  Research Intern; Managers: Donald Newell, Jaideep Moses
- **STMicroelectronics Ltd**, Delhi, India — June 2004 - June 2005
  Firmware Engineer for Nomadic, ST's multimedia system-on-chip processor
- **Tata Institute of Fundamental Research**, Mumbai, India — May-Aug 2003
  Visiting Students Research Program; Advisor: N. Raja

Education

- **Pennsylvania State University**, University Park, PA May 2010
  Ph.D. in Computer Science and Engineering
  Dissertation title: Application-Aware On-Chip Networks
- **National Institute of Technology**, Rourkela, India June 2004
  B.Tech. in Computer Science and Engineering

Awards

- **Intel Outstanding Researcher Award, 2020.**
  Intel Labs sponsors and works alongside leading researchers around the globe in such areas as quantum computing, artificial intelligence (AI), and other emerging innovative technologies. Annually, Intel recognizes the exceptional contributions being made from Intel university-sponsored research with the Outstanding Researcher Award. Award recipients must have demonstrated a high-level of innovation at enabling the understanding or solving of major technology roadblocks.
- **Sloan Research Fellowship, 2019.**
  The Alfred P. Sloan Foundation awards Sloan Research Fellowships to about 126 scientists annually. These early-career scholars represent the most promising scientific researchers working today. Their achievements and potential place them among the next generation of scientific leaders in the U.S. and Canada.
- **IEEE Micro's Top Picks Award, 2019.**
  Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks.
  Top picks "collects some of this year's most significant research papers in computer architecture based on novelty and long-term impact."
- **CRA-W Borg Early Career Award, 2018.**
  This annual award is given to a woman in computer science and/or engineering who has made significant research contributions and who has contributed to her profession, especially in the outreach to women. Borg Early Career Award honors the late Anita Borg, who was an early member of CRA-W.
- **ISCA Hall of Fame Award, 2018.**
  An honor given to outstanding researchers with eight or more papers at the ACM/IEEE International Symposium on Computer Architecture (ISCA). ISCA is the flagship conference for computer architecture.
- **MICRO Hall of Fame Award, 2017.**
  An honor given to outstanding researchers with eight or more papers at the ACM/IEEE International Symposium on Microarchitectures (MICRO). MICRO is the flagship conference for microarchitecture.
- **NSF CAREER Award, 2017.**
  "In-Situ Compute Memories for Accelerating Data Parallel Applications".
  The CAREER grant is one of the National Science Foundation's most prestigious awards, conferred for "the early career-development activities of those teacher-scholars who most effectively integrate research and education within the context of the mission of their organization."
- **Student Award: Charles Eckert, NDSEG, 2019.**
  National Defense Science and Engineering Graduate Fellowship.
- **Student Award: Arun Subramanian, Precision Health Scholars Awards, 2018.**
  University wide fellowship provided as part of UM's Precision Health initiative.
- **Student Award: Arun Subramanian, Rackham International Students Fellowship, 2017.**
  A college of engineering wide fellowship that recognizes outstanding international pre-candidate doctoral stu-

dents who have demonstrate outstanding academic and professional promise.

- **Student Award: Shaizeen Aga, Michigan CSE Graduate Students Honors Competition, 2016.**
  "Compute Caches"
  Yearly competition which "recognizes research of broad interest and exceptional quality done by graduate students."
- **Best Demo Award, C-FAR Annual Review, 2016**
  "Compute Caches"
  The best demo award was based on popular vote from industry sponsors and faculty PIs. Award was based on novelty, significance and real demonstration of proposed technology.
- **IEEE Micro's Top Picks Award, 2011.**
  "Aérgia: Exploiting Packet Latency Slack in On-Chip Networks".
  Top picks "collects some of this year's most significant research papers in computer architecture based on novelty and long-term impact."
- **Outstanding Research Assistant Award**, CSE Dept., Pennsylvania State University, 2008
- **Outstanding Teaching Assistant Award**, CSE Dept., Pennsylvania State University, 2006
- **College of Engineering Fellowship**, Pennsylvania State University, 2005-2006.
- **Meritorious Girls Scholarship, NIT Rourkela, 2000-2004.**
  Awarded for outstanding performance in Engineering Entrance Examination. The scholarship covered expenses for four years of undergraduate education.
- **Byomkesh Memorial Award, NIT Rourkela, 2001.**
  Awarded for being ranked first among 300+ students among all disciplines of college of engineering in the freshman year.
- **Visiting Students Research Scholarship (VSRP), Tata Institute of Fundamental Research (TIFR), Mumbai, 2003.**
  VSRP scholarship is offered annually to about ten undergraduate students in India.

Grants

- COVID-19: Rapid: Pathogen Detection with Real-Time Genetic, PI, $200,000, 2020-22
- National Science Foundation (NSF), SHF: Small: Acceleration Using Smart Memory-on-Chip, PI, $450,000, 2019-22
- Alfred Sloan Foundation, Sloan Fellowship, $70,000, PI, 2019-21.
- SRC/JUMP, "Applications Driving Architectures (ADA) Center," PI $896,000, 2019-22.
- Precision Health Scholars Award , "Hardware Accelerated Systems for NGS Analysis," 2018-19, $80,000, Co-PI.
- National Science Foundation (NSF), Compute Caches: Opportunistic Parallelism in General Purpose Processors at Extreme Scale, PI, $300,000, 2018-19

- Intel Corporation, Gift award for work on Compute Caches, PI, $308,000, 2017-25
- National Science Foundation (NSF), CAREER: In-Situ Compute Memories for Accelerating Data Parallel Applications, PI, $573,554, 2017-22
- Semiconductor Research Corporation (SRC), Towards Disintegration with Interposers: Design of Flexible Interconnect IPs for System-In-Package Architectures, PI, $318,000, 2017-20
- Center for Future Architectures Research (C-FAR), PI, $316,675, 2016-2017
- National Science Foundation (NSF), CCF, SHF: Small: Scaling the Compute Efficiency of General-Purpose Processors, co-PI, $450,000, 2012-15
- Huawei Corporation, Future Interconnects for Embedded SoCs, co-PI, $230,000, 2014-15
- National Science Foundation (NSF), CCF, Eager: Scaling On-Chip Interconnects for Exascale Systems, PI, $90,000, 2012-13

Teaching Experience

- **Instructor**, University of Michigan 2013, 2016, 2017, 2018, 2019, 2020
  Introduction to Computer Organization, EECS 370
  The EECS 370 course is designed to teach undergraduate students fundamentals of computer architecture and organization. It is a required course for both CMPSC and CMPENG majors. The class has more than 650 registered students this fall (2018) and it is considered one of the largest and most challenging undergraduate courses in the Computer Science and Engineering program. The course is particularly challenging because it covers a broad range of new concepts at a fairly deep level along with four different projects spread throughout the semester. As a fulltime instructor my responsibilities included delivering weekly lectures, managing the course assignments, mentoring students for course projects and administering the course grades. The course covered basics of microprocessors (control, datapath and I/O processing), and assembly language programming.
- **Instructor**, University of Michigan 2019, 2020
  EECS 498, Applied Parallel Programming with GPUs
  The class teaches applied parallel programming concepts, with special focus on massively parallel programming processors (GPUs). The goal of this class is to teach parallel computing and developing applications for massively parallel processors (e.g. GPUs). Self-driving cars, machine learning, and augmented reality are examples of applications involving parallel computing. The class focuses on computational thinking, forms of parallelism, programming models, mapping computations to parallel hardware, efficient data structures, paradigms for efficient parallel algorithms, and application case studies. The course will cover popular programming interface for graphics processors (CUDA for NVIDIA processors), internal architecture of graphics processors and how it impacts performance, and implementations of parallel algorithms on graphics processors. The class has heavy programming components, including six hands-on assignments and a final project.
- **Instructor**, University of Michigan Fall 2016
  Data Centric Systems, EECS 598
  This special topics course covered recent advances and new directions that are being pursued to design data-centric computing systems.

- **Instructor**, University of Michigan Fall 2017
  Special topics in Computer Architecture, EECS 670
  This special topics course covered advanced topics in computer architecture such as in-memory computing, specialized architectures for machine learning, IoT, accelerators, warehouse scale computing and emerging technologies.

- **Instructor**, Beihang University, China Summer 2012
  Seminars on Advanced Parallel Computer Architecture: Network-on-Chip, 111 Project Course Series
  This was a 12 hour special topics course on advanced concepts in Network-on-Chip architectures. The course had 70+ registered students from multiple universities and research institutes in Beijing.

- **Instructor**, Pennsylvania State University Spring 2009
  Introduction to Computer Organization, CMPEN 331
  The CMPEN 331 course in Pennsylvania State University is equivalent of EECS 370 course at University of Michigan.

- **Teaching Assistant**, Pennsylvania State University Spring 2007, Spring 2006, Fall 2005
  Introduction to Computer Architecture, CMPEN 431
  As a teaching assistant my responsibilities included, setting up simulators for course projects, grading assignments and exams, helping students with course assignments, taking few lectures on behalf of instructor and weekly office hours.

- **Teaching Assistant**, Pennsylvania State University Fall 2006
  Introduction to C++ Programming, CMPSC 101
  As a teaching assistant my responsibilities included, managing three instructional labs a week, grading exams, helping students with course assignments and weekly office hours.

Current Doctoral Students

- **Arun Subramaniyan** Aug 2016-present
- **Daichi Fuijiki** Aug 2016-present
- **Vidushi Goyal** Aug 2016-present
  Co-advised with Valeria Bertacco
- **Charlie Eckert** Aug 2017-present
- **Xiaowei Wang** Aug 2017-present
- **Yufeng Gu** Aug 2020-present
- **Owen Hoffend** Aug 2020-present

Graduated Doctoral Students

- **Andrew Lukefahr** Aug 2011- Aug 2016
  Co-advised with Scott Mahlke
  First Employment: Assistant Professor, Indiana University

- **Shruti Padmanabha** Aug 2011- Dec 2016
  Co-advised with Scott Mahlke
  First Employment: Software Engineer, Facebook

Professional Service

- HPCA Test of Time award selection committee chair, 2021.
- MICRO Test of Time award selection committee chair, 2020, 2021.
- Program co-chair for MICRO, 2019.
- HPCA Test of Time award selection committee, 2019.
- MICRO Test of Time award selection committee, 2018.
- TACO Associate Editor, 2020-2021.
- SIGARCH Computer Architecture Today, Blogger 2017-18.
- Program Committee Track Chair for DAC'17, DAC'18, DAC'19.
- Program Committee member for Micro Top Picks 2018, 2019, 2021
- Program Committee member for ISCA'21, ISCA'20, ISCA'19, ISCA'18, ISCA'17, ASPLOS'18, MICRO'18, MICRO'15, HPCA'18, HPCA'17, HPCA'16.
- Program Committee member for DATE'18, PACT'18, IPDPS'17, SC'16, ICS'16, SC'15, ICCD'15, MICRO-ERC'14, IPDPS'14, IISWC'14, NOCS'14, NOCS'13, MICRO-ERC'12, NOCS'12, ICCD'12, ICCD'11, IISWC'12.
- SIGARCH YouTube! Officer 2017-18.
- Publication chair for ISCA 2018 and PACT 2017.
- NSF Panels 2012, 2013, 2015, 2016, 2017, 2018
- NIH Review Panel 2020
- Webchair for 16th International Conference on High-Performance Computer Architecture (HPCA-16).

Outreach

- Engaging high-school female students in computing.
  We co-organized the Girls Encoded in 2016. Over 100 high school girls and their parents attended this event. The goal was to introduce high-school girls to the exciting world of computer science and engineering. The

day consisted of hands-on activities, a panel discussion, and lab tours to show students the different aspects of CSE. I hosted an activity which taught the girls how to build an electric circuit on a pizza board with a few paper clips, LEDs, resistors and a battery.

Recently I was a speaker and participant at an Ada Lovelace opera organized for high-school girls and families. The evening event began with eight TED-style lightning talks by female faculty and students at UM who are engaged in cutting-edge computing research. The talks were followed by an opera on Ada Lovelace's establishment as the research partner of inventor Charles Babbage in the 1840s.

- Teacher at CS Kickstart.
  At Michigan we organize a week-long introductory course for incoming freshmen women students who are interested in computer science or engineering. This course is inspired by Berkeleys CS Kick Start initiative. We hope to teach freshmen female students, What is Computer Science?, and introduce them to CS curriculum, programming, CS professors, and research. I taught a computer architecture lab at CS Kickstart organized in Fall 2017 and Fall 2018. We disassembled a computer and learned about how a computer ultimately runs binary instructions to process complex software applications.

- WiCArch Organizing Committee.
  WiCArch is an organization which brings together women researchers in the sub-discipline of computer architecture. I serve on WiCArch's organizing committee. Our goal is to create a nurturing environment for women researchers, improve their visibility and build a strong support system.

- Speaker and participant at Career Workshop for Women and Minorities at MICRO-50, 2017.

- Participant for Debugging the Gender Gap panel co-organized with LeanIn@Michigan team.

- Faculty adviser for Girls in Electrical Engineering and Computer Science (gEECS) at the University of Michigan.

Invited Talks

- *Systems for Precision Health*
  Keynote, ISPASS, 2021
- *Compute Cache for Data Parallel Acceleration*
  UCR ECE Distinguished Colloquium, 2020
- *Compute Cache for Data Parallel Acceleration*
  NoCArch Keynote, 2019
- *Blurring the Lines between Memory and Compute*
  Google Accelerated Compute Research Summit, 2018
- *Blurring the Lines between Memory and Compute*
  Microsoft Research, 2018
- *Blurring the Lines between Memory and Compute*
  AMD Research, 2018
- *Pushing the Limits of Near Data Computing*
  University of Utah, 2016

- *Pushing the Limits of Near Data Computing*
  C-FAR e-workshop, 2016
- *Architecting Components for a 10 Billion Transistor Processor*
  University of Rochestor, 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  University of Southern California (USC), 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  John Hopkins University, 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  Georgia Institute of Technology (GaTech), 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  University of California, Los Angeles (UCLA), 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  University of California, Riverside, 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  University of Michigan, 2015
- *Architecting Components for a 10 Billion Transistor Processor*
  Purdue University, 2015
- *Energy Proportional Computing in the Era of Many-Core Processors*
  Third Annual Offering: Tutorial/Workshop on Energy-Secure System Architectures (ESSA 2013), co-located with ISCA 2013

Conference Talks

- *A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures*
  ISCA-34, San Diego, June 2007
- *Performance and Power Optimization through Data Compression in Network-on-Chip Architectures*
  HPCA-14, Raleigh, February 2008
- *MIRA : A Multilayered Interconnect Router Architecture*
  ISCA-35, Beijing, June 2008
- *Application-Aware Prioritization Mechanisms for On-Chip Networks*
  MICRO-42, New York, December 2009
- *Application-to-Core Mapping Policies to Reduce Memory System Interference in Multi-Core Systems*
  HPCA-19, Shenzen, February 2013
- *Catnap: Energy Proportional Multiple Network-on-Chip Architecture*
  ISCA-40, Tel Aviv, June 2013

Publications

Refereed Conferences

Names of graduate students whom I provided significant advise are underlined.

[1] Arun Subramaniyan, Jack Wadden, Kush Goliya, Nathan Ozog, Xiao Wu, Satish Narayanasamy, David T. Blaauw, and Reetuparna Das. Accelerated seeding for genome sequence alignment with enumerated radix

trees. In *48th ACM/IEEE Annual International Symposium on Computer Architecture, ISCA 2021, Valencia, Spain, June 14-18, 2021*, pages 388–401. IEEE, 2021.

[2] Arun Subramaniyan, Yufeng Gu, Timothy Dunn, Somnath Paul, Md. Vasimuddin, Sanchit Misra, David T. Blaauw, Satish Narayanasamy, and Reetuparna Das. Genomicsbench: A benchmark suite for genomics. In *IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 2021, Stony Brook, NY, USA, March 28-30, 2021*, pages 1–12. IEEE, 2021.

[3] Timothy Dunn, Harisankar Sadasivan, Jack Wadden, Kush Goliya, Kuan-Yu Chen, David T. Blaauw, Reetuparna Das, and Satish Narayanasamy. Squigglefilter: An accelerator for portable virus detection. In *MICRO '21: 54th Annual IEEE/ACM International Symposium on Microarchitecture, Virtual Event, Greece, October 18-22, 2021*, pages 535–549. ACM, 2021.

[4] Xiaowei Wang, Vidushi Goyal, Jiecao Yu, Valeria Bertacco, Andrew Boutros, Eriko Nurvitadhi, Charles Augustine, Ravi R. Iyer, and Reetuparna Das. Compute-capable block rams for efficient deep learning acceleration on fpgas. In *29th IEEE Annual International Symposium on Field-Programmable Custom Computing Machines, FCCM 2021, Orlando, FL, USA, May 9-12, 2021*, pages 88–96. IEEE, 2021.

[5] Vidushi Goyal, Valeria Bertacco, and Reetuparna Das. Myml: User-driven machine learning. In *58th ACM/IEEE Design Automation Conference, DAC 2021, San Francisco, CA, USA, December 5-9, 2021*, pages 145–150. IEEE, 2021.

[6] Daichi Fujiki, Shunhao Wu, Nathan Ozog, Kush Goliya, David T. Blaauw, Satish Narayanasamy, and **Reetuparna Das**. Seedex: A genome sequencing accelerator for optimal alignments in subminimal space. In *53rd Annual IEEE/ACM International Symposium on Microarchitecture, **MICRO** 2020, Athens, Greece, October 17-21, 2020*, pages 937–950. IEEE, 2020.

[7] Vidushi Goyal, Valeria Bertacco, and **Reetuparna Das**. Seesaw: End-to-end dynamic sensing for iot using machine learning. In *57th ACM/IEEE Design Automation Conference, **DAC** 2020, San Francisco, CA, USA, July 20-24, 2020*, pages 1–19. IEEE, 2020.

[8] Vidushi Goyal, Xiaowei Wang, Valeria Bertacco, and **Reetuparna Das**. Neksus: An interconnect for heterogeneous system-in-package architectures. In *2020 IEEE International Parallel and Distributed Processing Symposium (**IPDPS**), New Orleans, LA, USA, May 18-22, 2020*, pages 12–21. IEEE, 2020.

[9] Xiao Wu, Arun Subramaniyan, Zhehong Wang, Satish Narayanasamy, **Reetuparna Das**, and David T. Blaauw. 17.3 GCUPS pruning-based pair-hidden-markov-model accelerator for next-generation DNA sequencing. In *IEEE Symposium on VLSI Circuits, **VLSI Circuits** 2020, Honolulu, HI, USA, June 16-19, 2020*, 2020.

[10] Zhehong Wang, Tianjun Zhang, Daichi Fujiki, Arun Subramaniyan, Xiao Wu, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, **Reetuparna Das** , Satish Narayanasamy, and David T. Blaauw. A 2.46m reads/s genome sequencing accelerator using a 625 processing-element array. In *2020 IEEE Custom Integrated Circuits Conference, **CICC** 2020, Boston, MA, USA, March 22-25, 2020*. IEEE, 2020.

[11] Xiaowei Wang, Charles Augistine, Ravi Iyer, and **Reetuparna Das**. Bit Prudent In-Cache Acceleration of Deep Convolutional Neural Networks. In *Proceedings of the 25th International Symposium on High Performance Computer Architecture (**HPCA-25**)*, 2019.

[12] Kevin Angstadt, Arun Subramaniyan, Elaheh Sadredini, Reza Rahimi, Kevin Skadron, Westley Weimer, and **Reetuparna Das**. ASPEN: A Scalable In-SRAM Architecture for Pushdown Automata. *To appear in the 51st Annual IEEE/ACM International Microarchitecture (**MICRO-51**)*, 2018.

[13] Daichi Fuijiki, Arun Subramaniyan, Tianjun Zhang, Yu Zeng, **Reetuparna Das**, David Blaauw, and Satish Narayanasamy. Genax: A genome sequencing accelerator. In *Proceedings of the 45th International Symposium on Computer Architecture (**ISCA-45**)*, 2018.

[14] Charles Eckert, Xiaowei Wang, Jingcheng Wang, Arun Subramaniyan, Ravi Iyer, Dennis Sylvester, David Blaauw, and **Reetuparna Das**. Neural Cache: In-Cache Acceleration of Deep Neural Networks. In *Proceedings of the 45th International Symposium on Computer Architecture (**ISCA-45**)*, 2018.

[15] Daichi Fuijiki, Scott Mahlke, and **Reetuparna Das**. In memory data parallel processor. In *Proceedings of the 23rd ACM Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS-23**)*, 2018.

[16] Arun Subramaniyan, Jingcheng Wang, Ezhil R. M. Balasubramanian, David Blaauw, Dennis Sylvester, and **Reetuparna Das**. Cache Automaton. In *Proceedings of the 50th Annual IEEE/ACM International Microarchitecture (**MICRO-50**)*, 2017.

[17] Shruti Padmanabha, Andrew Lukefahr, **Reetuparna Das**, and Scott Mahlke. Mirage Cores: The Illusion of Many Out-of-order Cores Using In-order Hardware. In *Proceedings of the 50th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO-50**)*, 2017.

[18] Jiecao Yu, Andrew Lukefahr, Ganesh Dasika David Palframan, **Reetuparna Das**, and Scott Mahlke. Scalpel: Customizing DNN Pruning to the Underlying Hardware Parallelism. In *Proceedings of the 44th International Symposium on Computer Architecture (**ISCA-44**)*, 2017.

[19] Arun Subramaniyan and **Reetuparna Das**. Parallel Automata Processor. In *Proceedings of the 44th International Symposium on Computer Architecture (**ISCA-44**)*, 2017.

[20] Shaizeen Aga, Supreet Jeloka, Arun Subramaniyan, Satish Narayanasamy, David Blaauw, and **Reetuparna Das**. Compute caches. In *Proceedings of the 23rd International Symposium on High Performance Computer Architecture (**HPCA-23**)*, 2017.

[21] Salessawi Ferede Yitbarek, Misiker Tadesse Aga, **Reetuparna Das**, and Todd Austin. Anvil: Software-based protection against next-generation rowhammer attacks. In *Proceedings of the 23rd International Symposium on High Performance Computer Architecture (**HPCA-23**)*, 2017.

[22] Zelalem Birhanu Aweke, Salessawi Ferede Yitbarek, Rui Qiao, **Reetuparna Das**, Matthew Hicks, Yossi Oren, and Todd Austin. Anvil: Software-based protection against next-generation rowhammer attacks. In *Proceedings 21st ACM Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS-21**)*, 2016.

[23] Shruti Padmanabha, Andrew Lukefahr, **Reetuparna Das**, and Scott Mahlke. DynaMOS: Dynamic Schedule Migration for Heterogeneous Cores. In *Proceedings of the 48th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO-48**)*, 2015.

[24] William Arthur, Sahil Madeka, **Reetuparna Das**, and Todd Austin. Locking down insecure indirection with hardware-based control-data isolation. In *Proceedings 48th IEEE/ACM International Symposium on Microarchitecture (**MICRO-48**)*, 2015.

[25] William Arthur, Ben Mehne, **Reetuparna Das**, and Todd Austin. Getting in Control of Your Control Flow with Control-Data Isolation. In *Proceedings of the International Symposium on Code Generation and Optimization (**CGO**)*, 2015.

[26] Supreet Jeloka, **Reetuparna Das**, Ronald Dreslinski, Trevor Mudge, and David Blaauw. Hi-Rise: A High-Radix Switch for 3D Integration with Single-cycle Arbitration. In *Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO-47**)*, 2014.

[27] Andrew Lukefahr, Shruti Padmanabha, **Reetuparna Das**, Ronald Dreslinski, Thomas Wenisch, and Scott Mahlke. Heterogeneous Microarchitectures Trump Voltage Scaling for Mobile Cores. In *Proceedings of the 23rd International Conference on Parallel Architectures and Compilation Techniques (**PACT-23**)*, 2014.

[28] Supriya Rao, Supreet Jeloka, **Reetuparna Das**, Ronald Dreslinski, David Blaauw, and Trevor Mudge. VIX: Virtual Input Crossbars for Efficient Switch Allocation. In *Proceedings of the 51st Design Automation Conference (**DAC-51**)*, 2014.

[29] Ritesh Parikh, **Reetuparna Das**, and Valeria Bertacco. Power-Aware NoCs through Routing and Topology Reconfiguration. In *Proceedings of the 51st Design Automation Conference (**DAC-51**)*, 2014.

[30] Nilmini Abeyratne, Supreet Jeloka, Yiping Kang, **Reetuparna Das**, Ronald Dreslinski, David Blaauw, and Trevor Mudge. High Radix Self-Arbitrating Switch Fabric with Multiple Arbitration Schemes and Quality of Service. In *Proceedings of the 51st Design Automation Conference (**DAC-51**)*, 2014.

[31] Rachata Ausavarungnirun, Chris Fallin, Xiangyao Yu, Kevin Chang, Greg Nazario, **Reetuparna Das**, Gabriel Loh, and Onur Mutlu. Design and Evaluation of Hierarchical Rings with Deflection Routing. In *Proceedings of the 26th International Symposium on Computer Architecture and High Performance Computing (**SBAC-PAD**)*, 2014.

[32] Shruti Padmanabha, Andrew Lukefahr, **Reetuparna Das**, and Scott Mahlke. Trace Based Phase Prediction For Tightly-Coupled Heterogeneous Cores. In *Proceedings of the 46th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO-46**)*, 2013.

[33] **Reetuparna Das**, Satish Narayanasamy, Sudhir Satpathy, and Ronald G. Dreslinski. Catnap: Energy Proportional Multiple Network-on-Chip Architecture. In *Proceedings of the 40th International Symposium on Computer Architecture (**ISCA-40**)*, 2013.

[34] Nilmini Abeyratne, **Reetuparna Das**, Qingkun Li, Korey Sewell, Bharan Giridhar, Ronald G. Dreslinski, David Blaauw, and Trevor Mudge. Scaling Towards Kilo-Core Processors with Asymmetric High Radix Topologies. In *Proceedings of the 19th International Symposium on High Performance Computer Architecture (**HPCA-19**)*, 2013.

[35] **Reetuparna Das**, Rachata Ausavarungnirun, Onur Mutlu, Akhilesh Kumar, and Mani Azimi. Application-to-Core Mapping Policies to Reduce Memory System Interference in Multi-Core Systems. In *Proceedings of the 19th International Symposium on High Performance Computer Architecture (**HPCA-19**)*, 2013.

[36] Andrew Lukefahr, Shruti Padmanabha, **Reetuparna Das**, Faissal Sleiman, Ronald Dreslinski, Thomas Wenisch, and Scott Mahlke. Composite Cores: Pushing Heterogeneity into a Core. In *Proceedings of the 45th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO-45**)*, 2012.

[37] Sudhir Satpathy, **Reetuparna Das**, Ronald Dreslinski, Trevor Mudge, Dennis Sylvester, and David Blaauw. High Radix Self-Arbitrating Switch Fabric with Multiple Arbitration Schemes and Quality of Service. In *Proceedings of the 49th Design Automation Conference (**DAC-49**)*, 2012.

[38] Ronald G. Dreslinski, Korey Sewell, Thomas Manville, Sudhir Satpathy, Nathaniel Ross Pinckney, Geoffrey Blake, Michael Cieslak, **Reetuparna Das**, Thomas F. Wenisch, Dennis Sylvester, David Blaauw, and Trevor N. Mudge. Swizzle switch: A self-arbitrating high-radix crossbar for noc systems. In *In IEEE Symposium of High Performance Chips* ***(HotChips-24)***, 2012.

[39] Ronald G. Dreslinski, Thomas Manville, Korey Sewell, **Reetuparna Das**, Nathaniel Pinckney, Sudhir Satpathy, David Blaauw, Dennis Sylvester, and Trevor Mudge. XPoint Cache: Scaling Existing Bus Based Coherence Protocols for 2D and 3D Many-Core Systems. In *Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques (****PACT-21****)*, 2012.

[40] **Reetuparna Das**, Rachata Ausavarungnirun, Onur Mutlu, Akhilesh Kumar, and Mani Azimi. Application-to-core mapping policies to reduce memory interference in multi-core systems. In *Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques (****PACT-21****),* ***Poster***, 2012.

[41] **Reetuparna Das**, Andres Mejia, Gaspar Mora Porta, Dongkook Park, Roy Saharoy, and Anahita Shayesteh. SIMORA: A Performance Evaluation Methodology for Manycore Interconnection Networks. In *Design and Test Technology Conference (****DTTC****), Intel*, 2011.

[42] **Reetuparna Das**, Onur Mutlu, Thomas Moscibroda, and Chita R Das. Aérgia: Exploiting Packet Latency Slack in On-Chip Networks. In *Proceedings of the 37th International Symposium on Computer Architecture (****ISCA-37, selected for IEEE Micro Top Picks Award****)*, 2010.

[43] Xiaoxia Wu, Guangyu Sun, Xiangyu Dong, **Reetuparna Das**, Jian Li, Yuan Xie, and Chita R. Das. Cost-driven 3D Integration with Interconnect Layers. In *Proceedings of the 47th Design Automation Conference (****DAC-47****)*, 2010.

[44] **Reetuparna Das**, Onur Mutlu, Thomas Moscibroda, and Chita R Das. Application-Aware Prioritization for On-Chip Networks. In *Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture(****MICRO-42****)*, 2009.

[45] Asit K. Mishra, **Reetuparna Das**, Soumya Eachempati, Vijaykrishnan Narayanan, Ravi Iyer, and Chita R. Das. A Case for Dynamic Frequency Tuning in On-Chip Networks. In *Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture(****MICRO-42****)*, 2009.

[46] Shekhar Srikantaiah, **Reetuparna Das**, Asit K. Mishra, Mahmut Kandemir, and Chita R. Das. A Case for Integrated Processor-Cache Partitioning in Chip Multiprocessors. In *International Conference for High Performance Computing, Networking, Storage, and Analysis,(****SC****)*, 2009.

[47] **Reetuparna Das**, Soumya Eachempati, Asit K. Mishra, Vijaykrishnan Narayanan, and Chita R. Das. Design and Evaluation of Hierarchical On-Chip Network Topologies for next generation CMPs. In *Proceedings of 15th International Conference on High-Performance Computer Architecture (****HPCA-15****)*, 2009.

[48] Dongkook Park, Soumya Eachempati, **Reetuparna Das**, Asit K. Mishra, Vijaykrishnan Narayanan, Yuan Xie, and Chita R. Das. MIRA : A Multilayered Interconnect Router Architecture. In *Proceedings of 35th International Symposium on Computer Architecture (****ISCA-35****)*, 2008.

[49] **Reetuparna Das**, Asit K. Mishra, Chrysostomos Nicopoulos, Dongkook Park, Vijaykrishnan Narayanan, Ravi Iyer, and Chita R. Das. Performance and Power Optimization through Data Compression in Network-on-Chip Architectures. In *Proceedings of 14th International Conference on High-Performance Computer Architecture (****HPCA-14****)*, 2008.

[50] Jongman Kim, Chrysostomos Nicopoulos, Dongkook Park, **Reetuparna Das**, Yuan Xie, Vijaykrishnan Narayanan, Mazin S. Yousif, and Chita R. Das. A novel dimensionally-decomposed router for on-chip communication in 3D architectures. *Proceedings of 34th International Symposium on Computer Architecture (**ISCA-34**)*, 2007.

[51] Dongkook Park, **Reetuparna Das**, Chrysostomos Nicopoulos, Jongman Kim, Narayanan Vijaykrishnan, Ravishankar Iyer, and Chita R. Das. Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects. *Proceedings of 15th IEEE Symposium on High-Performance Interconnects Stanford University (**HOTI-15**)*, 2007.

Journals

[52] Jingcheng Wang, Xiaowei Wang, Charles Eckert, Arun Subramaniyan, Reetuparna Das, David T. Blaauw, and Dennis Sylvester. A 28-nm compute SRAM with bit-serial logic/arithmetic operations for programmable in-memory vector computing. *IEEE J. Solid State Circuits*, 55(1):76–86, 2020.

[53] Korey Sewell, Ronald G. Dreslinski, Thomas Manville, Sudhir Satpathy, Nathaniel Ross Pinckney, Geoffrey Blake, Michael Cieslak, **Reetuparna Das**, Thomas F. Wenisch, Dennis Sylvester, David Blaauw, and Trevor N. Mudge. Swizzle-switch networks for many-core systems. *IEEE Journal of Emerging Selected Topics Circuits Systems*, 2012.

[54] **Reetuparna Das**, Onur Mutlu, Thomas Moscibroda, and Chita R Das. Aérgia: A Network-on-Chip Exploiting Packet Latency Slack. In *IEEE Micro Special Issue: Top Picks from Computer Architecture Conferences January/February*, 2011.

[55] Asit K. Mishra, Aditya Yanamandra, **Reetuparna Das**, Soumya Eachempati, Ravi Iyer, N. Vijaykrishnan, and Chita R. Das. RAFT: A Router Architecture with Frequency Tuning for On-chip Networks. In *Special Issue on On-Chip Networks: Journal of Parallel and Distributed Computing (JPDC)*, 2011.

Book Chapters

[56] Soumya Eachempati, **Reetuparna Das**, N. Vijaykrishnan, Suman Datta, Yuan Xie, and Chita R. Das. HeTERO: Hybrid Topology Exploration for RF based On Chip Networks. In *Communication Architectures for Systems-on-Chip*, 2011.

[57] Dongkook Park, Soumya Eachempati, **Reetuparna Das**, Asit K. Mishra, Vijaykrishnan Narayanan, Yuan Xie, and Chita R. Das. Three Dimensional On-Chip Interconnect Architectures. In *Designing Network-on-Chip Architectures in the Nanoscale Era*, 2011.

Patents

[58] Jiecao Yu, Andrew Lukefahr, David Palframan, **Reetuparna Das**, and Scott Mahlkee. Systems and Devices for Compressing Neural Network. US Patent (filed) 2017.

[59] Andrew Lukefahr, Shruti Padmanabha, Jiecao Yu, **Reetuparna Das**, and Scott Mahlke. Controlling Transition Between Using First and Second Processing Circuitry. US Patent (filed) 2016.

[60] Shruti Padmanabha, Andrew Lukefahr, **Reetuparna Das**, and Scott Mahlke. Controls of Switching Between Execution Mechanisms. US Patent (filed) 2014.

[61] Andrew Lukefahr, Shruti Padmanabha, **Reetuparna Das**, and Scott Mahlke. Heterogeneity Within A Processor Core. US Patent (filed) 2013.

[62] Shruti Padmanabha, Andrew Lukefahr, **Reetuparna Das**, and Scott Mahlke. Controls of switching between executed mechanisms.

[63] Nilmini Abeyratne, Supreet Jeloka, **Reetuparna Das**, Ronald Dreslinski, Trevor Mudge, and David Blaauw. Single-cycle Arbitration. US Patent (filed) 2013.

Personal

US Permanent Resident. Date of Birth - September 1982.