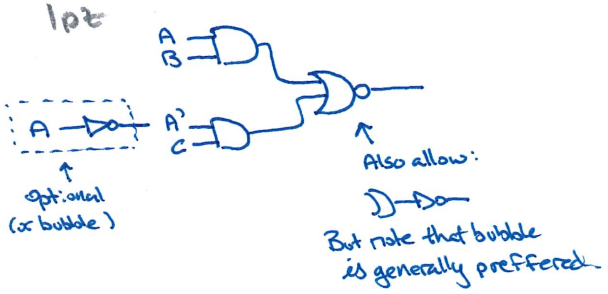
EECS 373 - W'15 - Homework #1a - KEY

Q1.a. 1pt

A	B	C	(AB)	(A'C)	((AB)+(A'C))'
1	1	1	1	0	0
1	1	0	1	0	0
1	0	1	0	0	1
1	0	0	0	0	1
0	1	1	0	1	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	0	0	1

optional

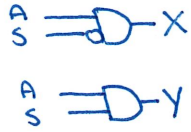
Q1.b. 1pt



Q2.a. 1pt

A	S	X	Y
1	1	0	1
1	0	1	0
0	1	0	0
0	0	0	0

Q2.b. 1pt

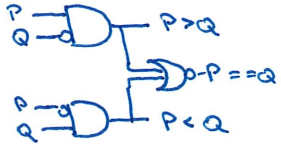


(variations of S' are fine)

Q3.a. 1pt

P	Q	P>Q	P==Q	P<Q
1	1	0	1	0
1	0	1	0	0
0	1	0	0	1
0	0	0	1	0

Q3.b. 1pt



(variations that are correct are fine)

Q4. 2pts

a. 1pt `assign X = (~A&B)|(~(~A&C))|(B&~C);` - 0.5 total if no semicolons

b. 1pt `assign {X,Y} = {A&~S, A&S};`

Q5. 6pts

a. 3pts

```
module DEMUX21 (
    input A,
    input S,
    output X,
    output Y
);
assign X = A&~S;
assign Y = A&S;
endmodule
```

b. 3pts

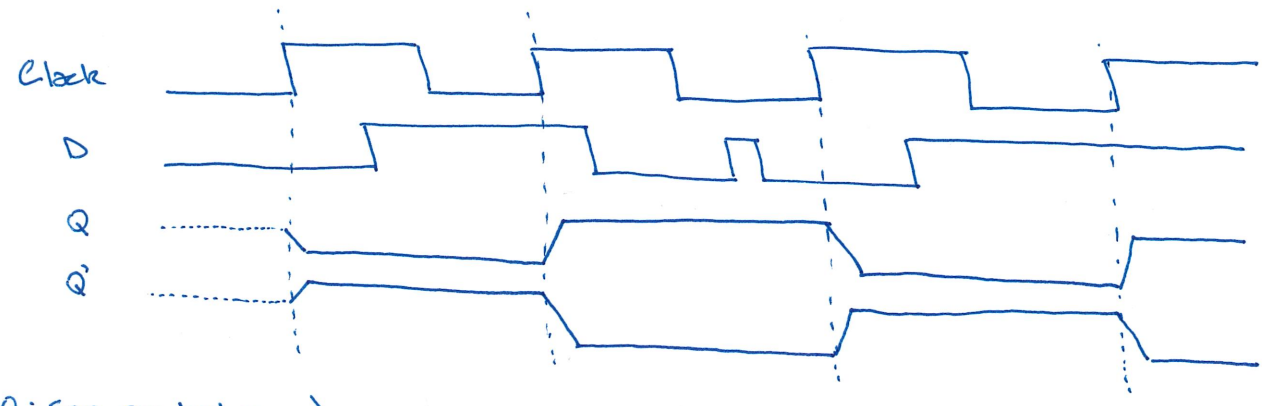
```
module DEMUX41 (
    input A,
    input [1:0] S,
    output [3:0] Z,
);
DEMUX21 dm1 (A, ~S[1]&S[0], Z[0], Z[1]);
DEMUX21 dm2 (A, S[1]&S[0], Z[2], Z[3]);

endmodule
```

Q6. 2pts

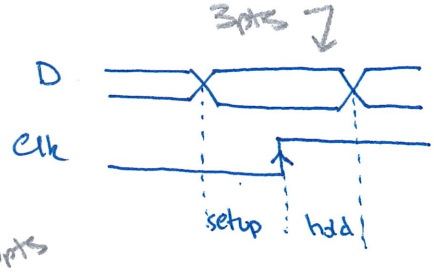
```
(same)
output reg X
output reg Y
...
always @(*) begin
    X = A&~S;
    Y = A&S;
end
```

Q7. -4pts, 1 per clk, .5 → Q, .5 → Q'



(Q8-10: see ~~last~~ last page)

Q11. -5pts



setup: input stable before clock edge ← 1pt

hold: input stable after clock edge ← 1pt

Q12. -10pts

a.

1pt i: A buffer that can turn its output "off". States are High (1), Low (0), and HighZ (Z). HiZ is high impedence, that is the output is functionally disconnected.

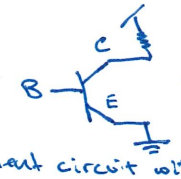
1pt ii: A drives high. Others HiZ

1pt iii: Drive same value (high or low) nothing. Drive high and low ⇒ short.

1pt iv: Undefined. HiZ is floating.

6pts b.

2pts i: A BJT where



collector is pulled high by a resistor and the emitter is grounded.

(note the equivalent circuit with a MOSFET is a open-drain, not open collector, but the terms are often used interchangably. Correct the error, but do not mark off for it).

The pull-up causes the collector ~~and~~ to be normally high.

1pt ii: A does nothing to drive 1. Othe devices also do nothing.

1pt iii: A turns on its BJT, grounding the circuit.

1pt iv: Invert the whole set-up (the high & use a pull down resistor)

1pt v: The size of the resistor, the capacitance of the collector network.

Rubric

Q1:	2pts	7:	4pts
2:	2pts	8:	5pts
3:	2pts	9:	5pts
4:	2pts	10:	5pts
5:	6pts	11:	5pts
6:	2pts	12	10pts

EECS 373 - Fall 14 - Homework # 1 - Key
Prabal Dutta

Q8. Build a module-4 counter: 0 → 1 → 2 → 3

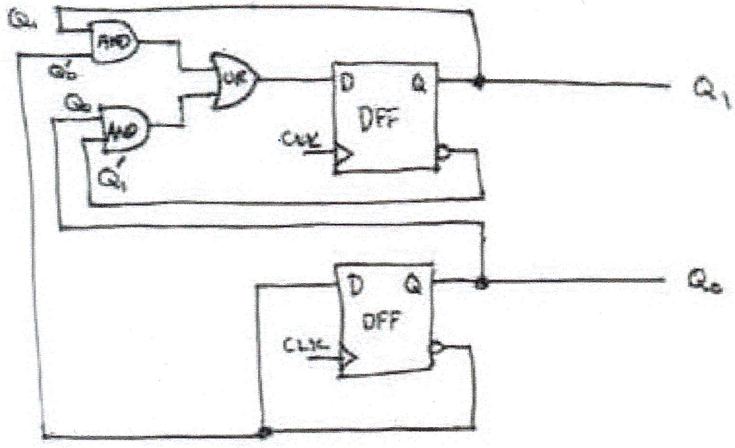
5 pts

2 pts if close but wrong

PS Q_1	PS Q_0	NS Q_1	NS Q_0	D_1	D_0
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

$D_1 = Q_1 \oplus Q_0 = Q_1' \cdot Q_0 + Q_1 \cdot Q_0'$

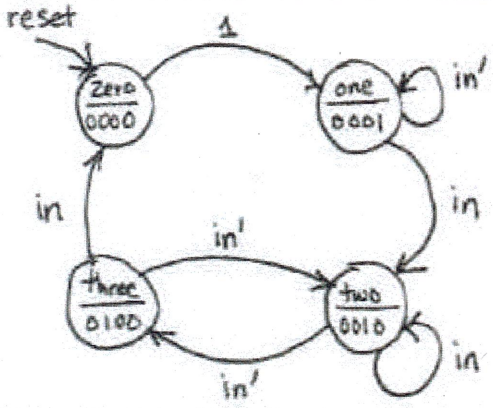
$D_0 = Q_0'$



Q10

5 pts

2 pts if close but wrong.



Q9 - 5pts

a. 3 bits are used. 1pt

Could have been done w/ 2. 1pt

b. always @*

pro
- clear, readable for complex state machines
- compiler can verify all cases covered

con
- can be verbose
- easy to accidentally miss a case

assigns

pro
- concise, easier to read for simple expressions

con
- hard to understand w/ many states
- hard to spot typos

1pt per claim, upto 3

(accept any other reasonable arguments)