PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications

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MICRO-51

http://check.cs.princeton.edu/

Memory Consistency Models (MCMs)

- Specify rules governing values returned by loads in parallel programs
- MCM must be correctly implemented for **all possible programs**

Compiler

Microarchitecture

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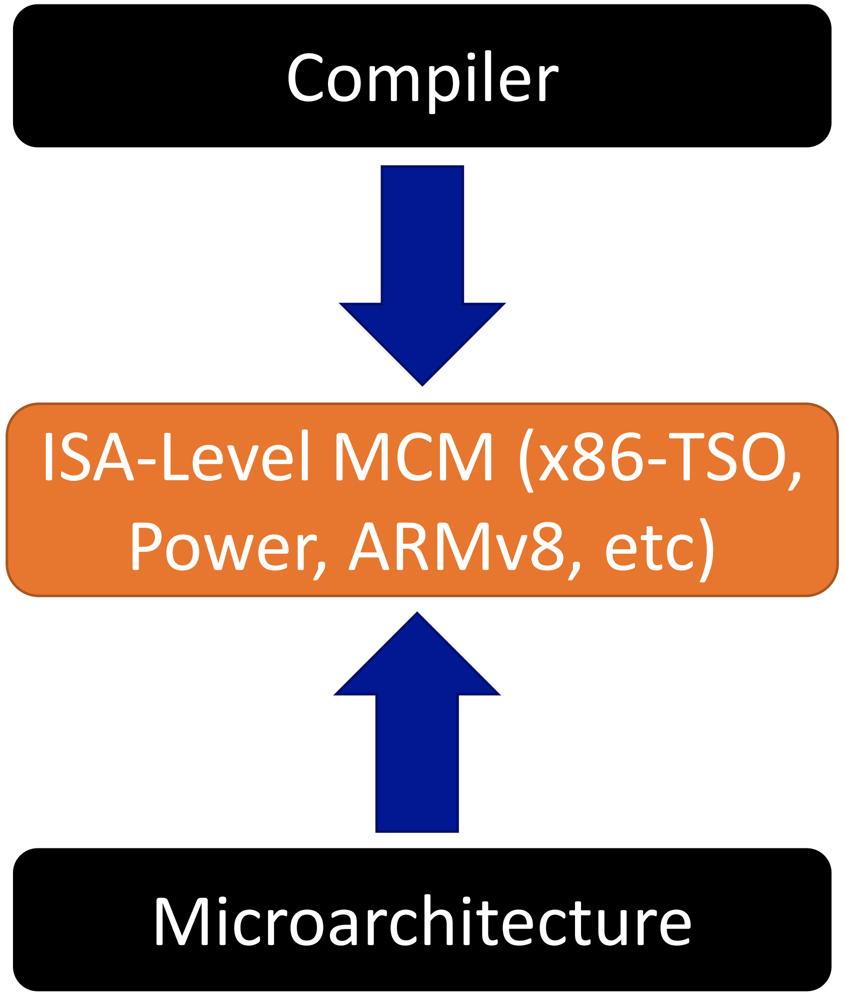

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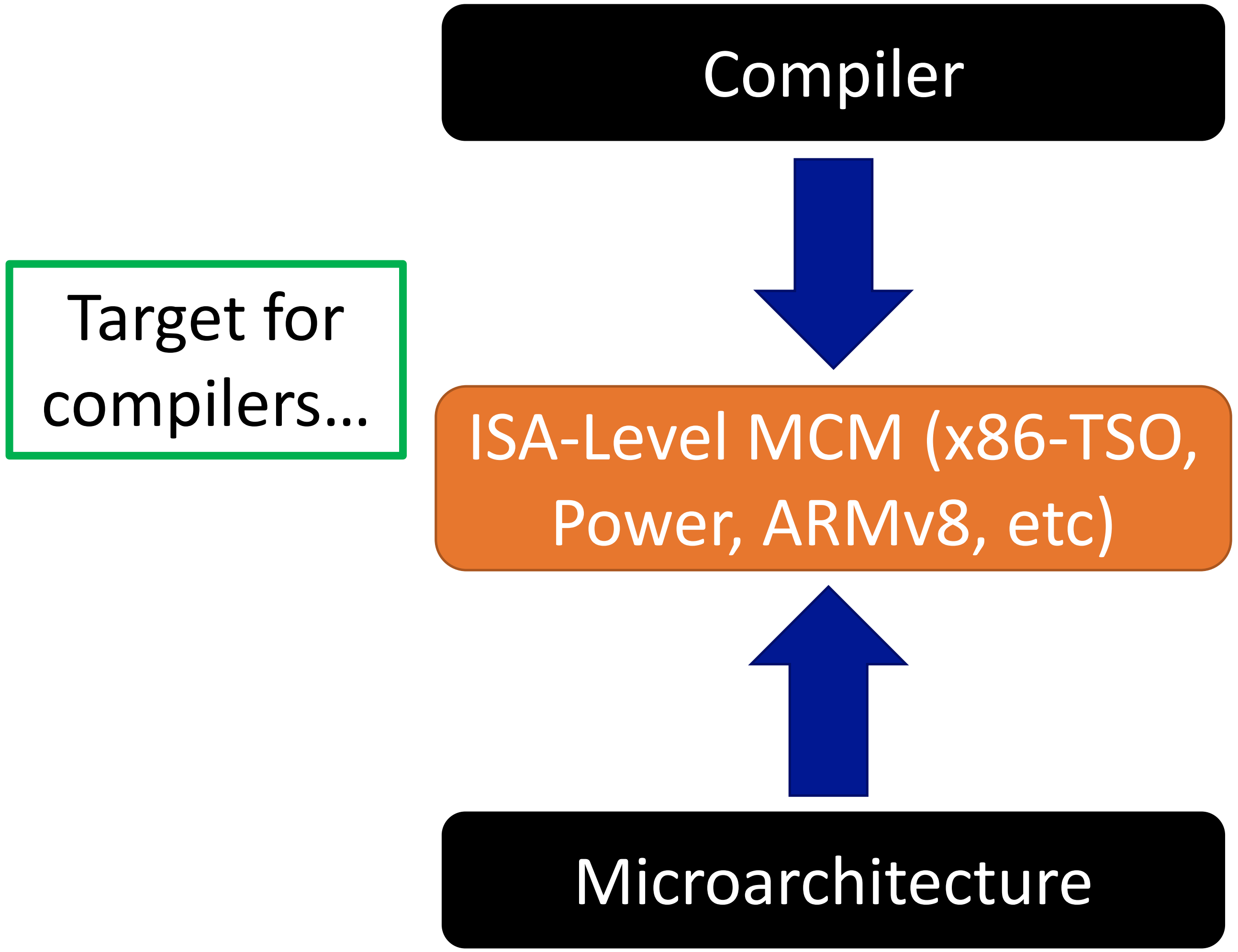

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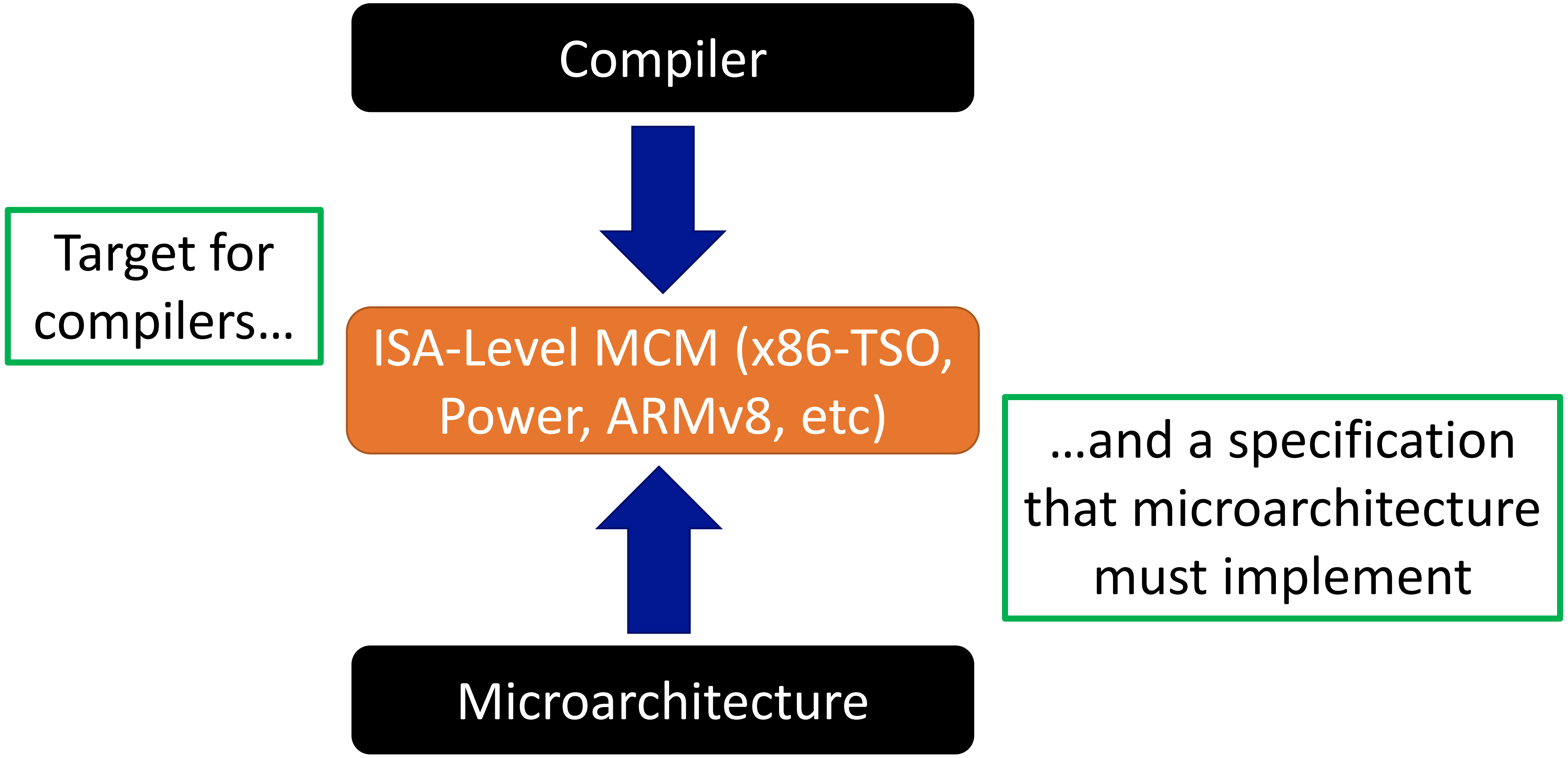
Compiler
Target for compilers…
ISA-Level MCM (x86-TSO, Power, ARMv8, etc)
…and a specification that microarchitecture must implement
Microarchitecture

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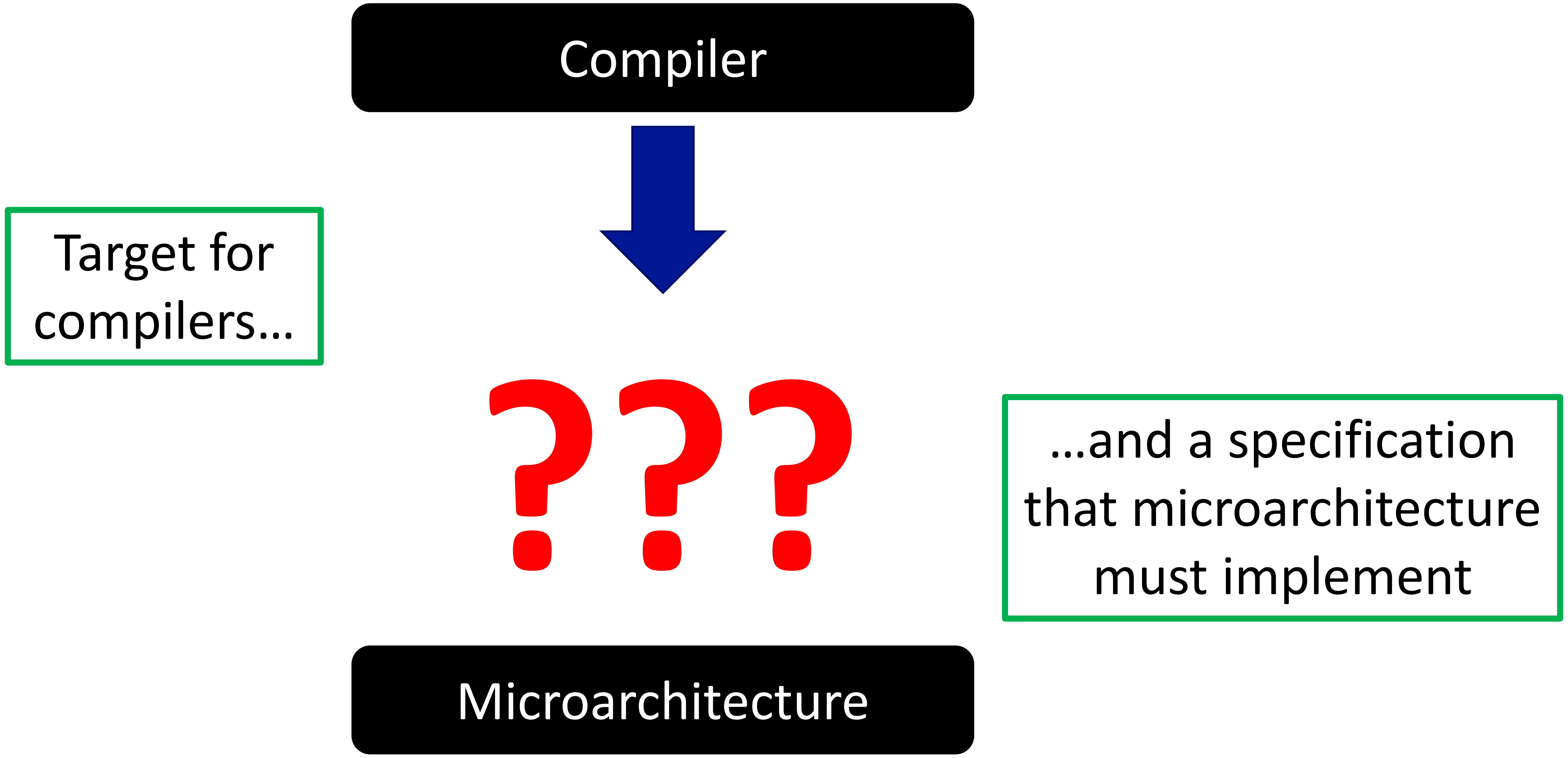
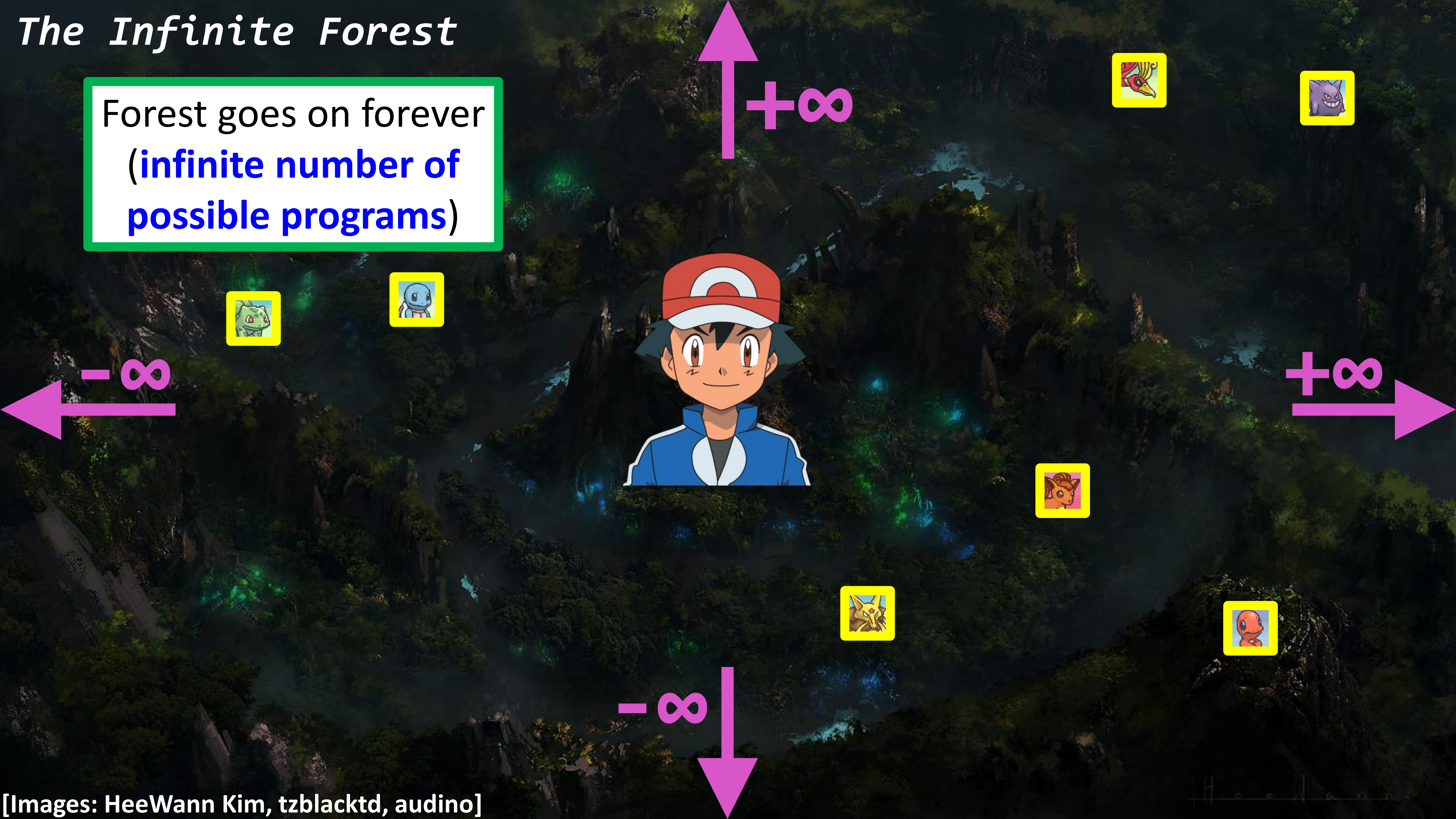


The Infinite Forest

[Images: HeeWann Kim, tzblacktd, audino]

The Infinite Forest

Forest goes on forever (**infinite number of possible programs**)



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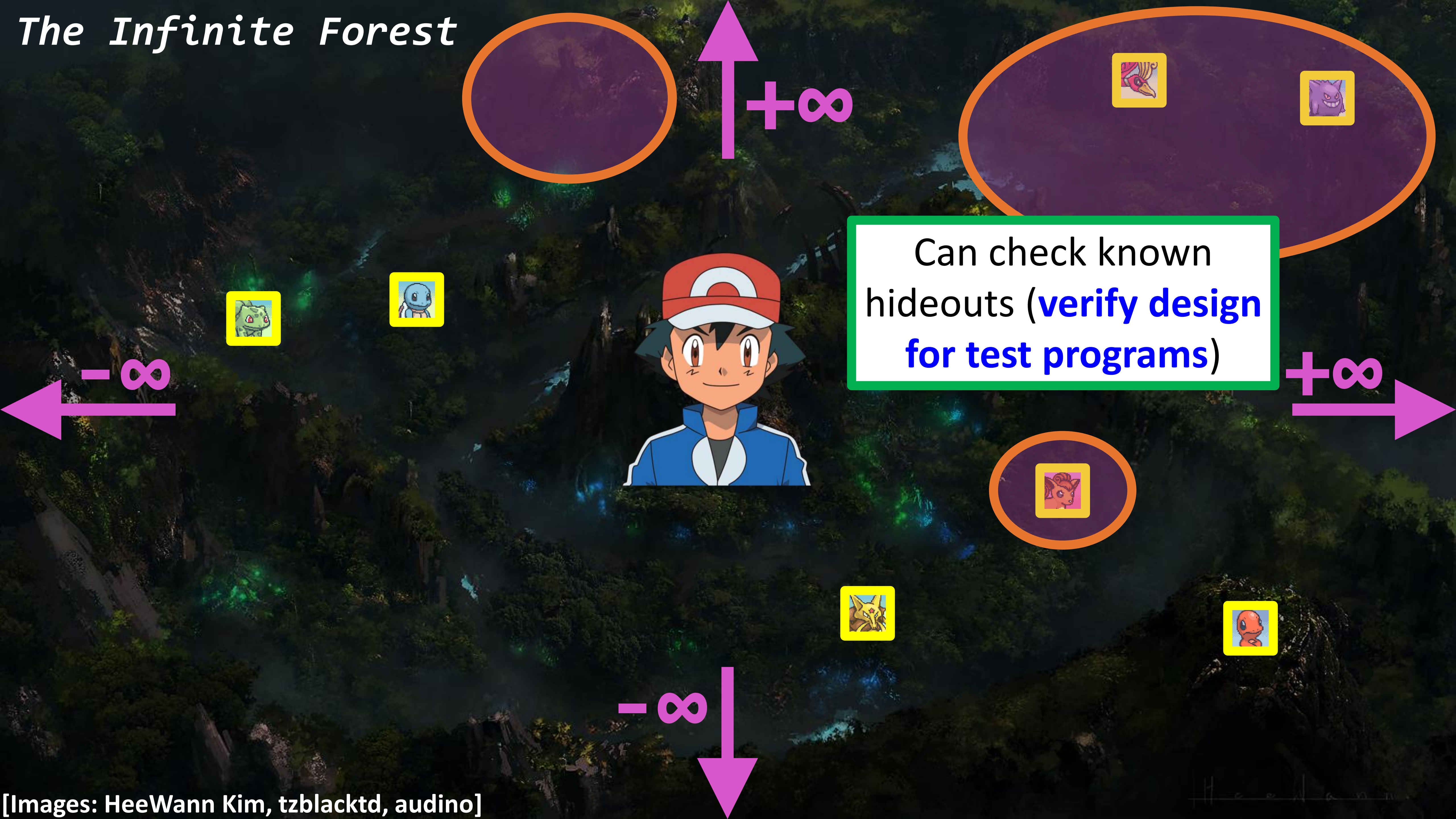

Can check known hideouts (**verify design for test programs**)

[Images: HeeWann Kim, tzblacktd, audino]

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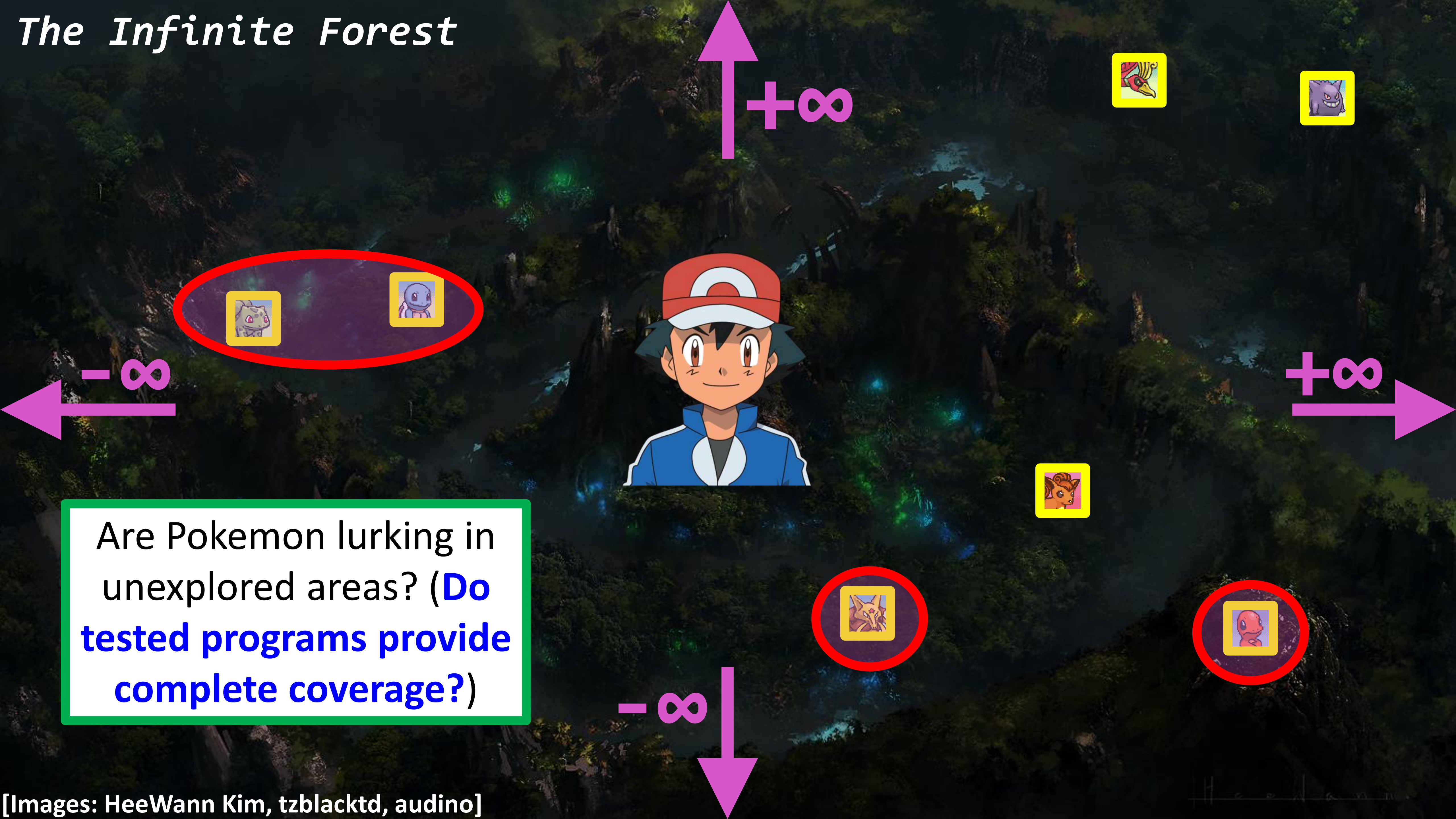


Are Pokemon lurking in unexplored areas? (**Do tested programs provide complete coverage?**)

[Images: HeeWann Kim, tzblacktd, audino]

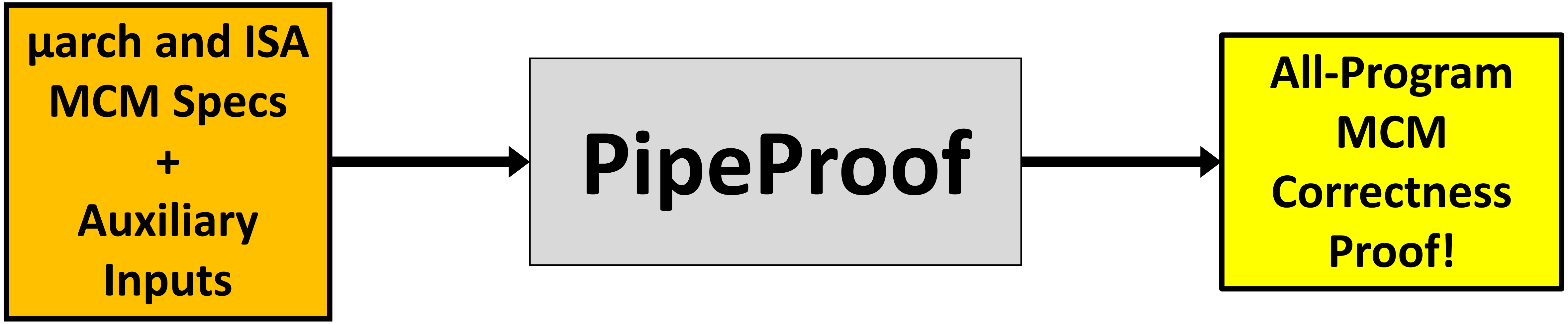
The Infinite Forest

Have we caught all the Pokemon?
(**Are there any MCM bugs left in the design?**)

[Images: HeeWann Kim, tzblacktd, audino]

PipeProof Overview

- **First automated all-program microarchitectural MCM verification!**
  - Covers all possible addresses, values, numbers of cores
- Proof methodology based on automatic abstraction refinement
- Early-stage: Can be conducted before RTL is written!


µarch and ISA MCM Specs + Auxiliary Inputs
PipeProof
All-Program MCM Correctness Proof!

Outline

- Background
  - ISA-level MCM specs
  - Microarchitectural ordering specs
- Microarchitectural Correctness Proof
  - Transitive Chain (TC) Abstraction
- Overall PipeProof Operation
  - TC Abstraction Support Proof
  - Chain Invariants
- Results

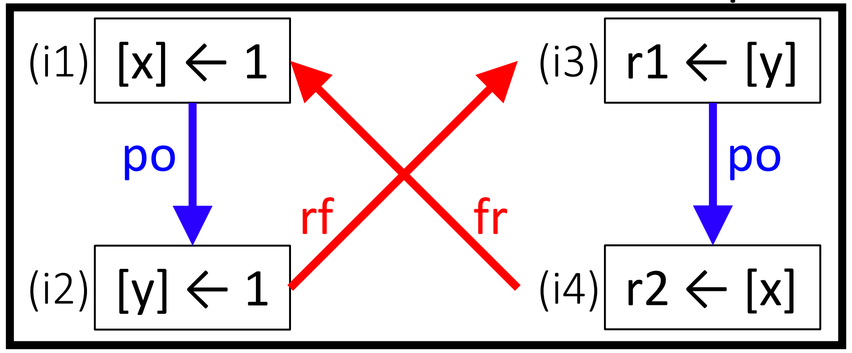
ISA-Level MCM Specifications

- Defined in terms of relational patterns [Alglave et al. TOPLAS 2014]
- ISA-level executions are graphs
  - **Nodes:** instructions, **edges:** ISA-level relations between instrs
- Correctness based on acyclicity, irreflexivity, etc of relational patterns
  - Eg: SC is $acyclic(po \cup co \cup rf \cup fr)$

Message passing (mp) litmus test

Core 0	Core 1
(i1) $[x] \leftarrow 1$ (i2) $[y] \leftarrow 1$	(i3) $r1 \leftarrow [y]$ (i4) $r2 \leftarrow [x]$
Under SC: Forbid r1=1, r2=0	

An ISA-level execution of mp



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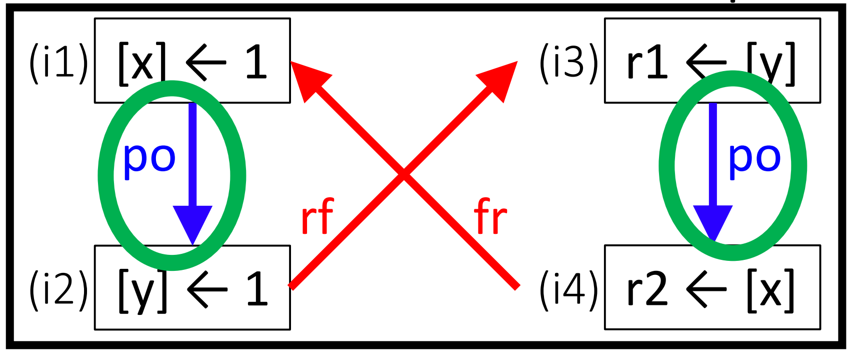

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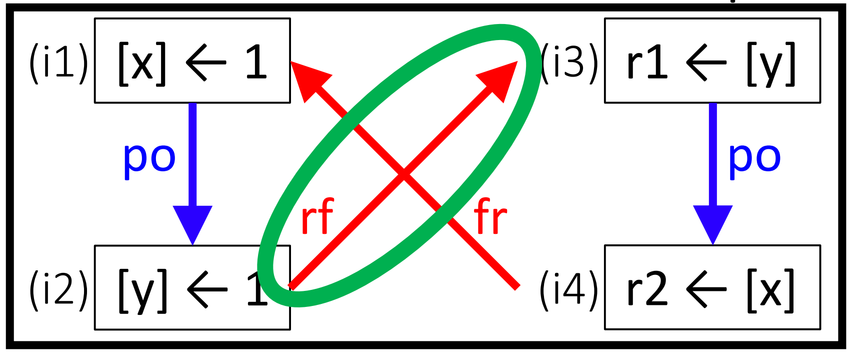

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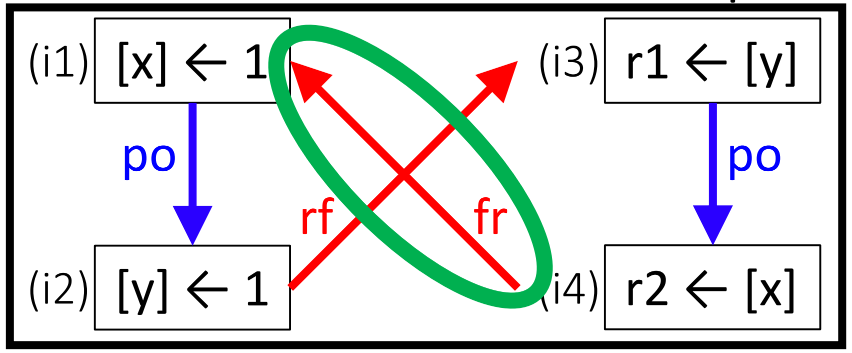

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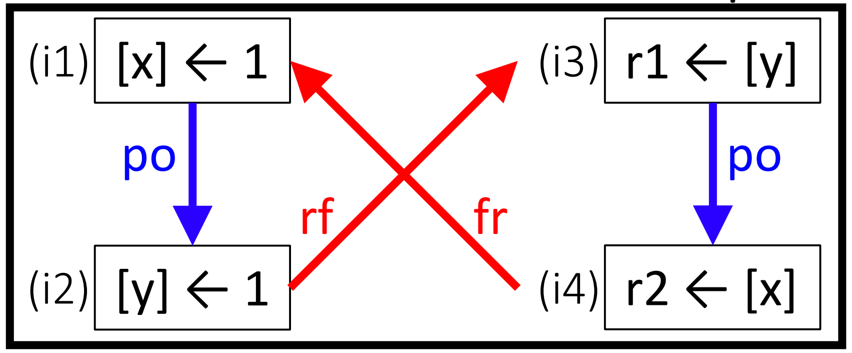

Microarchitectural Ordering Specifications

- Set of axioms in µspec DSL [Lustig et al. ASPLOS 2016]
- Used to generate microarchitectural executions as **µhb graphs**
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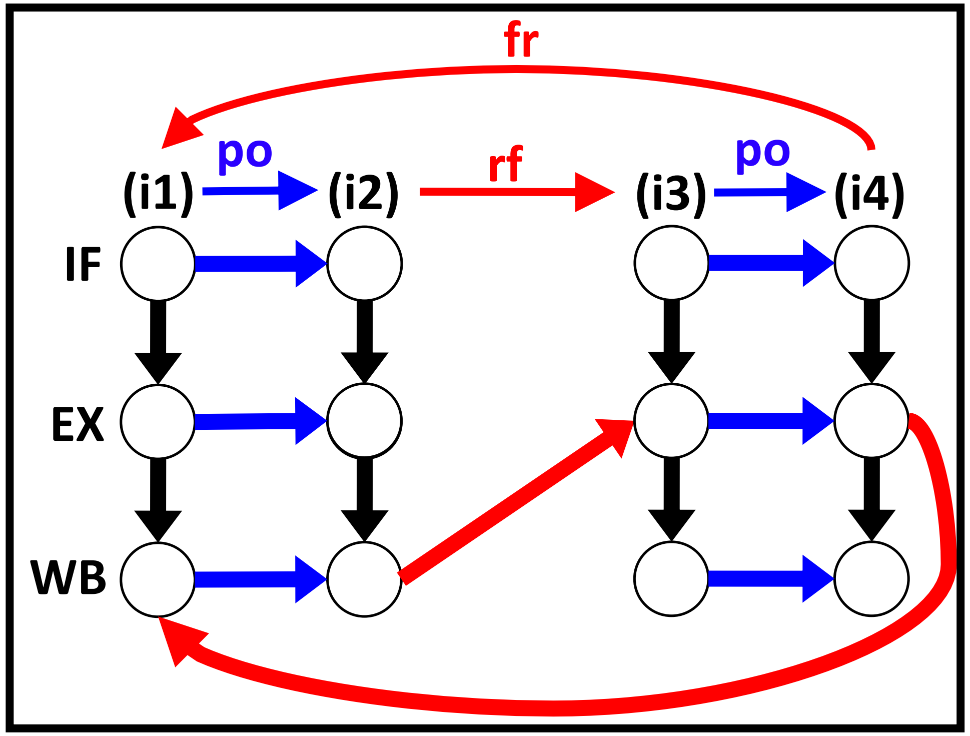
A µhb graph of mp on simpleSC



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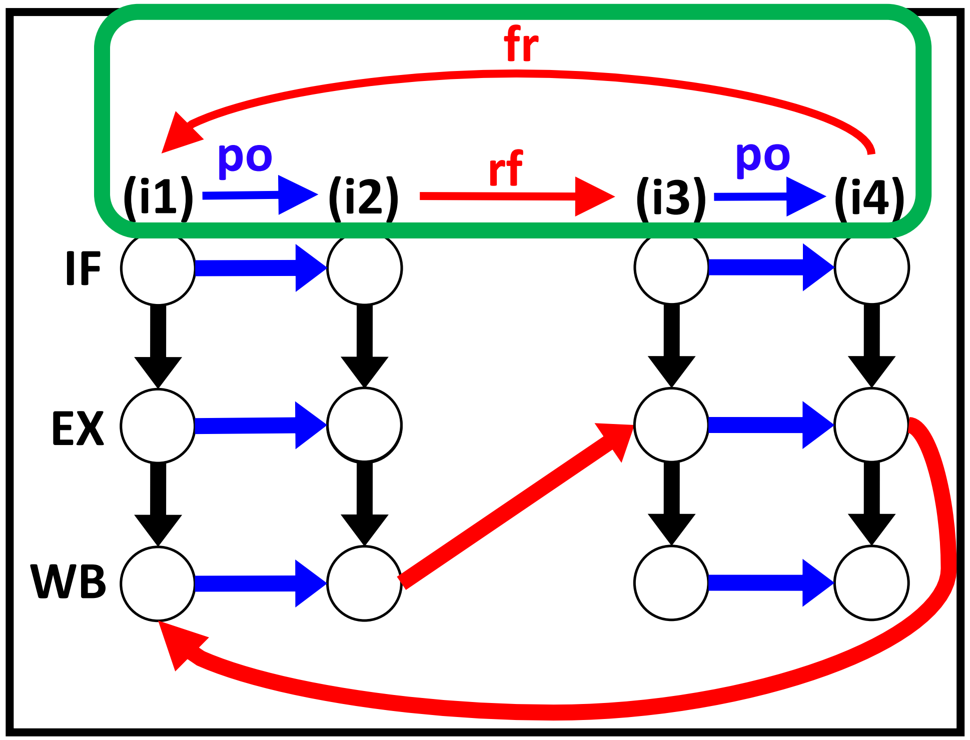

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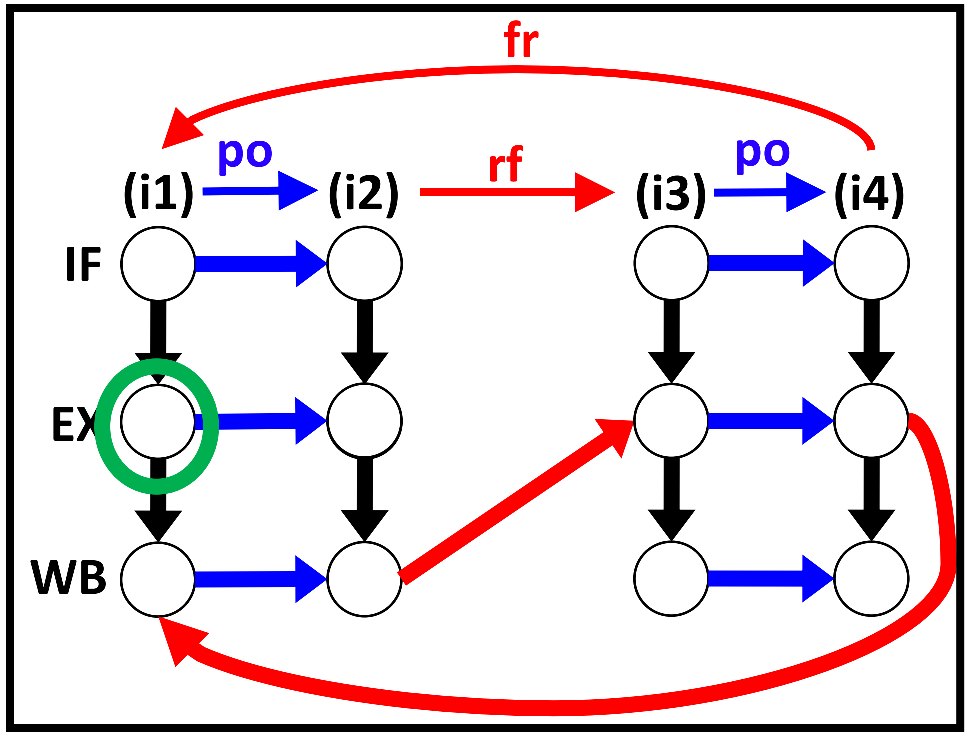

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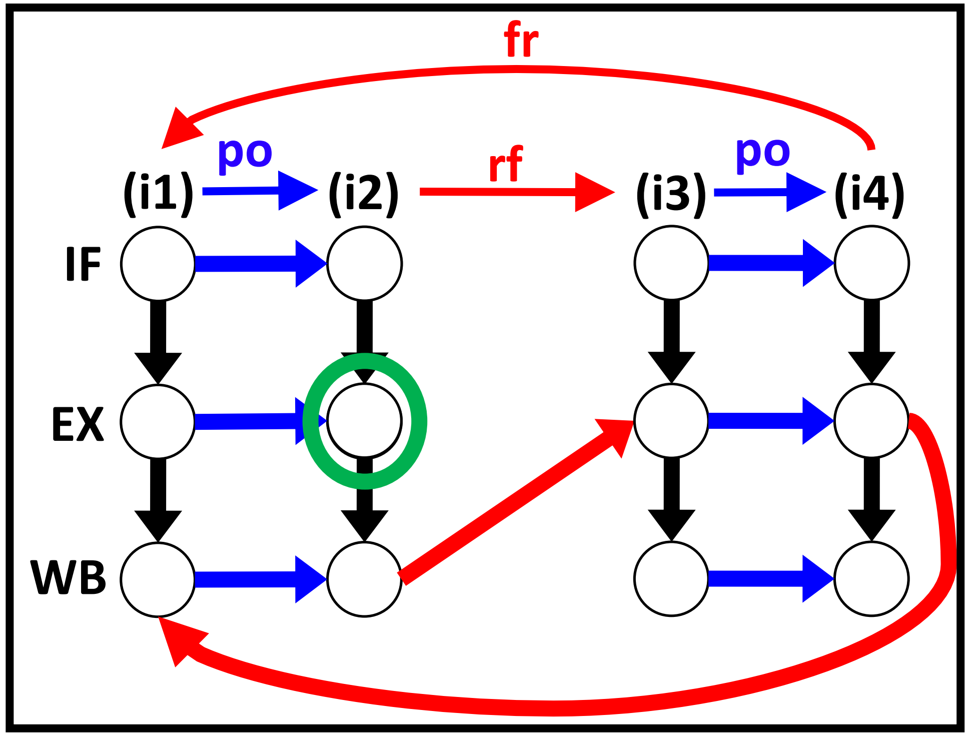

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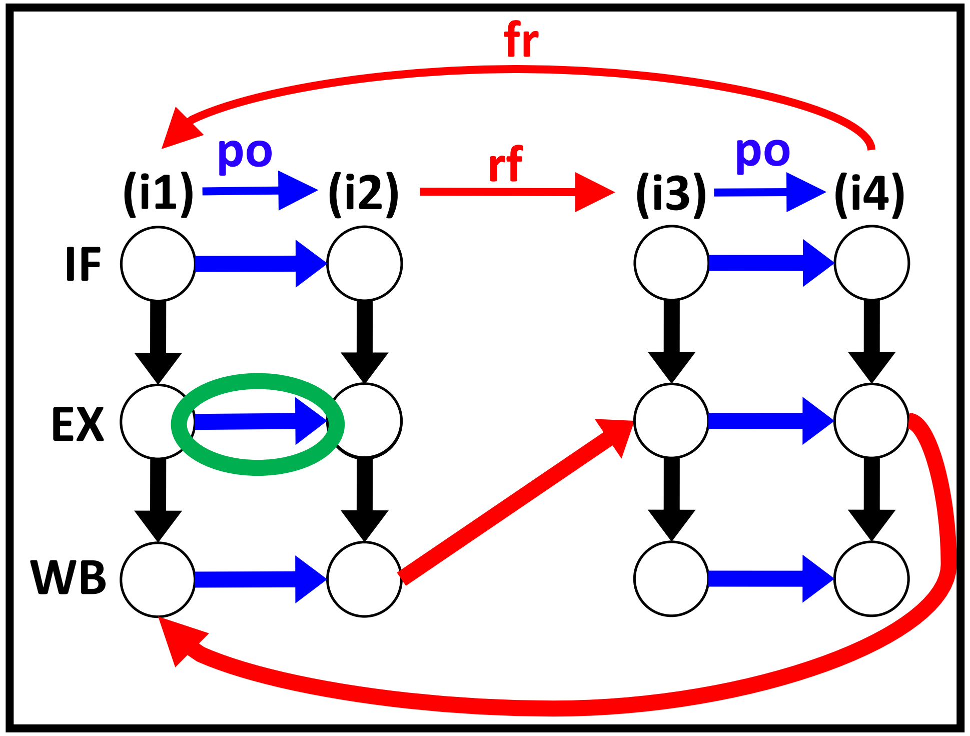

Our Prior Work: Litmus Test-Based MCM Verification

Microarchitecture in μspec DSL

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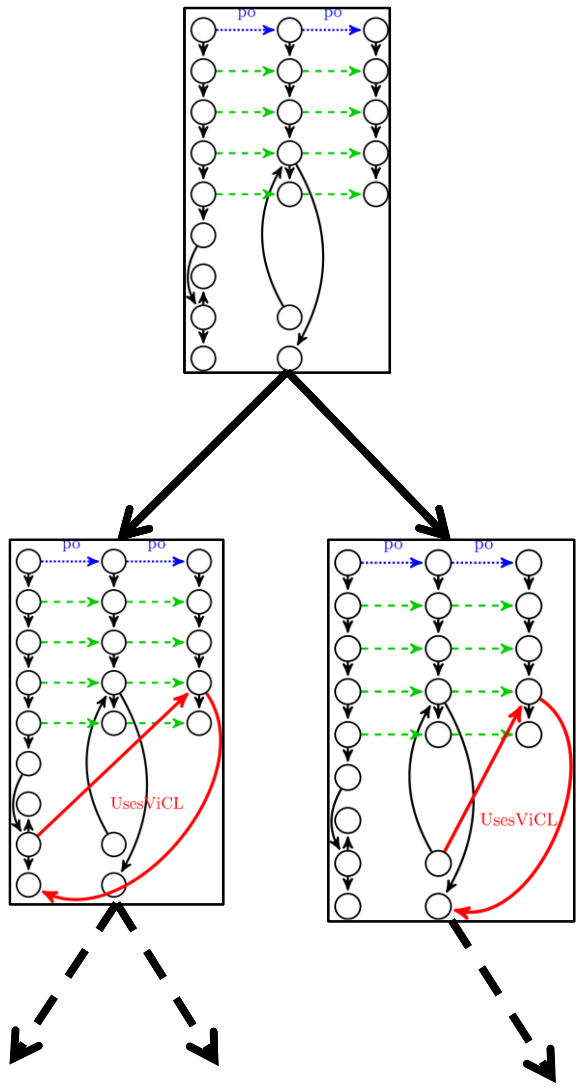

Microarchitectural happens-before (μhb) graphs

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Allowed	OK	OK (stricter than necessary)
Forbidden	Consistency violation!	OK

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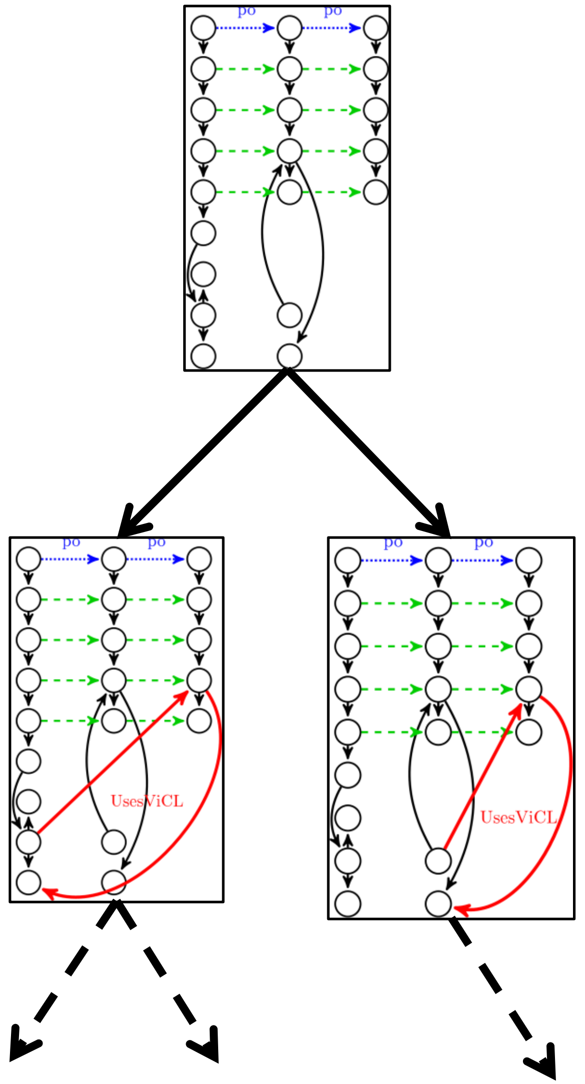

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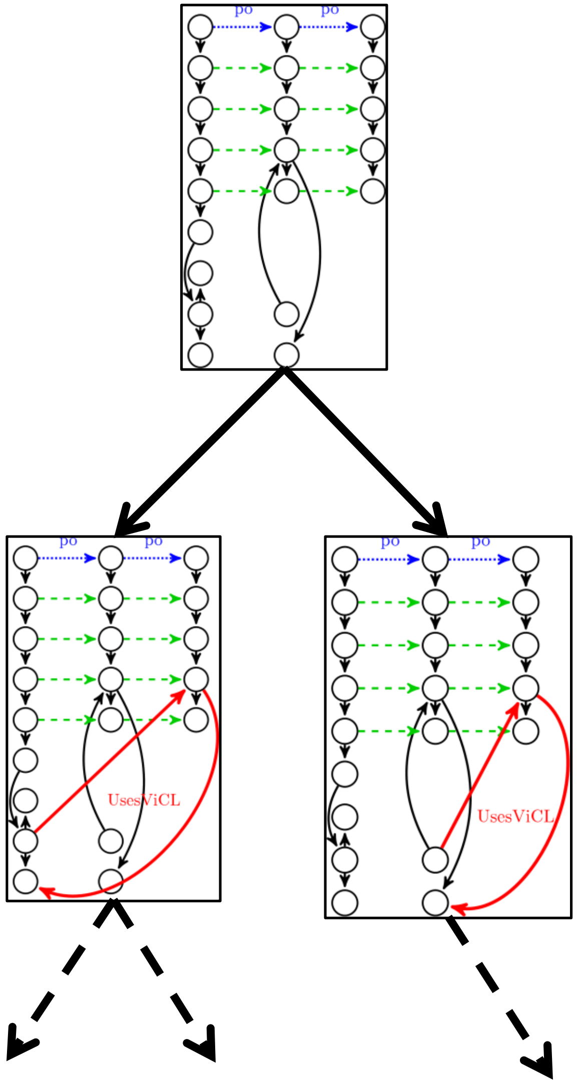

Microarchitectural happens-before (μhb) graphs

[Lustig et al. MICRO-47, …]

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Perennial Question:

"Do your litmus tests cover all possible MCM bugs?"

How to automatically prove correctness for all programs?

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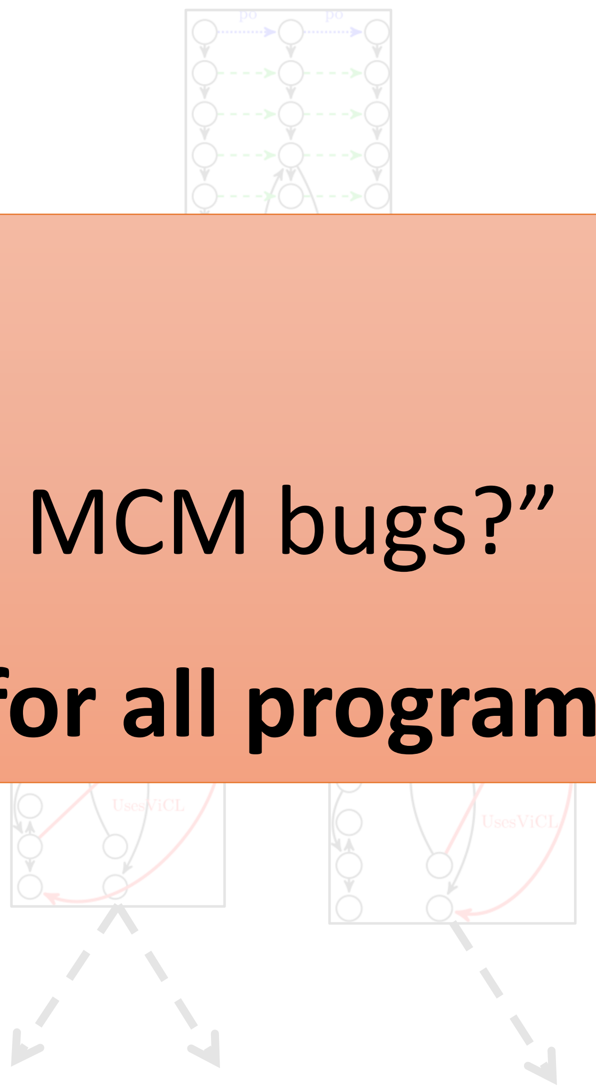

Microarchitectural happens-before (μhb) graphs

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The Transitive Chain (TC) Abstraction

All non-unary cycles containing fr

$$\begin{tikzcd} i_1 \arrow[r, dashed, "r_{1\ldots n-1}"] & i_n \arrow[l, bend right, "fr"'] \end{tikzcd}$$

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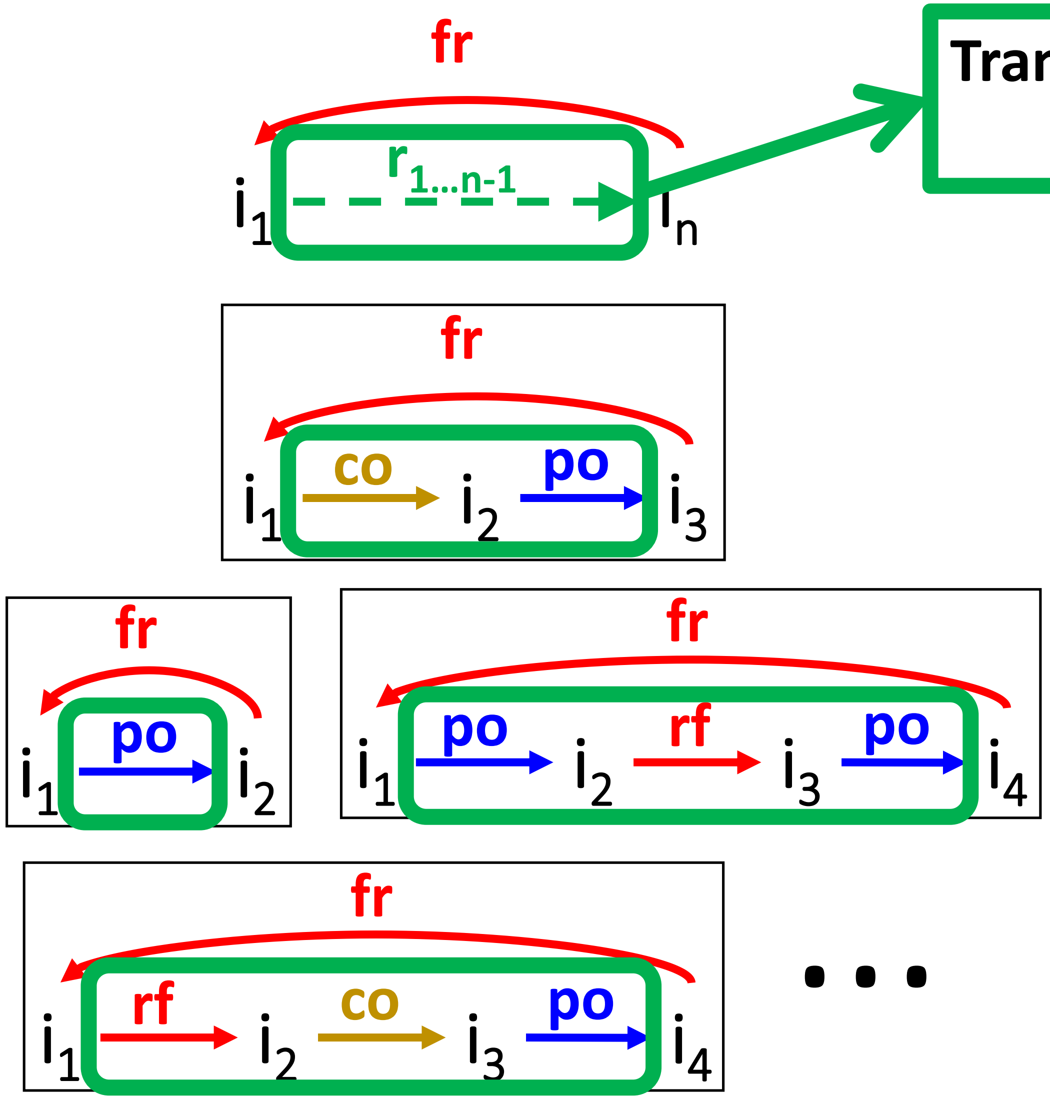
Transitive chain (sequence) of ISA-level edges



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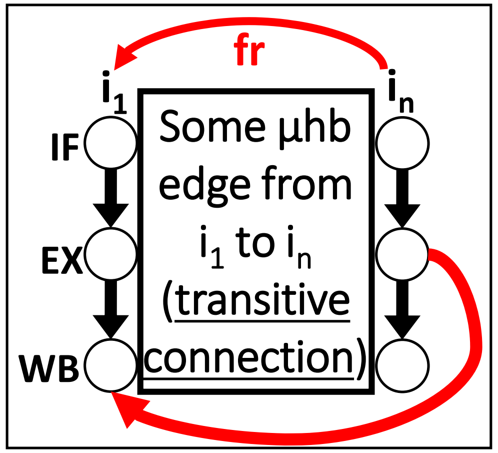
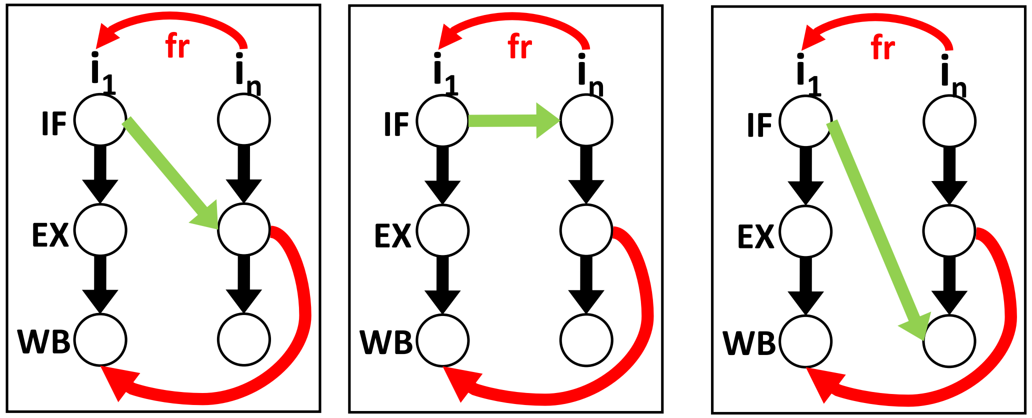
. . .

Using TC Abstraction

$\Longrightarrow$





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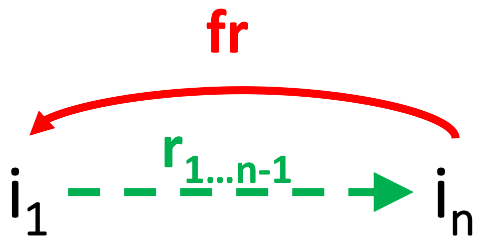

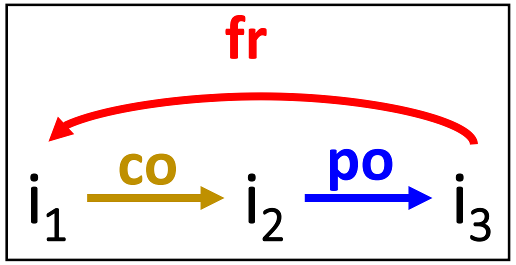

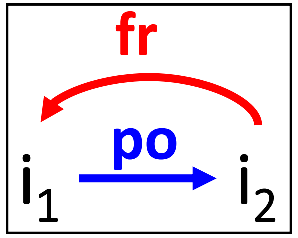

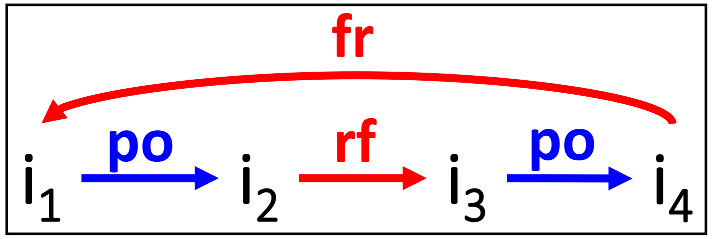

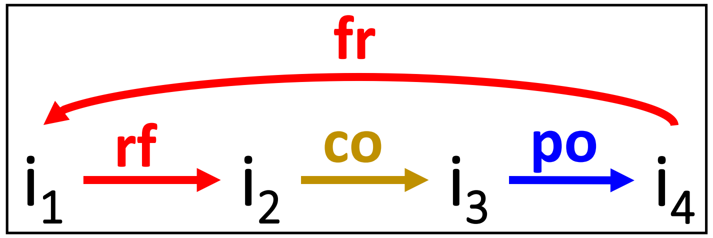

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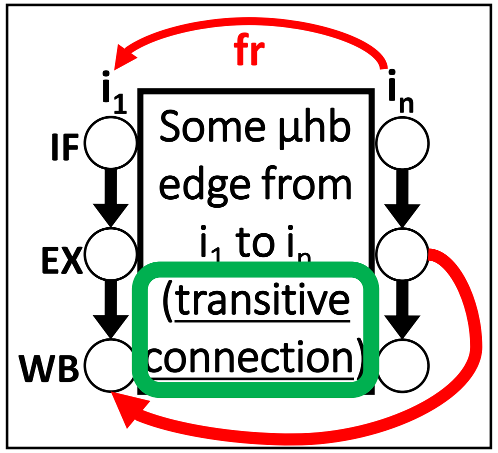

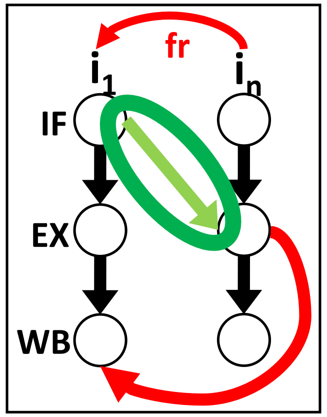

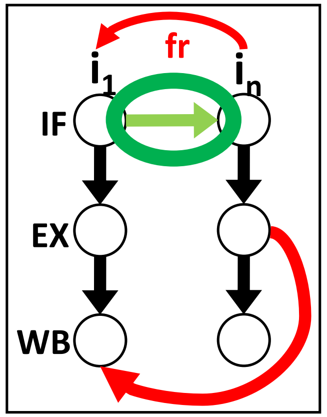

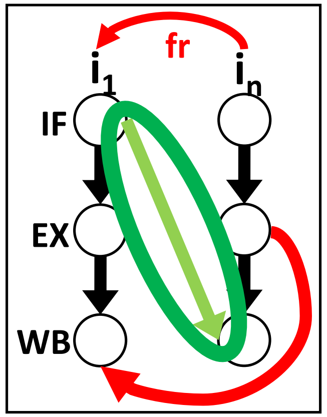

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$$\begin{tikzcd} i_1 \arrow[r, "rf"] & i_2 \arrow[r, "co"] & i_3 \arrow[r, "po"] & i_4 \arrow[lll, bend right, "fr"'] \end{tikzcd}$$

$$\begin{tikzcd} i_1 \arrow[r, "po"] & i_2 \arrow[l, bend right, "fr"'] \end{tikzcd}$$

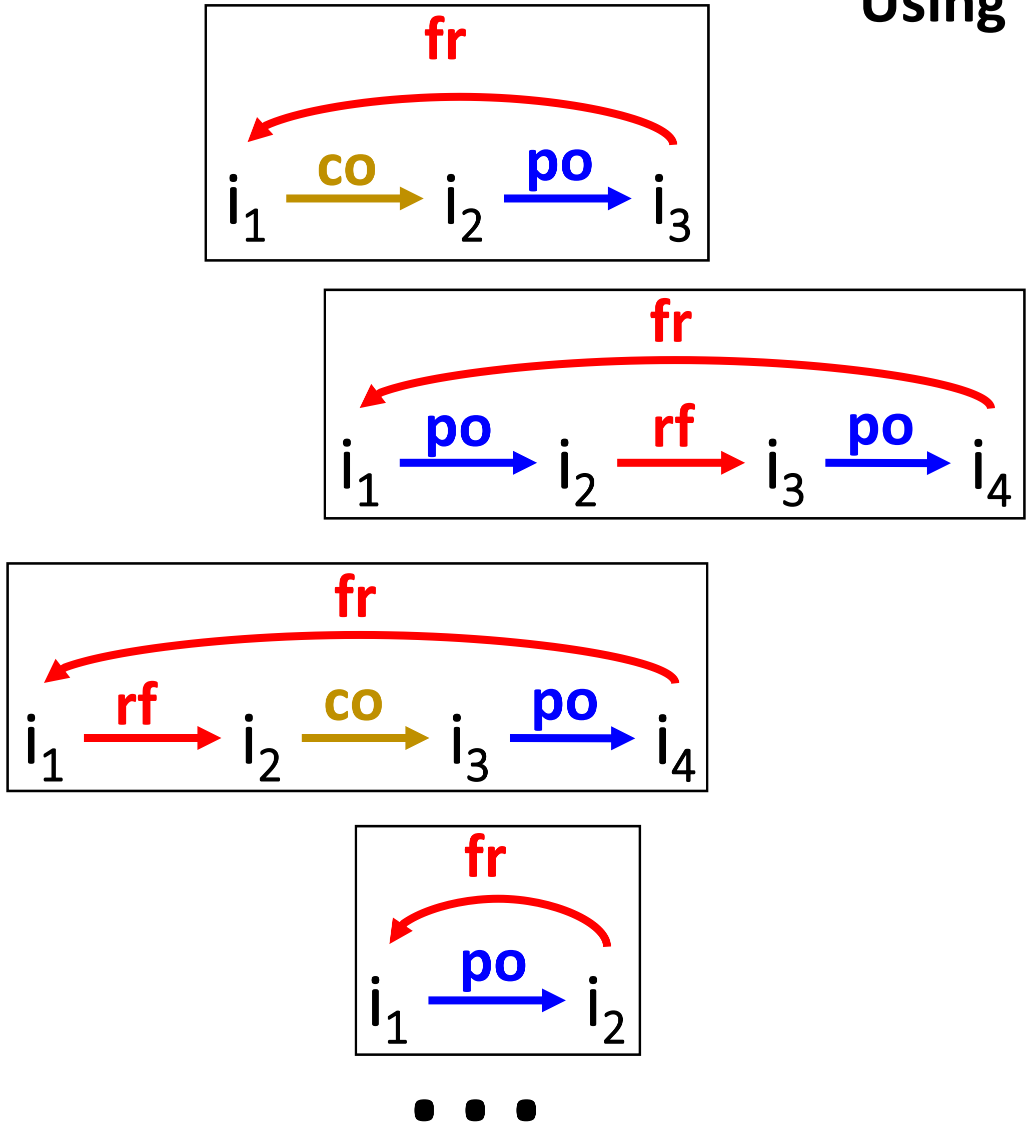
...

$\Longrightarrow$

Using TC Abstraction

The Transitive Chain (TC) Abstraction

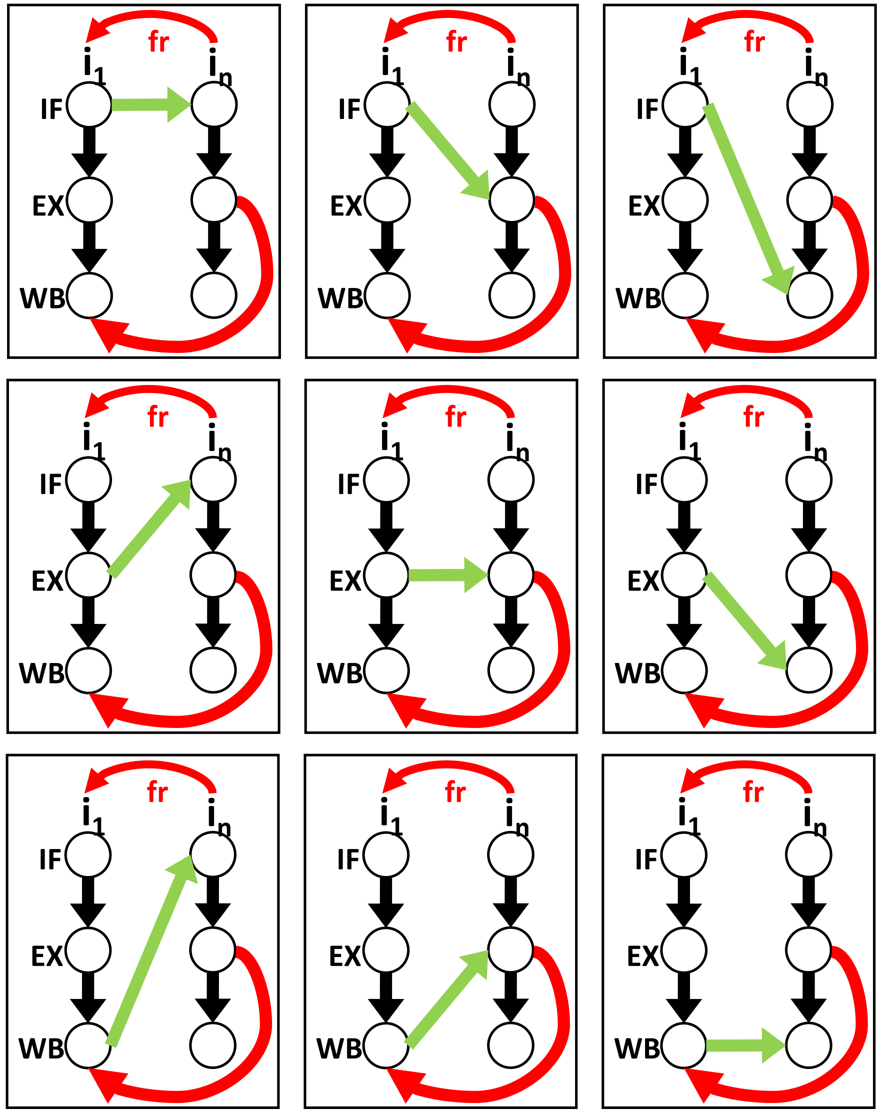
Infinite



$\Longrightarrow$

Using TC Abstraction

Finite!



The Transitive Chain (TC) Abstraction

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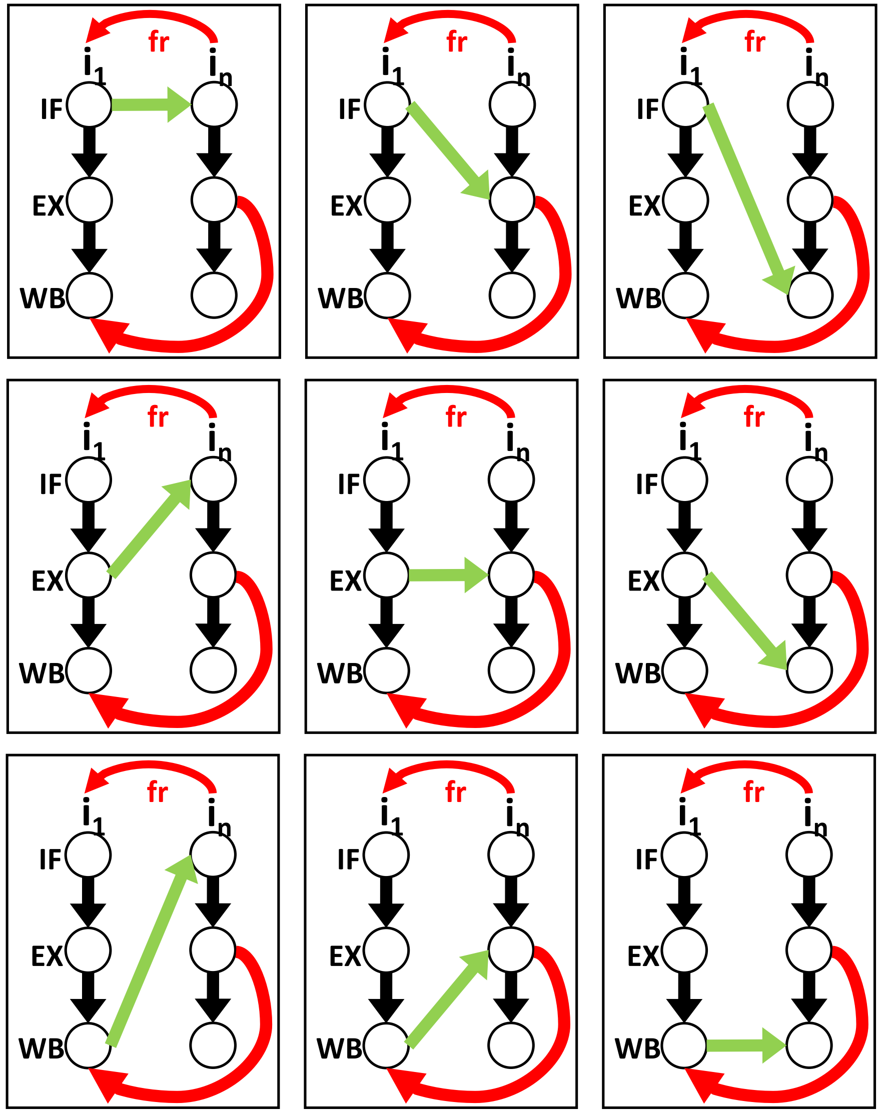
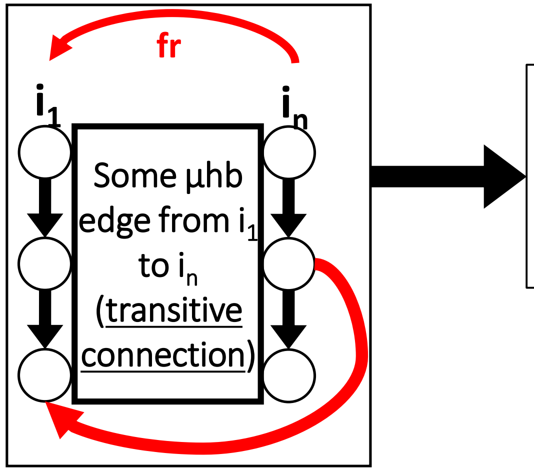


Soundness verified as a supporting proof!

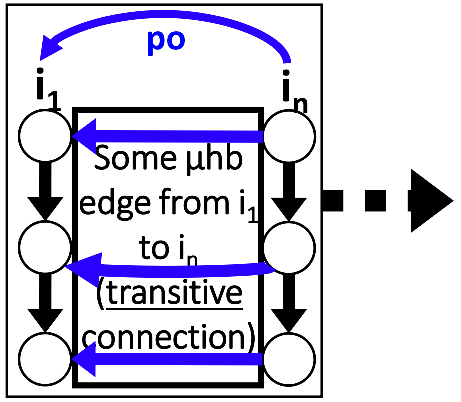
Microarchitectural Correctness Proof

Cycles containing *fr*



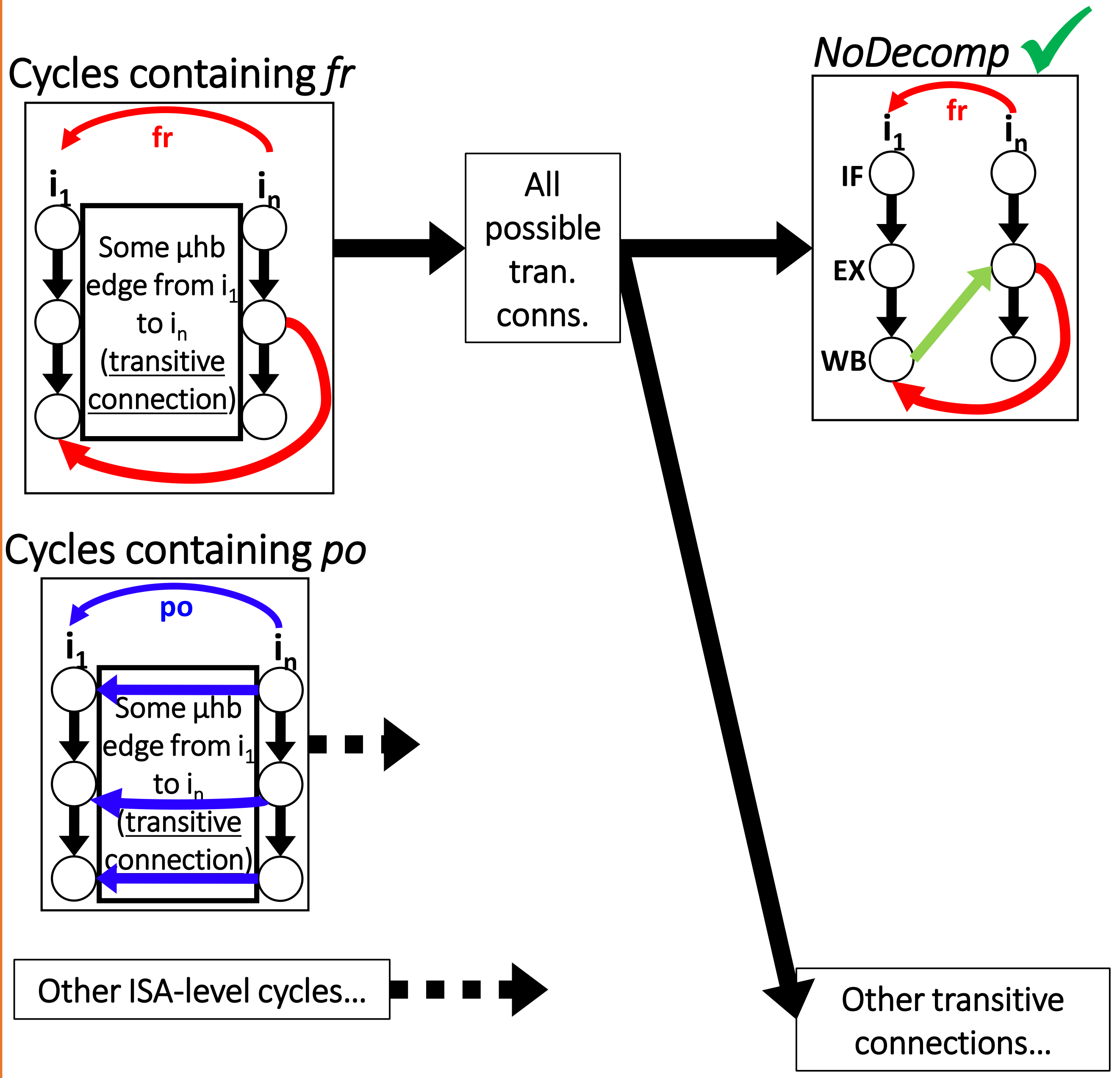
All possible tran. conns.

Cycles containing *po*

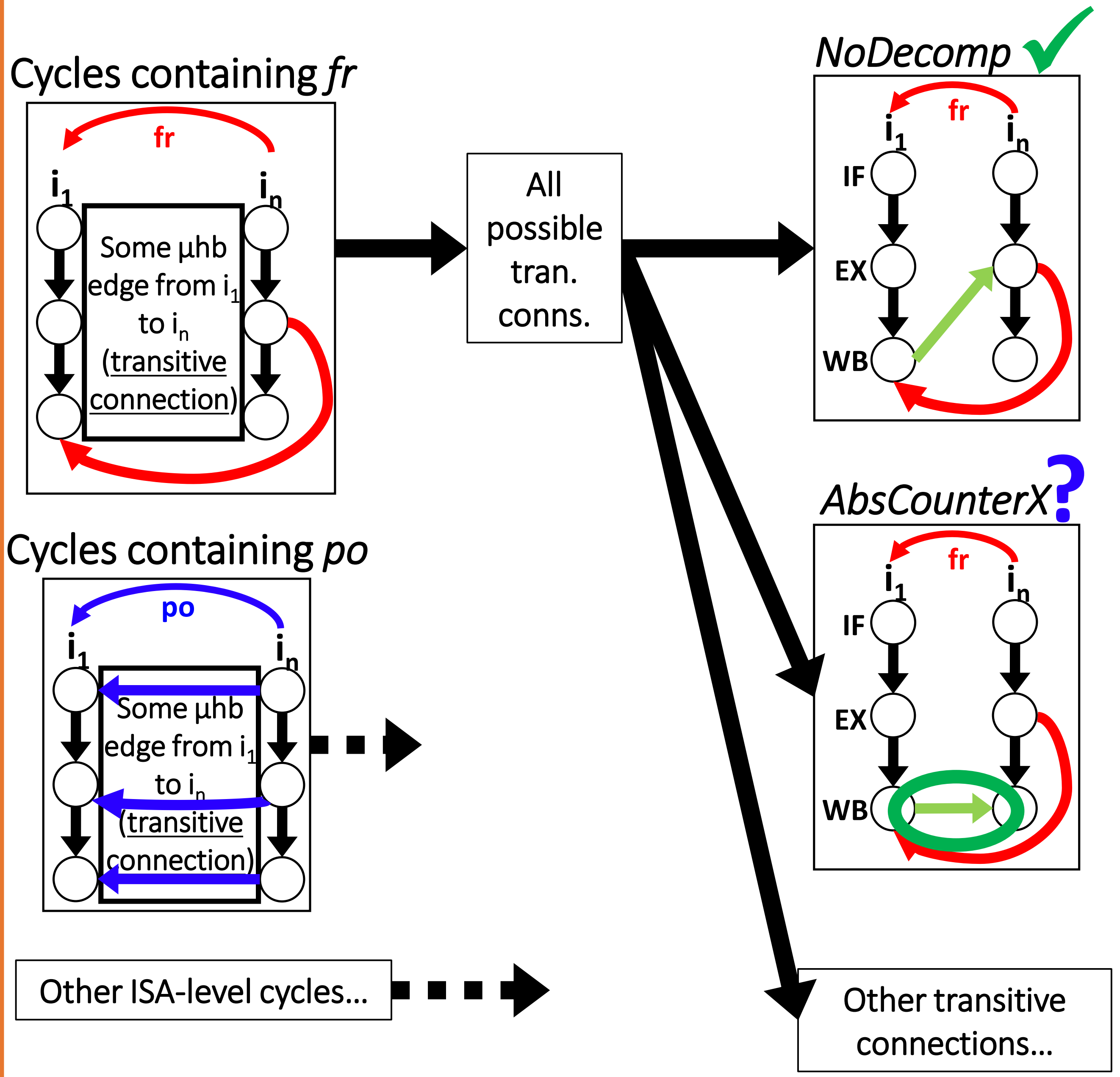


Other ISA-level cycles…

Microarchitectural Correctness Proof

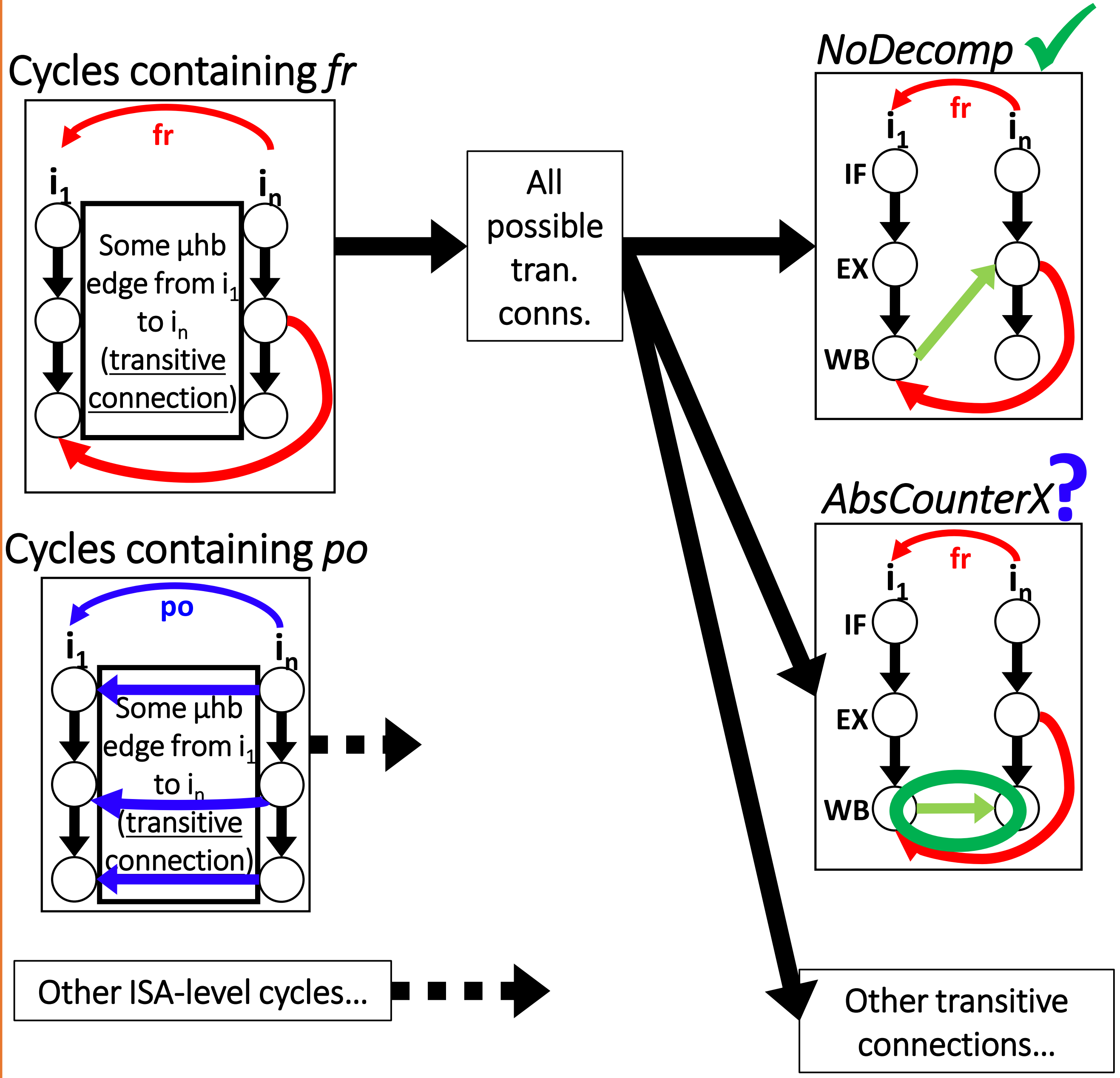

Cycles containing *fr*
fr
i1
in
Some µhb edge from i1 to in (transitive connection)
All possible tran. conns.
NoDecomp ✓
IF
EX
WB
Cycles containing *po*
po
Other ISA-level cycles…
Other transitive connections…

Microarchitectural Correctness Proof



Cycles containing *fr*
fr
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Cycles containing *po*
po
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Other ISA-level cycles...
All possible tran. conns.
NoDecomp ✓
fr
i_1
i_n
IF
EX
WB
AbsCounterX ?
fr
i_1
i_n
IF
EX
WB
Other transitive connections...

Microarchitectural Correctness Proof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All possible tran. conns.
NoDecomp
fr
i1
in
IF
EX
WB
AbsCounterX
fr
i1
in
IF
EX
WB
Other transitive connections...

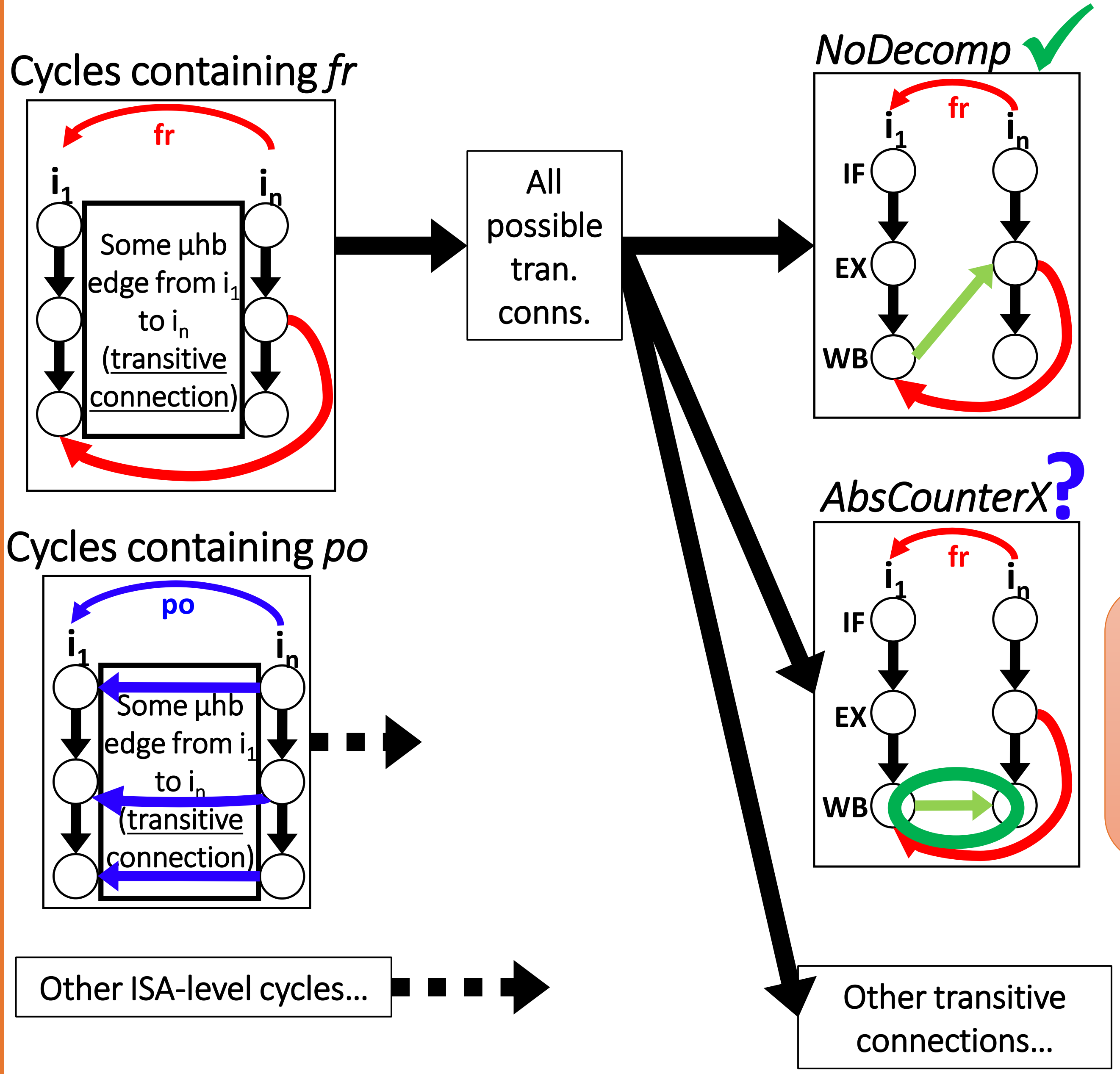
Acyclic graph with

transitive connection =>

Abstract Counterexample

(i.e. possible bug)

Microarchitectural Correctness Proof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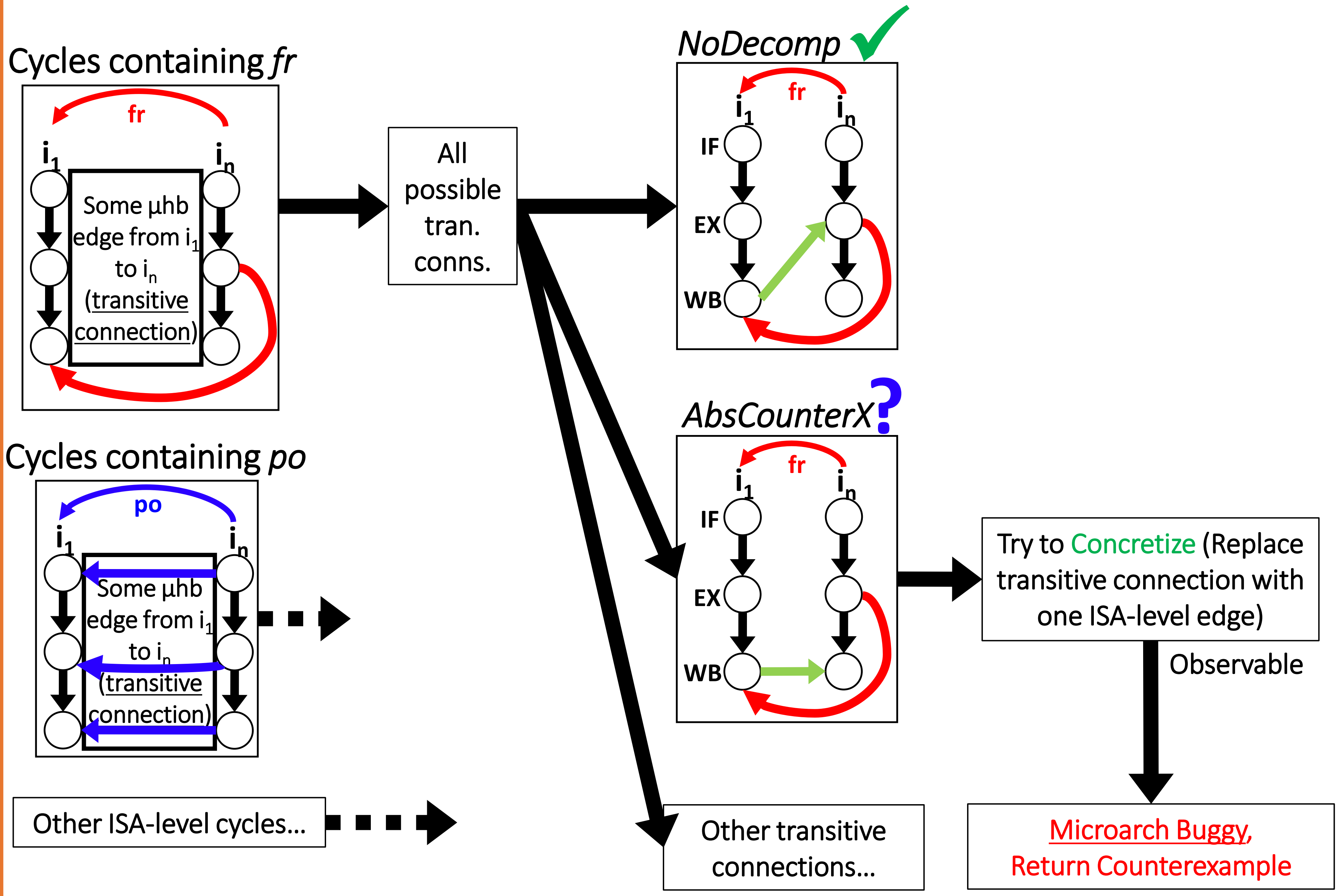
Some μhb edge from i1 to in (transitive connection)
Other ISA-level cycles…
All possible tran. conns.
NoDecomp
fr
i1
in
IF
EX
WB
AbsCounterX
fr
i1
in
IF
EX
WB
Other transitive connections…

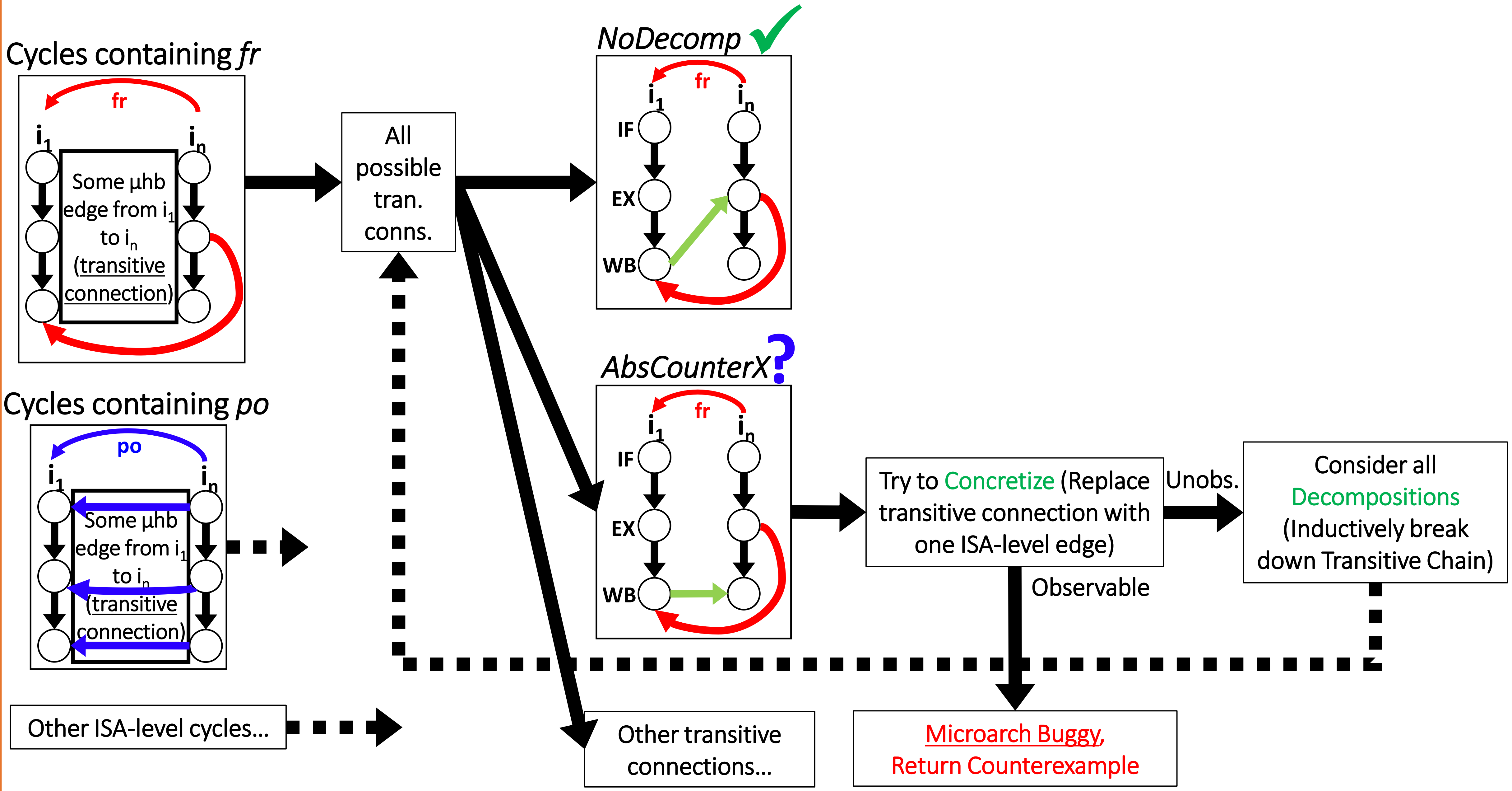
Transitive connection may represent one or multiple ISA-level edges

Microarchitectural Correctness Proof



Cycles containing *fr*
fr
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Cycles containing *po*
po
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Other ISA-level cycles...
All possible tran. conns.
NoDecomp ✓
fr
i_1
i_n
IF
EX
WB
AbsCounterX ?
fr
i_1
i_n
IF
EX
WB
Other transitive connections...
Try to Concretize (Replace transitive connection with one ISA-level edge)
Observable
Microarch Buggy, Return Counterexample

Microarchitectural Correctness Proof


Cycles containing *fr*
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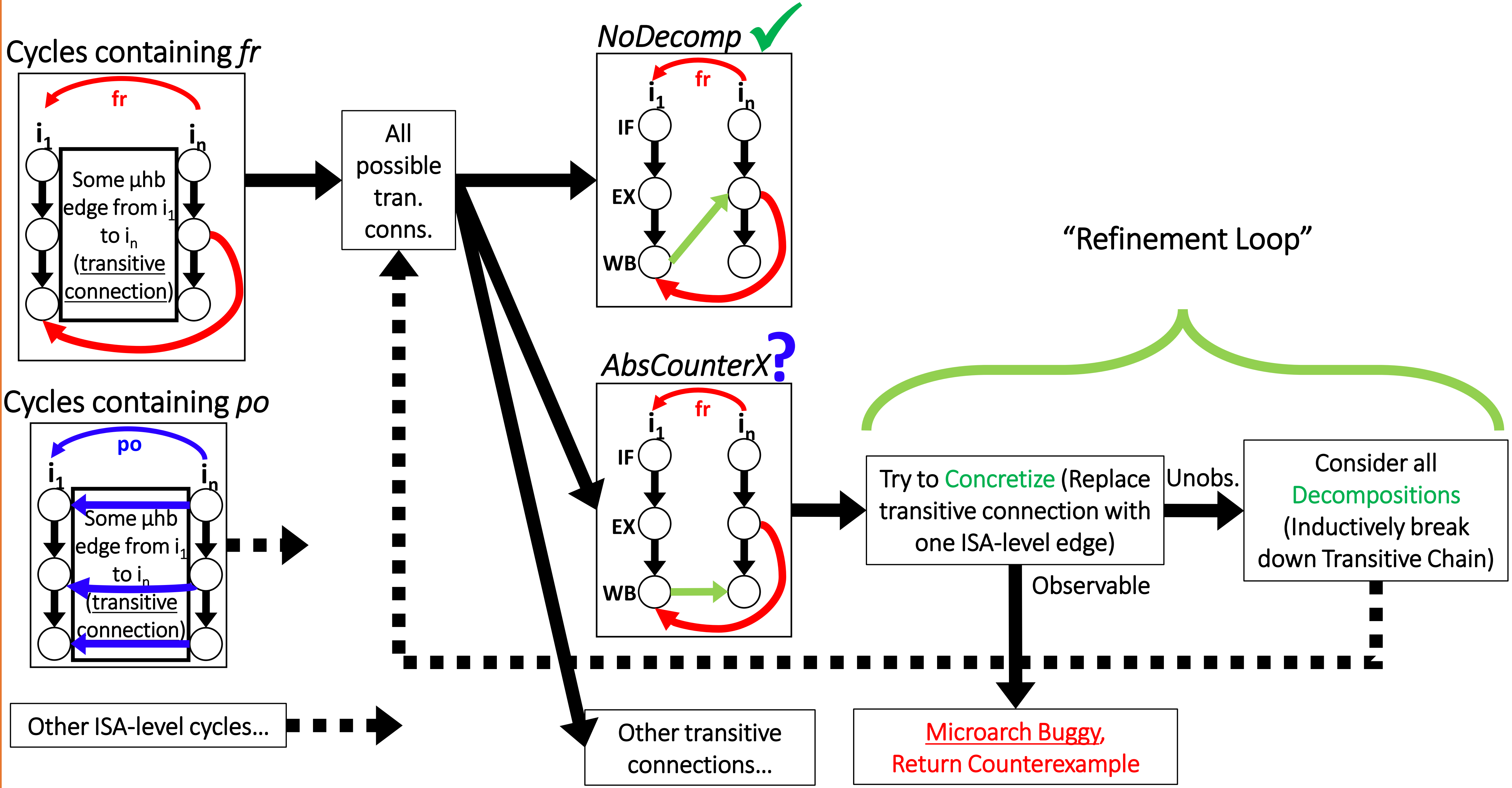
Cycles containing *po*
po
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Other ISA-level cycles…
All possible tran. conns.
NoDecomp
fr
i_1
i_n
IF
EX
WB
AbsCounterX
fr
i_1
i_n
IF
EX
WB
Try to Concretize (Replace transitive connection with one ISA-level edge)
Unobs.
Consider all Decompositions (Inductively break down Transitive Chain)
Observable
Other transitive connections…
Microarch Buggy, Return Counterexample

Microarchitectural Correctness Proof


Cycles containing *fr*
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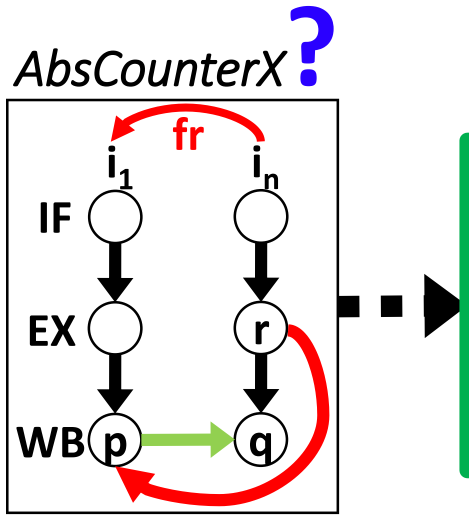
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Cycles containing *po*
po
i_1
i_n
Some μhb edge from i_1 to i_n (transitive connection)
Other ISA-level cycles…
All possible tran. conns.
NoDecomp ✓
fr
i_1
i_n
IF
EX
WB
AbsCounterX?
fr
i_1
i_n
IF
EX
WB
Other transitive connections…
"Refinement Loop"
Try to Concretize (Replace transitive connection with one ISA-level edge)
Unobs.
Consider all Decompositions (Inductively break down Transitive Chain)
Observable
Microarch Buggy, Return Counterexample

Concretization

- All concretizations must be unobservable
- Observable concretizations are counterexamples



Concretization:

Replace transitive connection with single ISA-level edge

Concretization

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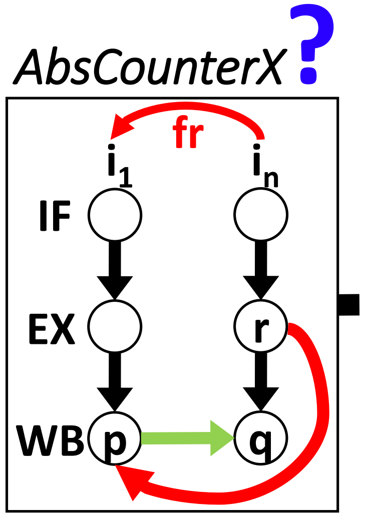
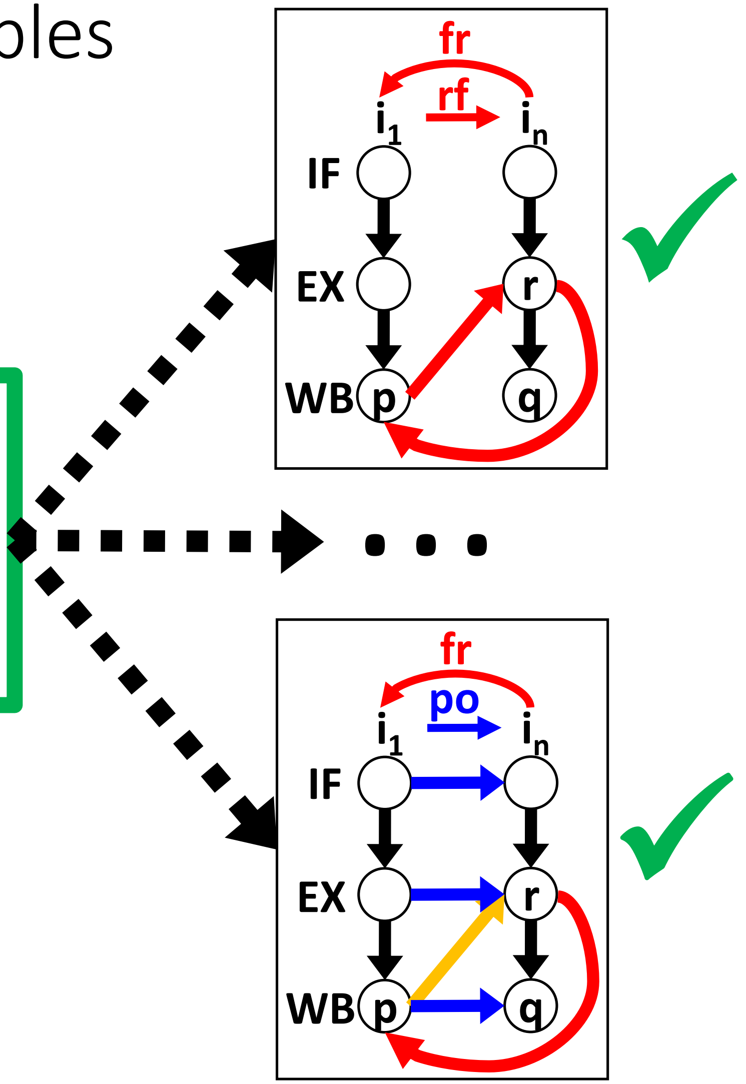


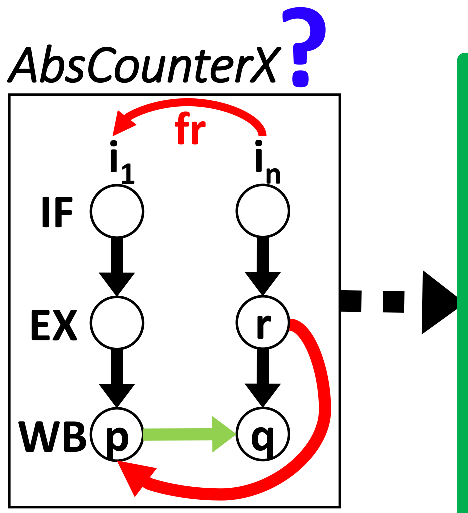
Concretization:

Replace transitive connection with single ISA-level edge



Decomposition

- Additional instruction and ISA-level edge modelled => extra constraints
  - May be enough to make execution unobservable



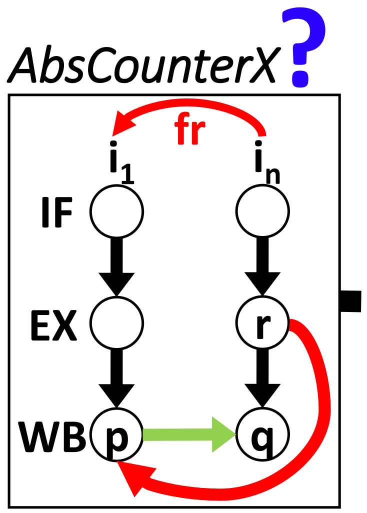
Decomposition:

Inductively break down transitive chain

(Chain of length n == Chain of length n-1 + single “peeled-off” edge)

Decomposition

- Additional instruction and ISA-level edge modelled => extra constraints
  - May be enough to make execution unobservable



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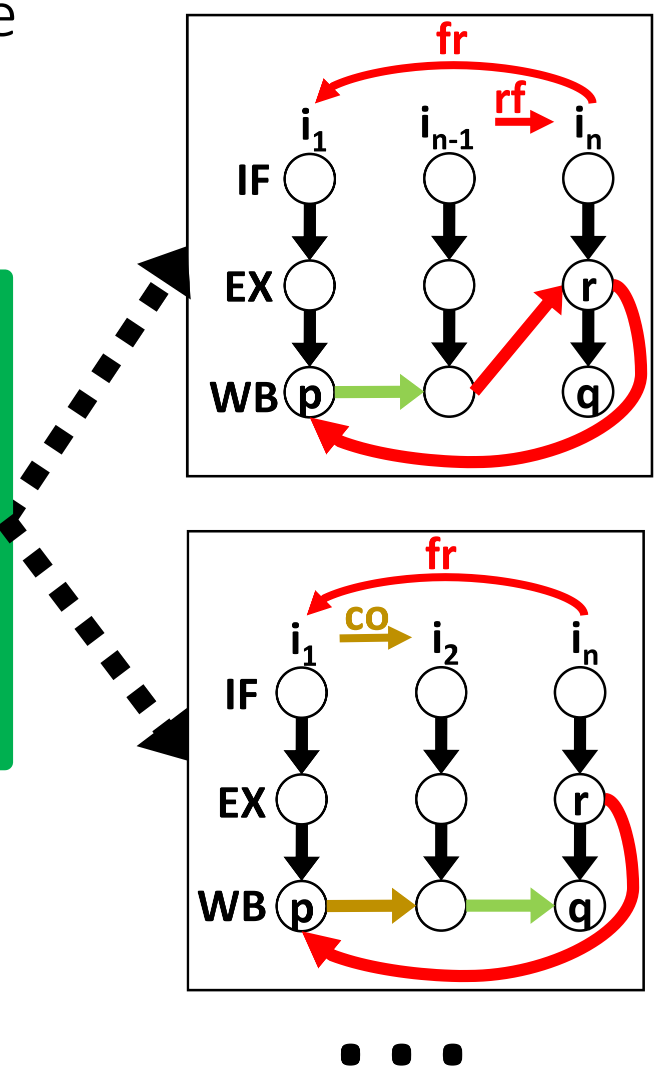

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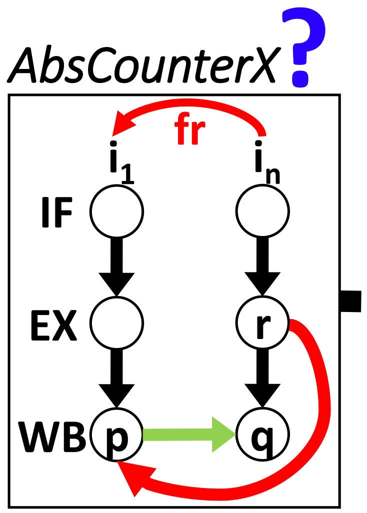

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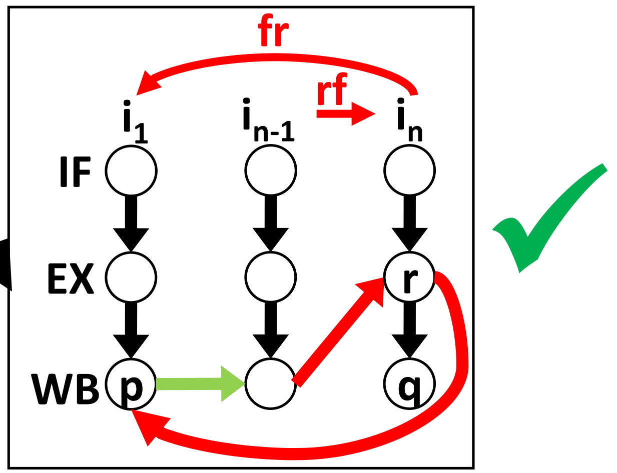

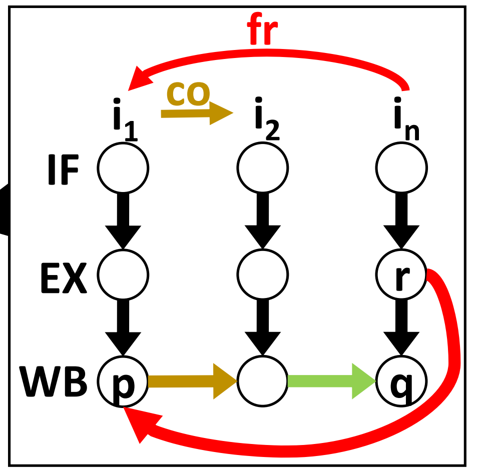

...

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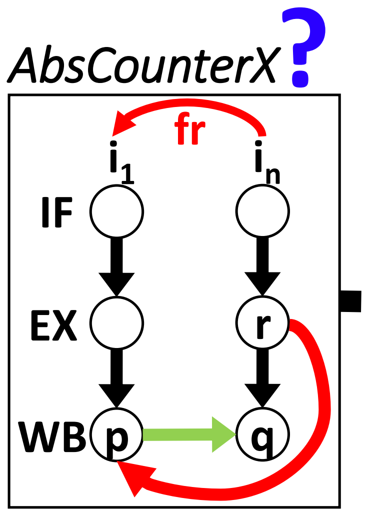

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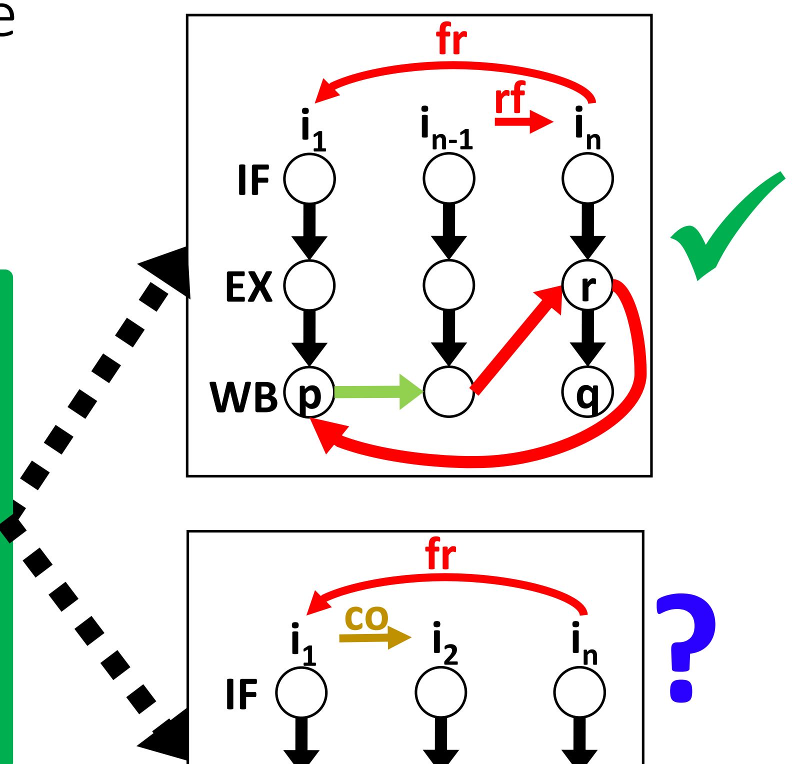

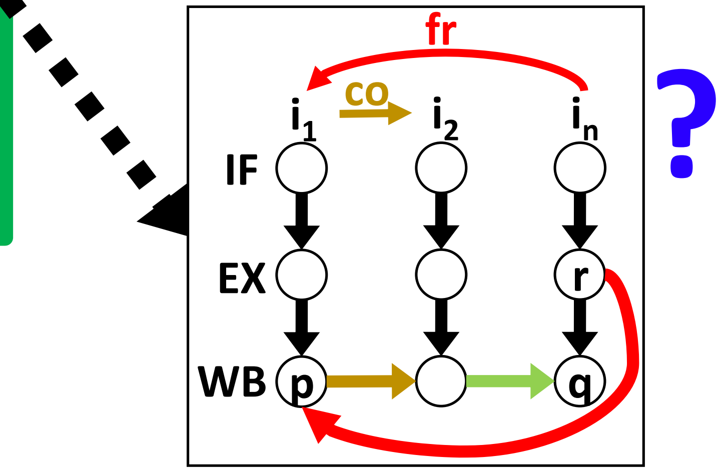

. . .

Decomposition

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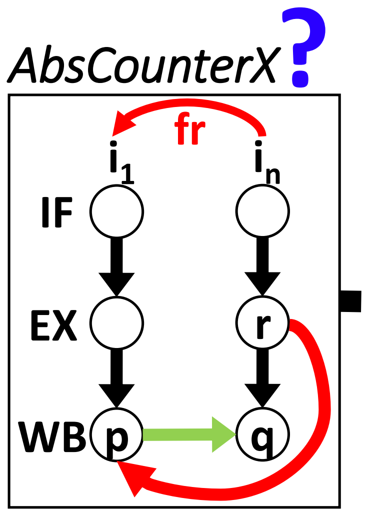

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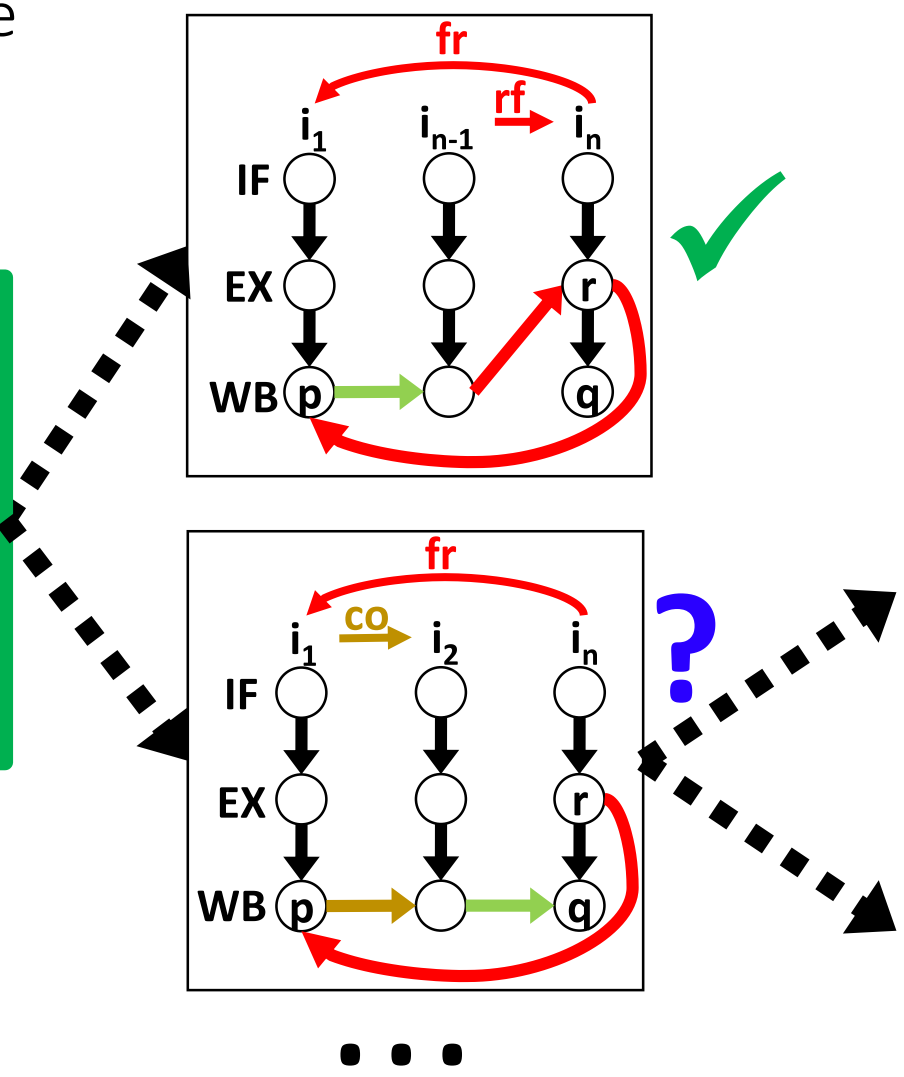
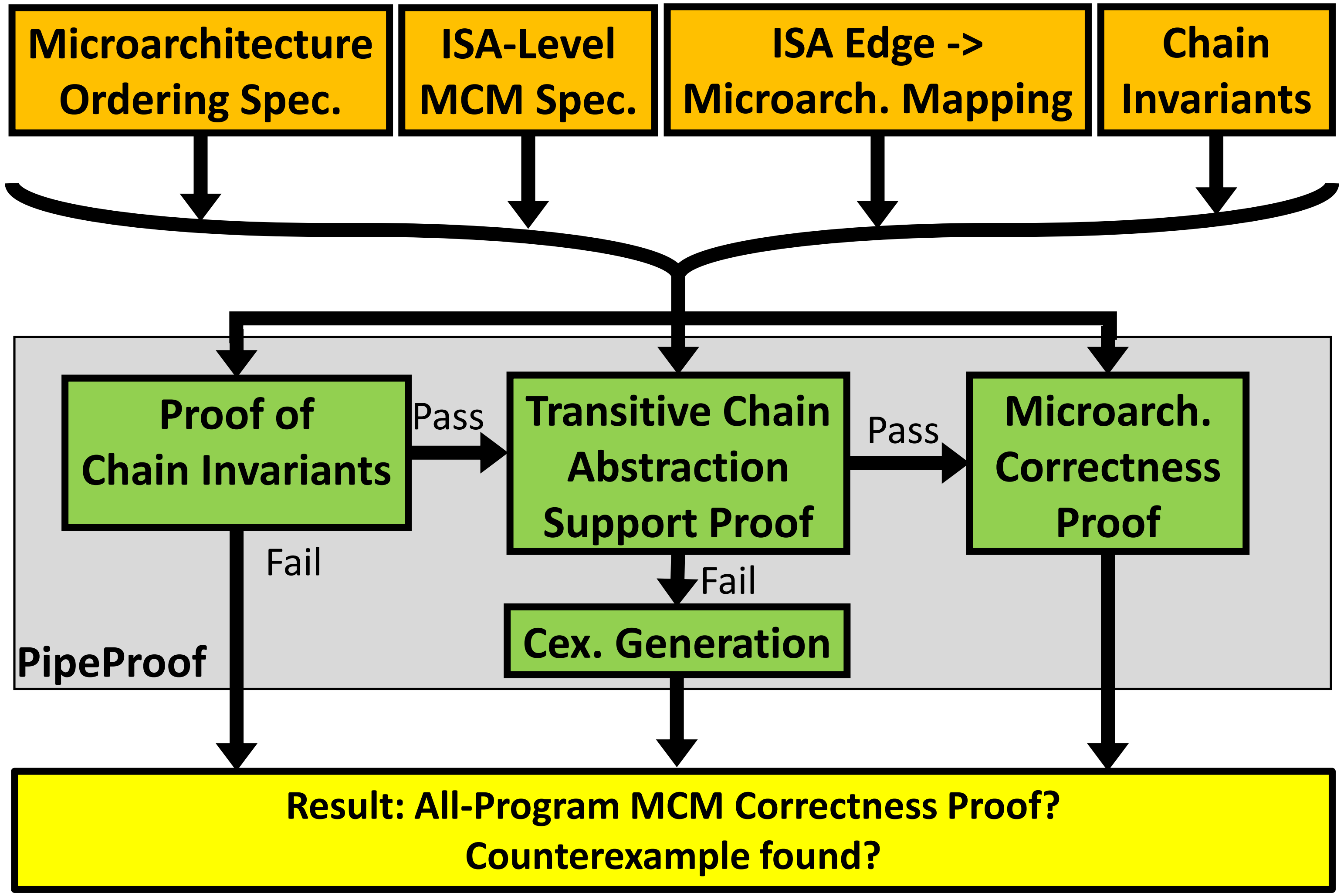


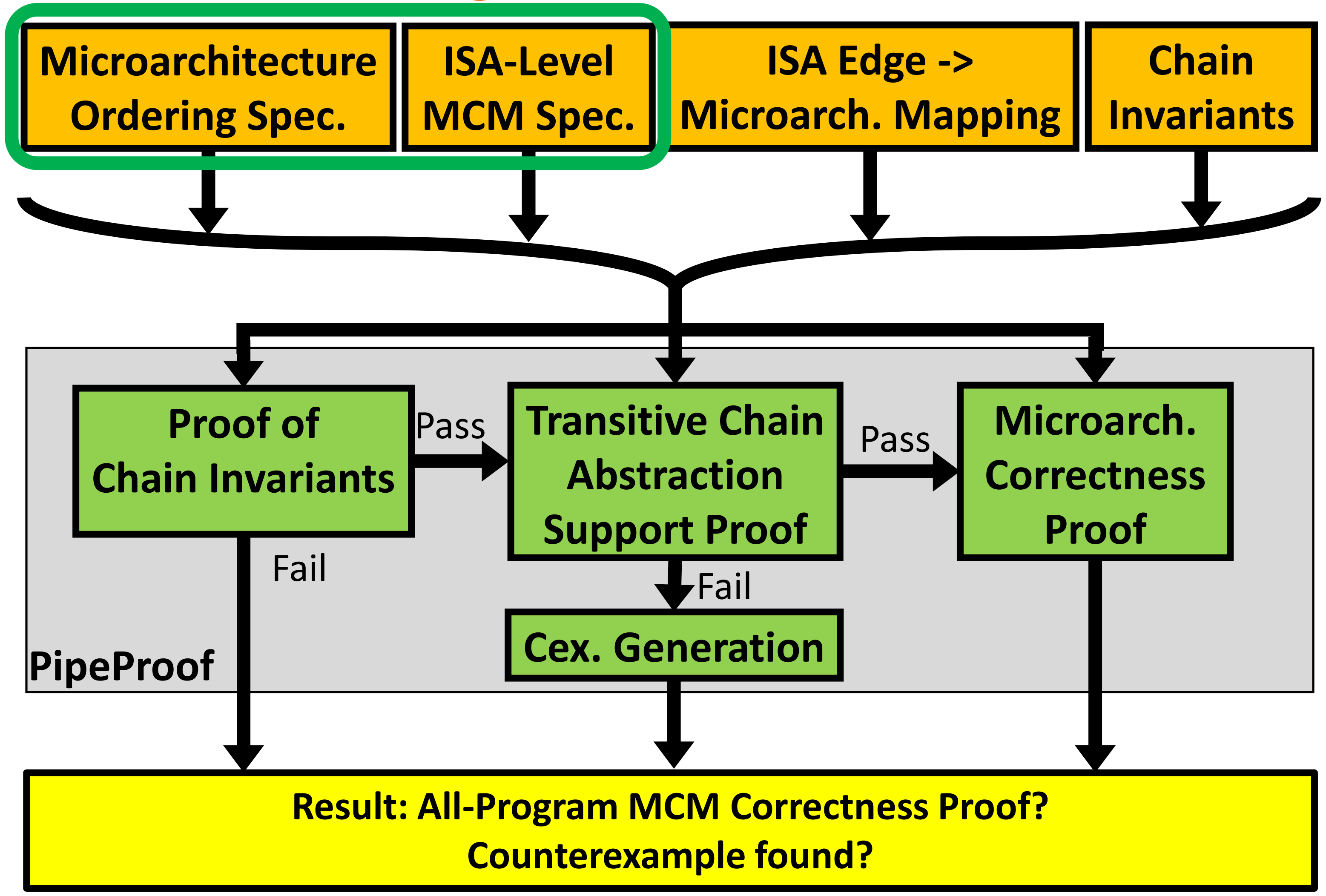
Outline

- Background
  - ISA-level MCM specs
  - Microarchitectural ordering specs
- Microarchitectural Correctness Proof
  - Transitive Chain (TC) Abstraction
- Overall PipeProof Operation
  - TC Abstraction Support Proof
  - Chain Invariants
- Results

PipeProof Block Diagram


Microarchitecture Ordering Spec.
ISA-Level MCM Spec.
ISA Edge -> Microarch. Mapping
Chain Invariants
Proof of Chain Invariants
Pass
Transitive Chain Abstraction Support Proof
Pass
Microarch. Correctness Proof
Fail
Fail
Cex. Generation
PipeProof
Result: All-Program MCM Correctness Proof? Counterexample found?

PipeProof Block Diagram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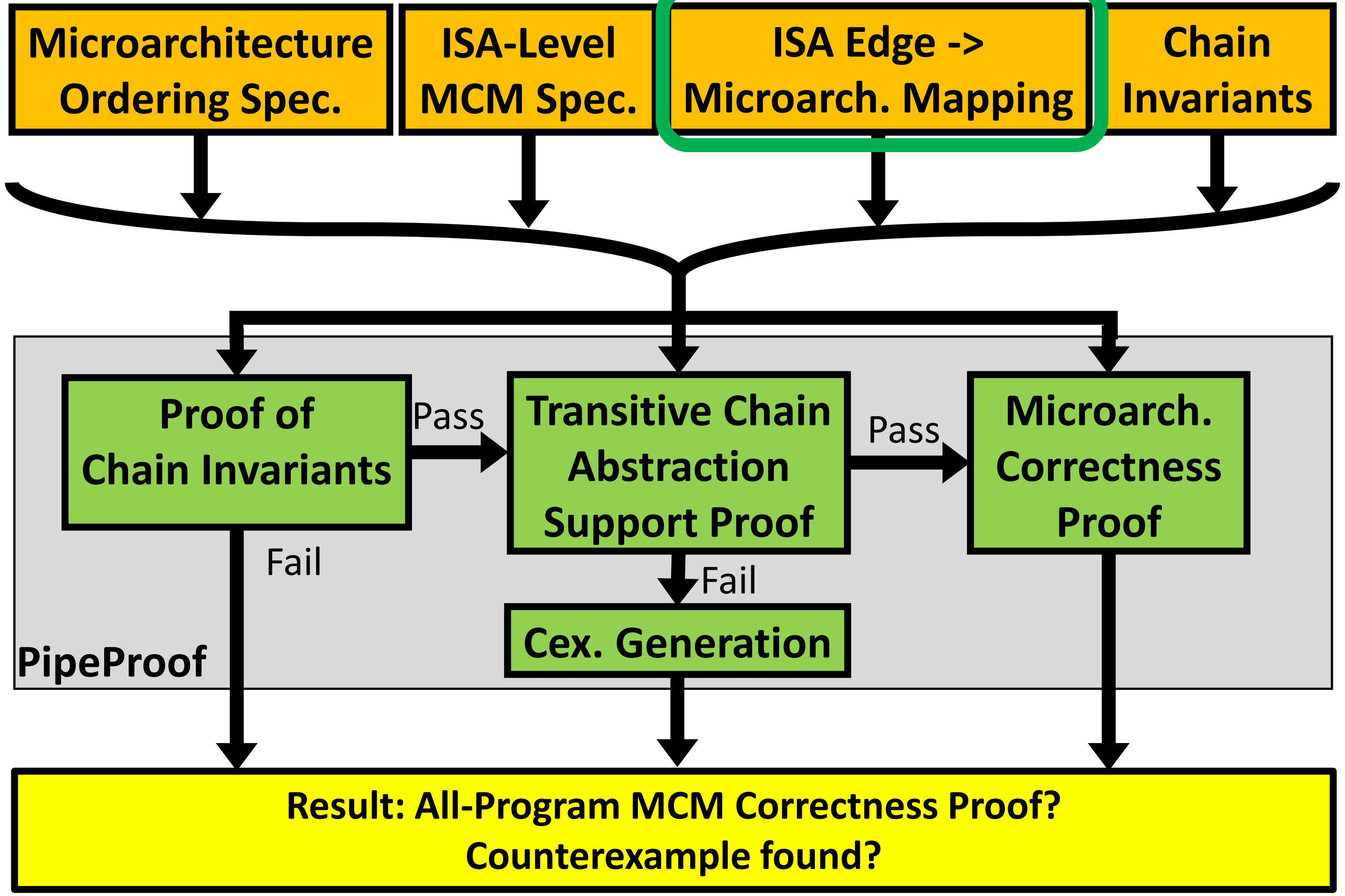
PipeProof Block Diagram

Links ISA-level and µarch executions



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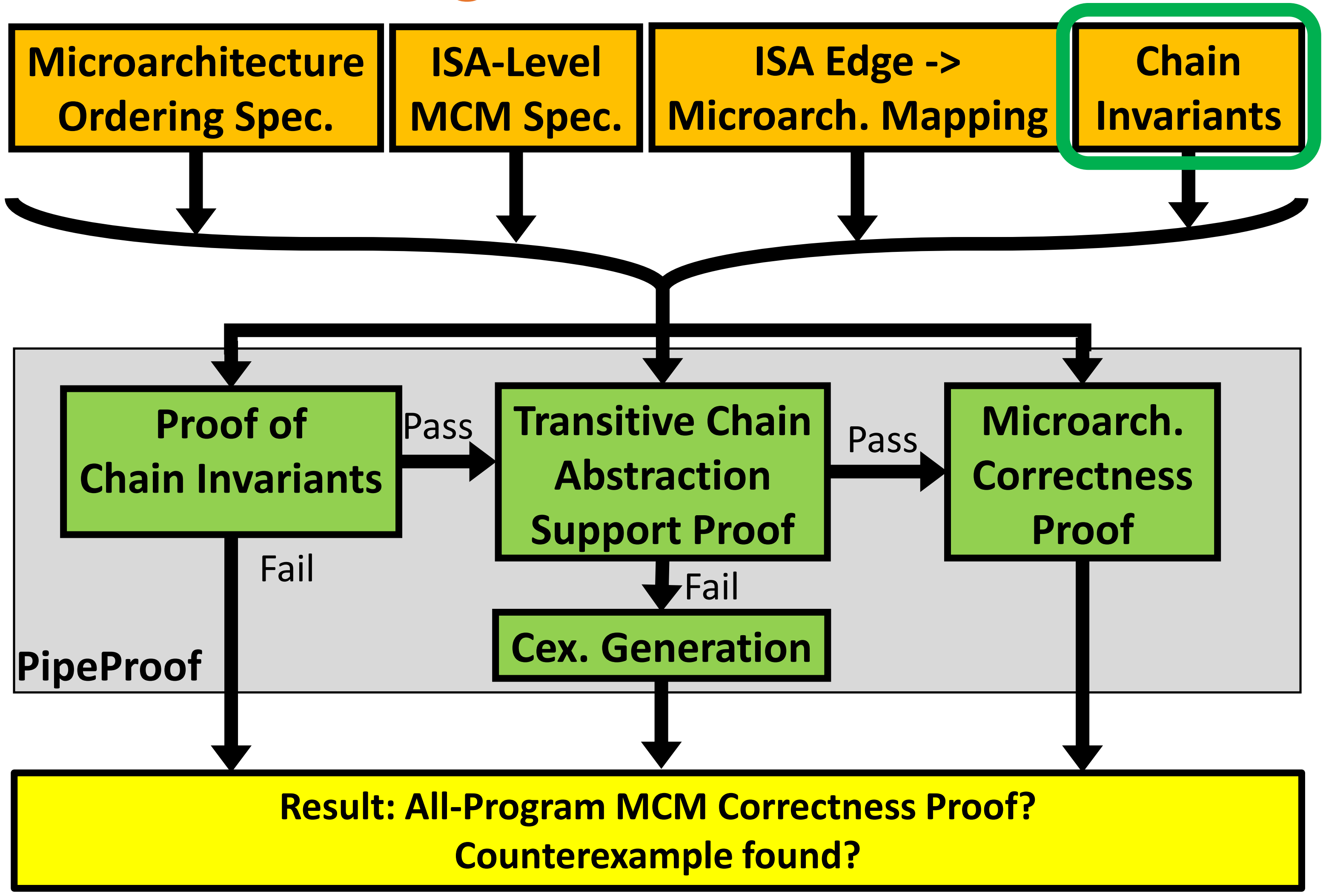
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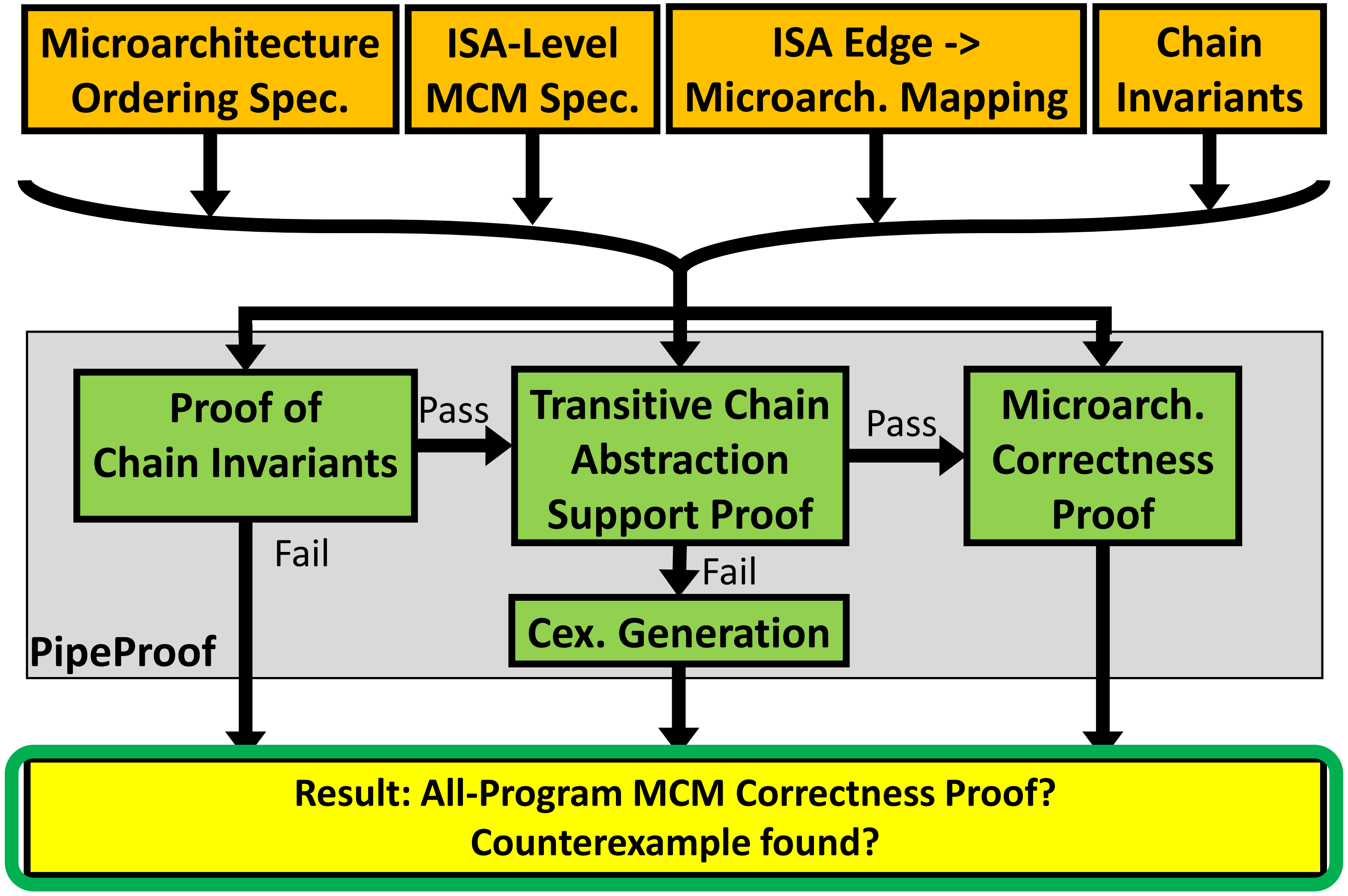
Represent repeated ISA-level patterns

PipeProof Block Diagram



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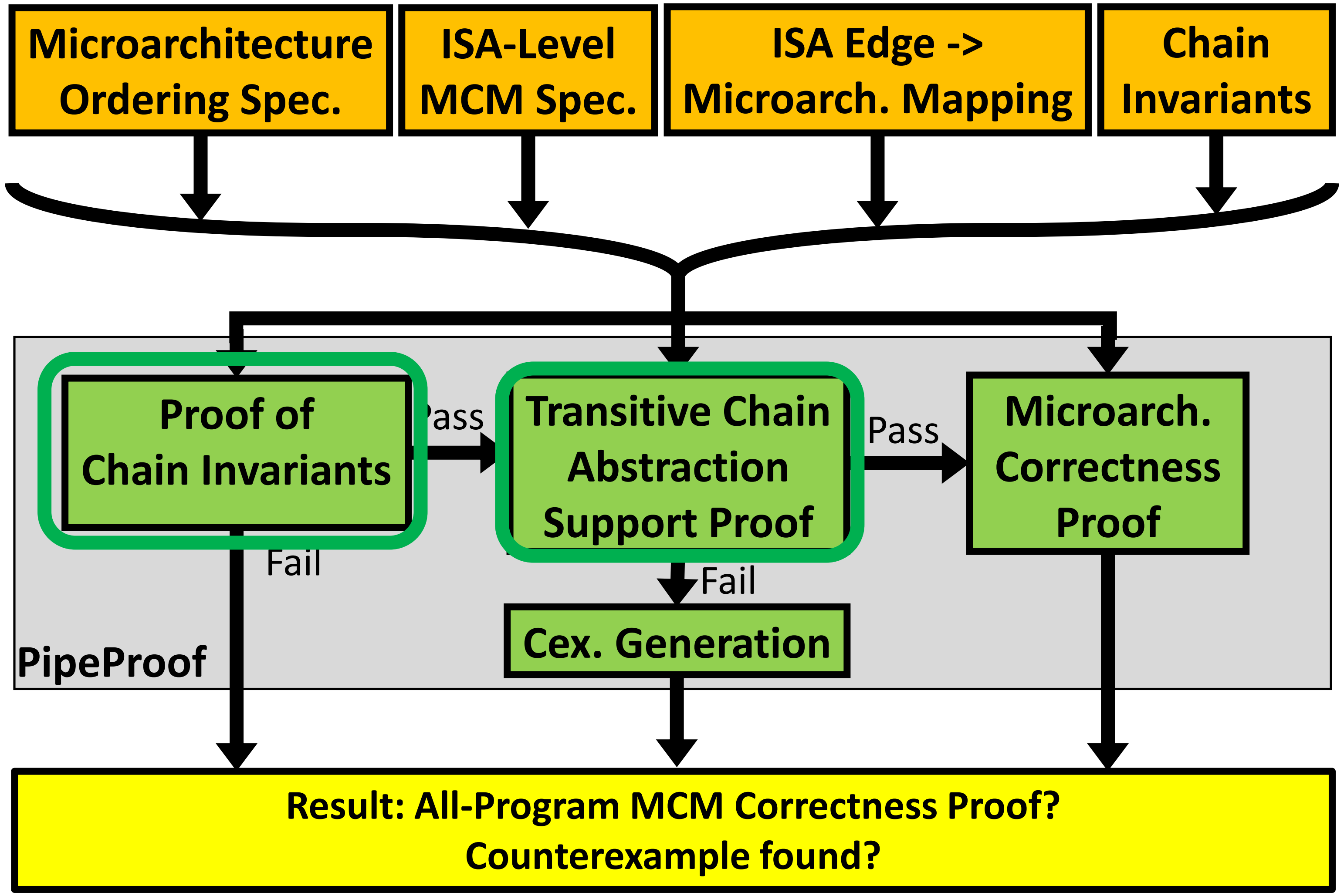
Pass
Microarch. Correctness Proof
Fail
Fail
Cex. Generation
PipeProof
Result: All-Program MCM Correctness Proof? Counterexample found?

If design can’t be verified, a counterexample (a forbidden execution that is observable) is often returned

PipeProof Block Diagram



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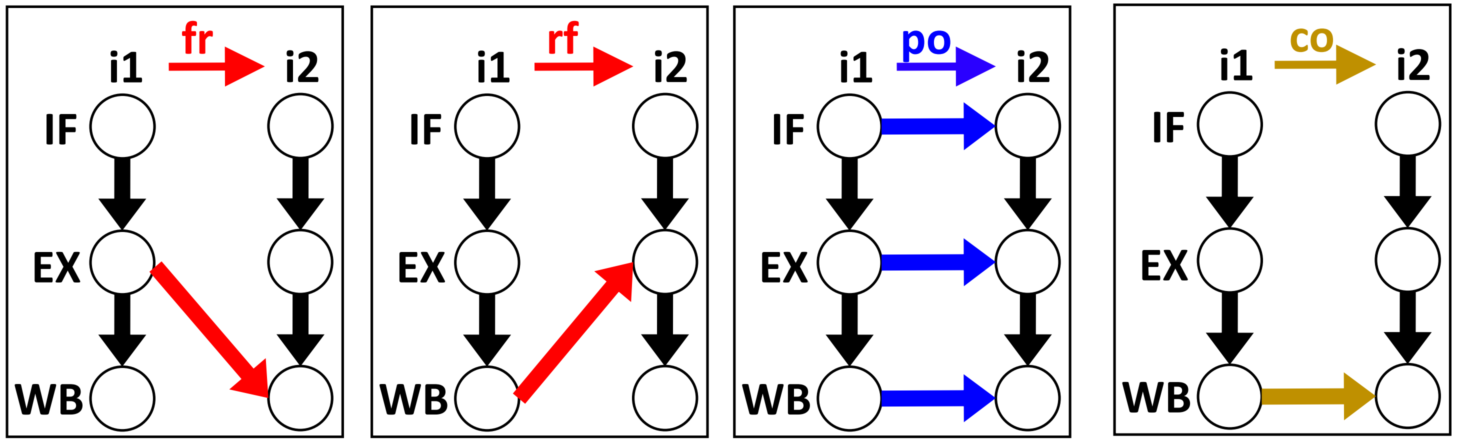
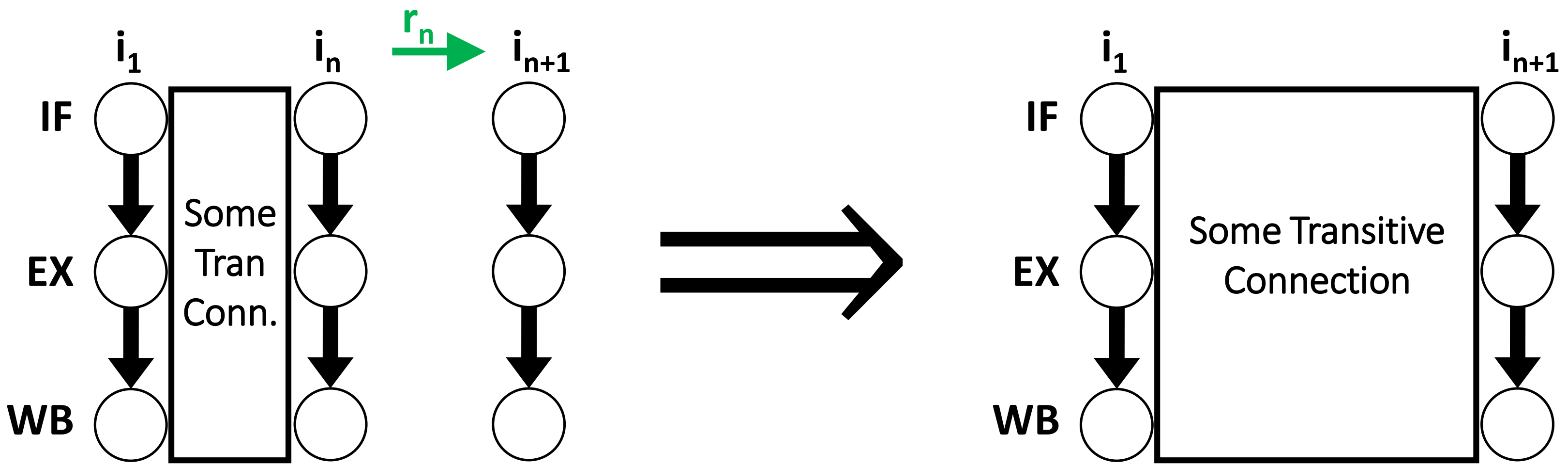
Supporting proofs provide foundation for correctness proof

Transitive Chain (TC) Abstraction Support Proof

- Ensure that ISA-level pattern and µarch. support TC Abstraction
- Base case: Do initial ISA-level edges guarantee connection?



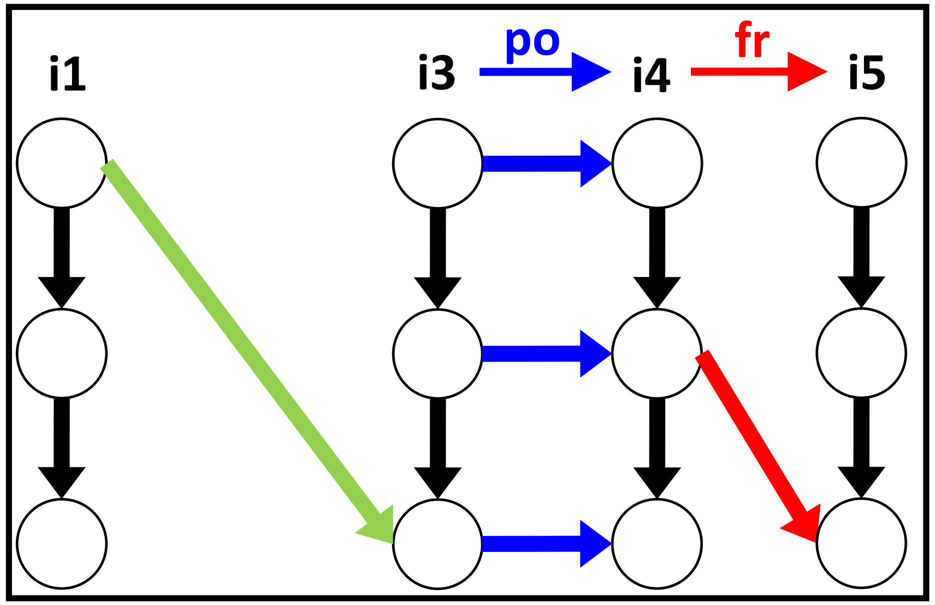
- Inductive case: Extend transitive chain => extend transitive connection?



Chain Invariants

- Abstractly represent repeated ISA-level patterns
- Sometimes needed for refinement loop to terminate
- Inductively proven by PipeProof before their use in proof algorithms
- <u>Example:</u> checking for edge from i1 to i5 (TC abstraction support proof)

Abstract Counterexample



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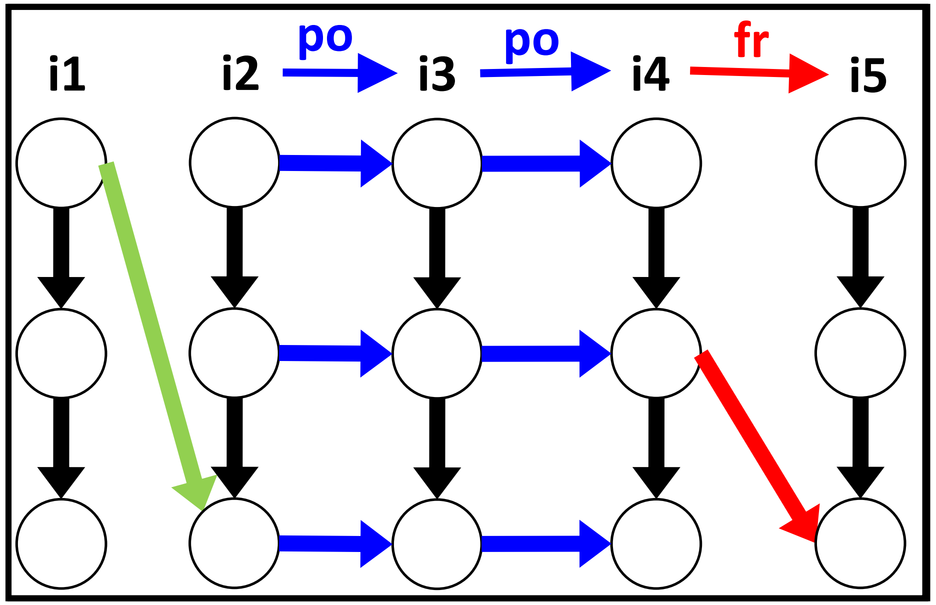
Repeating ISA-Level Pattern



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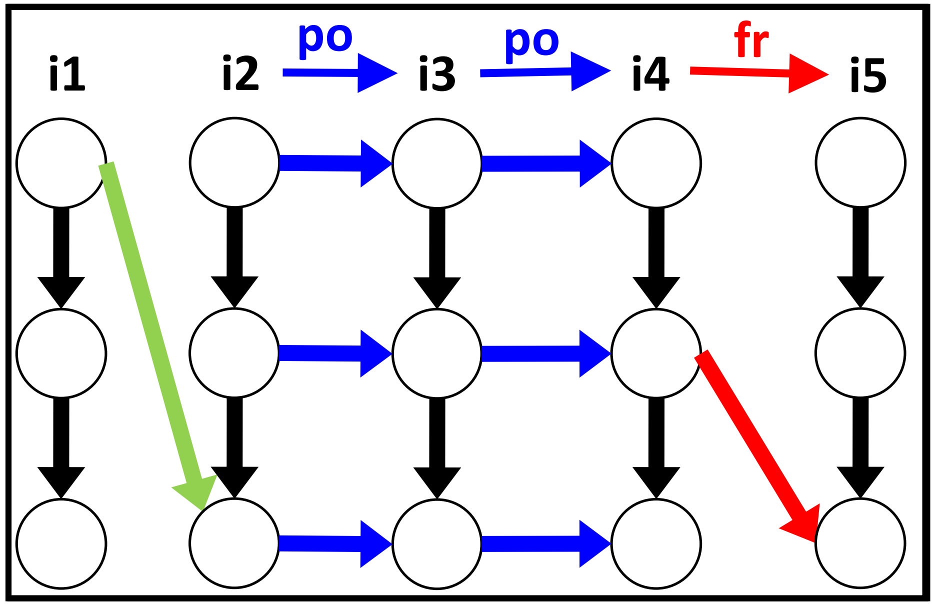

Can continue decomposing in this way forever!

Chain Invariants

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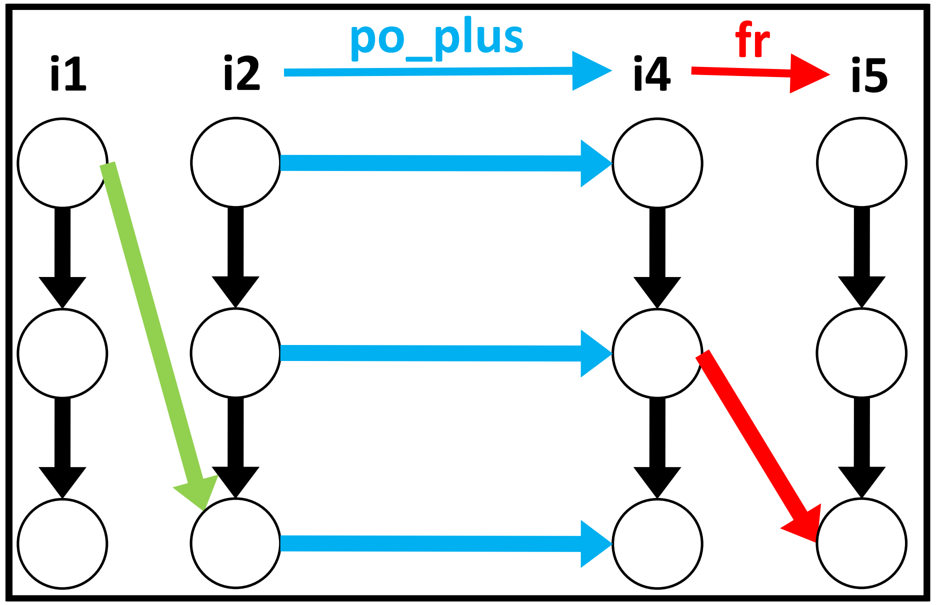
- Inductively proven by PipeProof before their use in proof algorithms
- **Example:** checking for edge from i1 to i5 (TC abstraction support proof)

Chain Invariant Applied



-**po_plus** = arbitrary number of repetitions of **po**
-Next edge peeled off will be something other than **po**

In the paper…

- Optimizations
  - Covering Sets: Eliminate redundant transitive connections
  - Memoization: Eliminate redundant ISA-level cycles
- Inductive ISA edge generation
- Adequate Model Over-Approximation
  - Needed to ensure soundness of PipeProof's abstraction-based approach
- …and more!

Results

- Ran PipeProof on simpleSC (SC) and simpleTSO (TSO) µarches
  - 3-stage in-order pipelines
- Proved correctness of both microarchitectures for all programs
  - With optimizations, runtimes < 1 hour!

	simpleSC	**simpleSC (w/ Covering Sets + Memoization)**
Total Time	**225.9 sec**	**19.1 sec**

	simpleTSO	**simpleTSO (w/ Covering Sets + Memoization)**
Total Time	**Timeout**	**2449.7 sec (≈ 41 mins)**

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Total Time	**Timeout**	**2449.7 sec (≈ 41 mins)**

Results

- Ran PipeProof on simpleSC (SC) and simpleTSO (TSO) µarches
  - 3-stage in-order pipelines
- Proved correctness of both microarchitectures for all programs
  - With optimizations, runtimes < 1 hour!

	simpleSC	**simpleSC (w/ Covering Sets + Memoization)**
Total Time	**225.9 sec**	**19.1 sec**

	simpleTSO	**simpleTSO (w/ Covering Sets + Memoization)**
Total Time	**Timeout**	**2449.7 sec (≈ 41 mins)**

Conclusions

- **PipeProof:** Automated ***All-Program*** Microarchitectural MCM Verification
  - Designers no longer need to choose between completeness and automation
- **Transitive Chain Abstraction** allows inductive modelling and verification of the infinite set of all possible executions
  - Abstraction is automatically refined as necessary to prove correctness
- Verified simple microarchitectures implementing SC and TSO in < 1 hour!

Code available at
https://github.com/ymanerka/pipeproof

[Image: Napish]

PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications

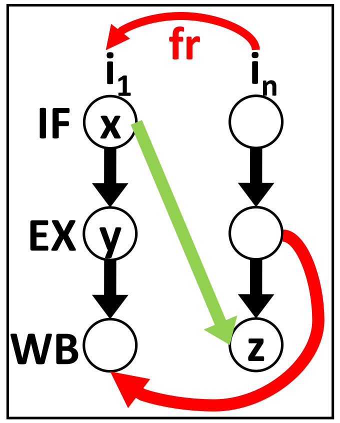
Yatin A. Manerkar, Daniel Lustig*,
Margaret Martonosi, and Aarti Gupta

Code available at
https://github.com/ymanerka/pipeproof

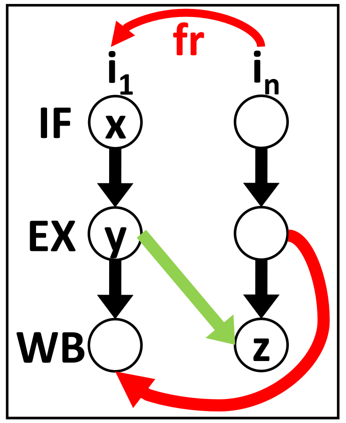
Covering Sets Optimization

- Must verify across all possible transitive connections
- Each decomposition creates a new set of transitive connections
  - Can quickly lead to a case explosion
- The Covering Sets Optimization eliminates redundant transitive connections

A



B



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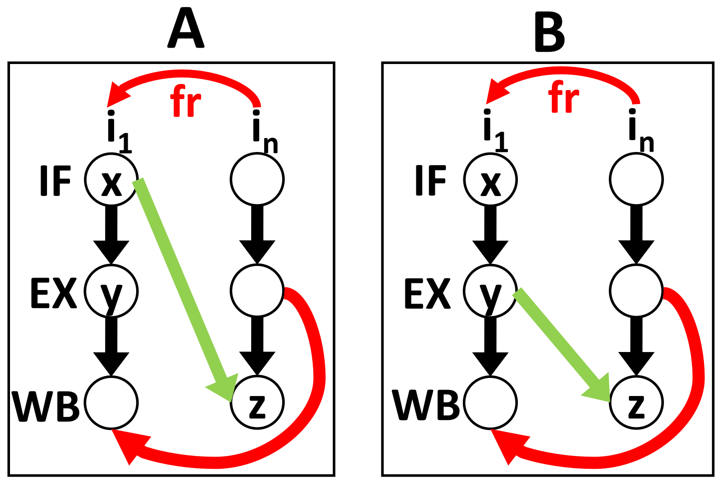

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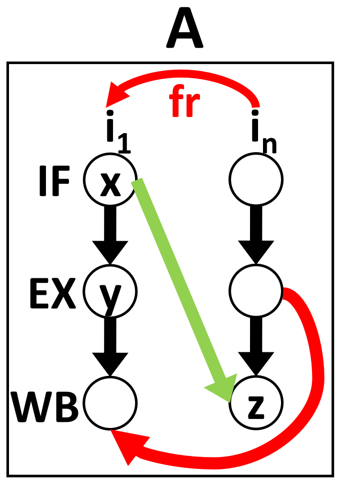

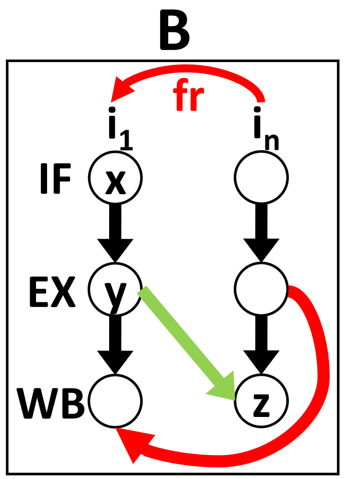

Graph B has edges from y→z (tran conn.) and x→z (by transitivity)

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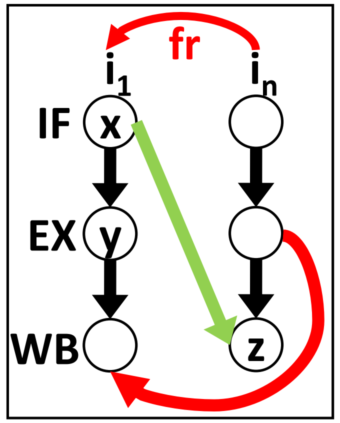

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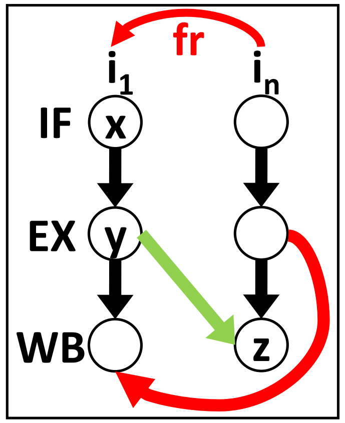
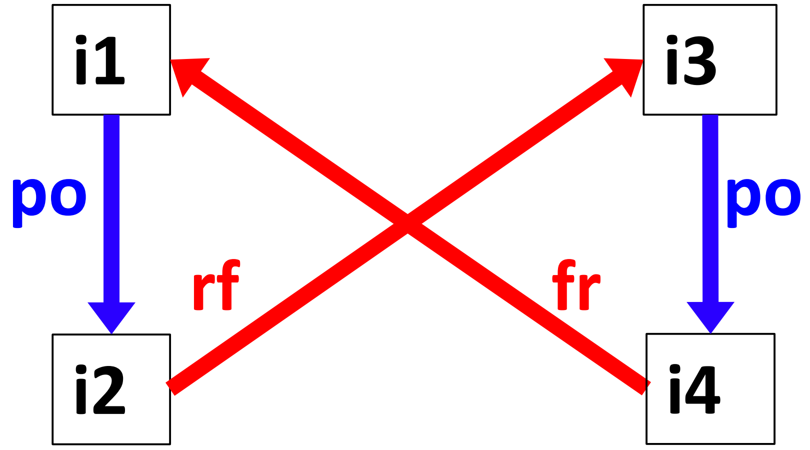


Graph B has edges from y→z (tran conn.) and x→z (by transitivity)

Correctness of A => Correctness of B (since B contains A's tran conn.)
Checking B explicitly is redundant!

Memoization Optimization

- Base PipeProof algorithm examines some cycles multiple times
- Memoization eliminates redundant checks of cycles that have already been verified



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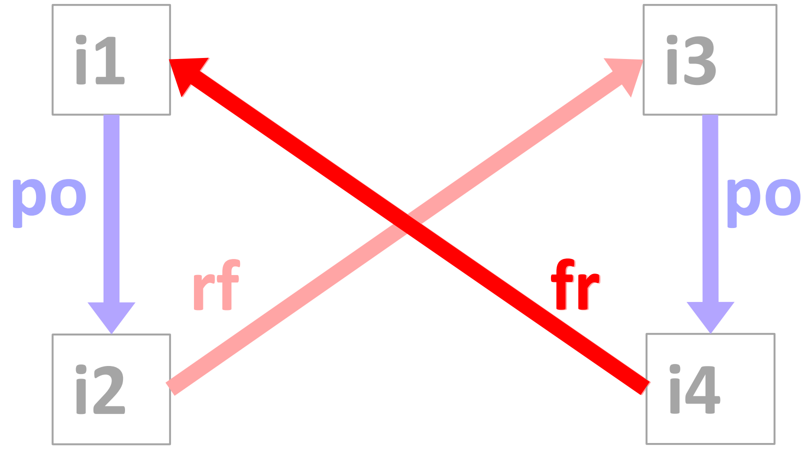

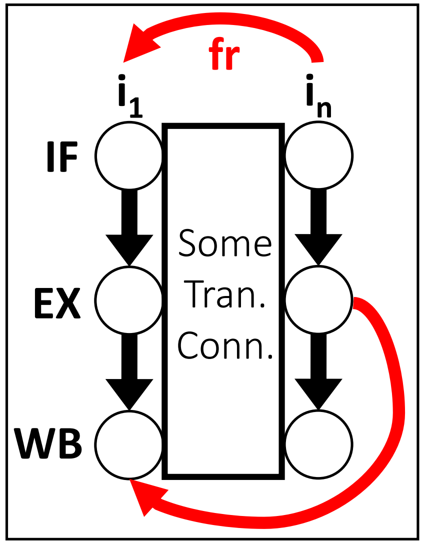

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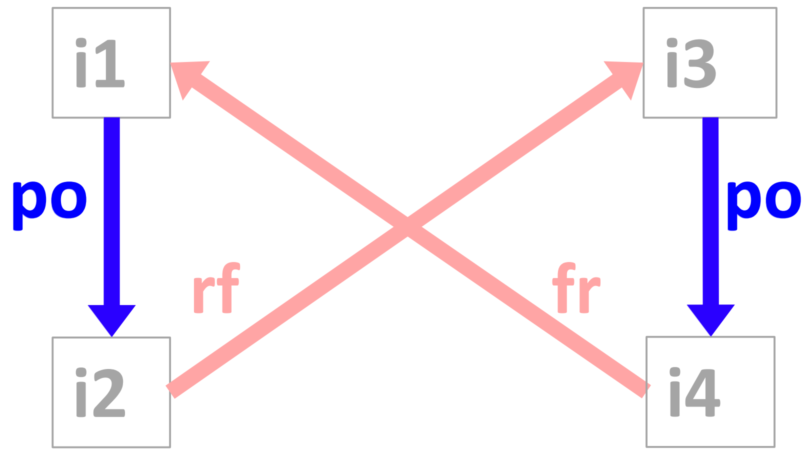

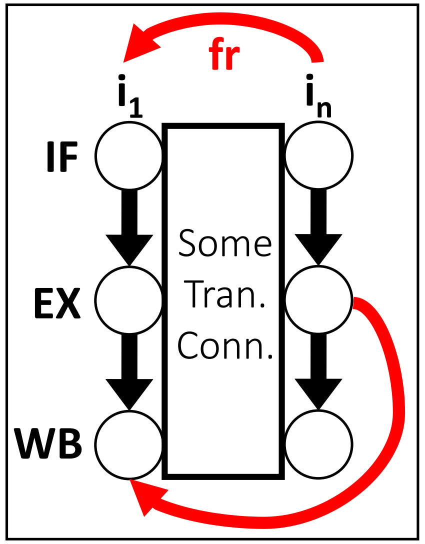

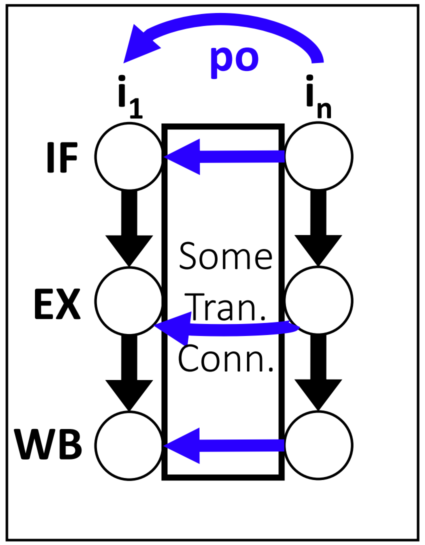

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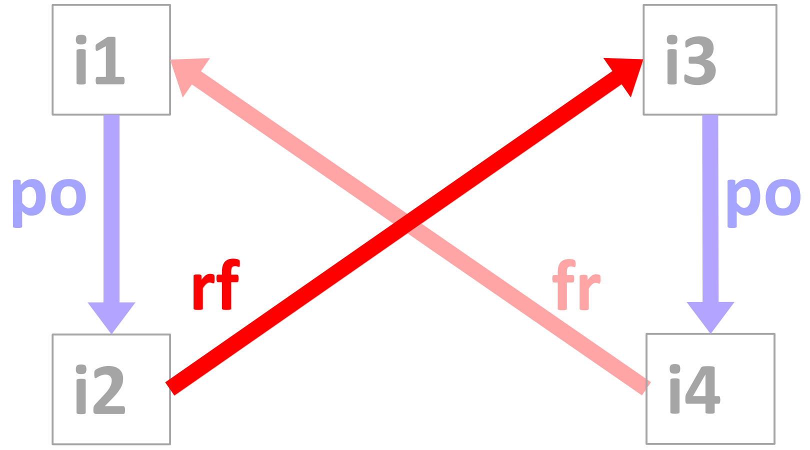
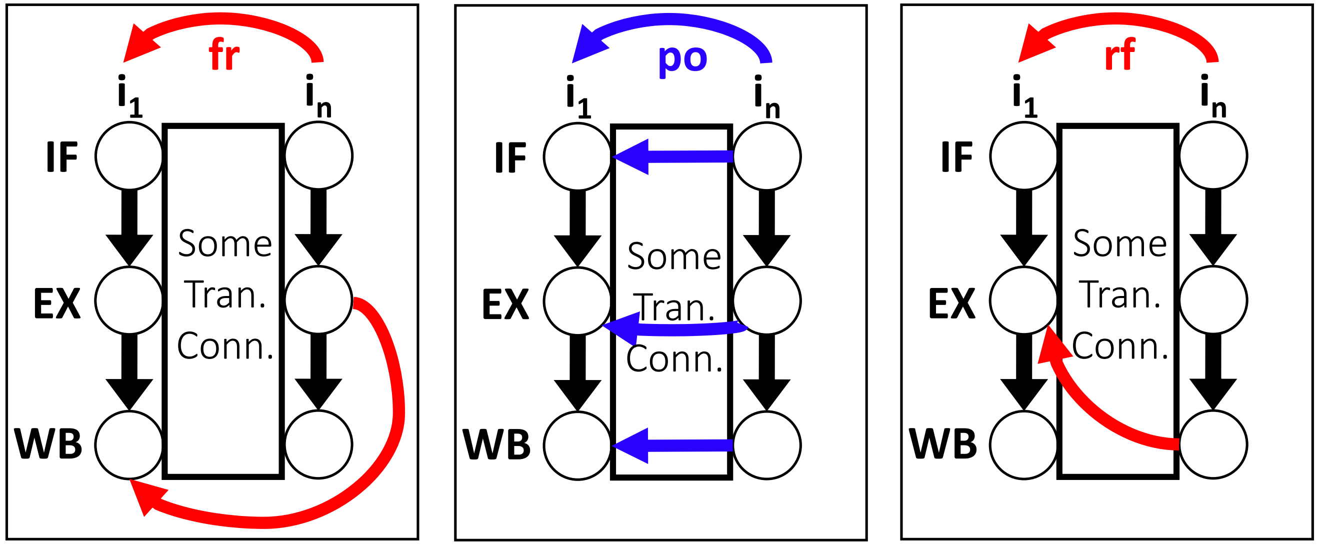


Same cycle is checked 3 times!



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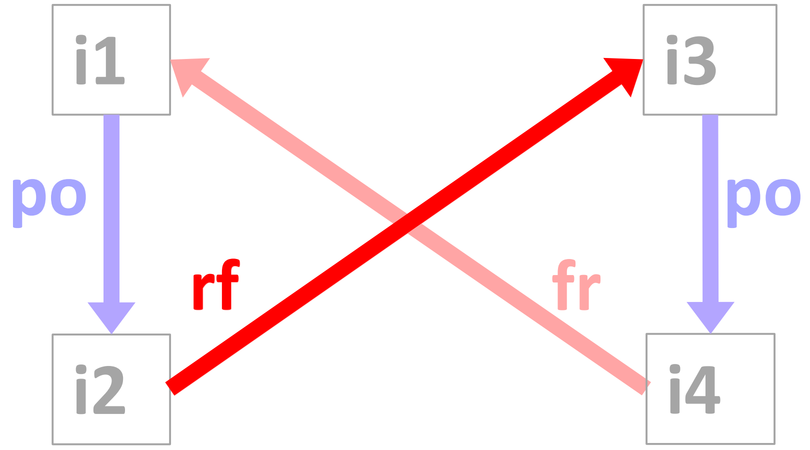
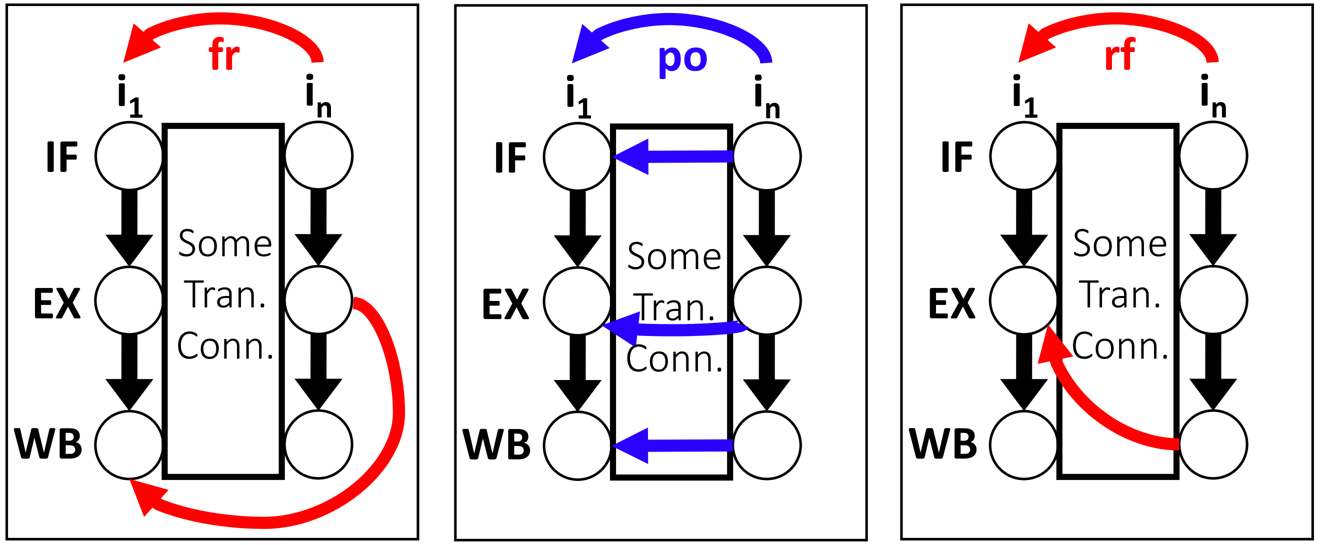


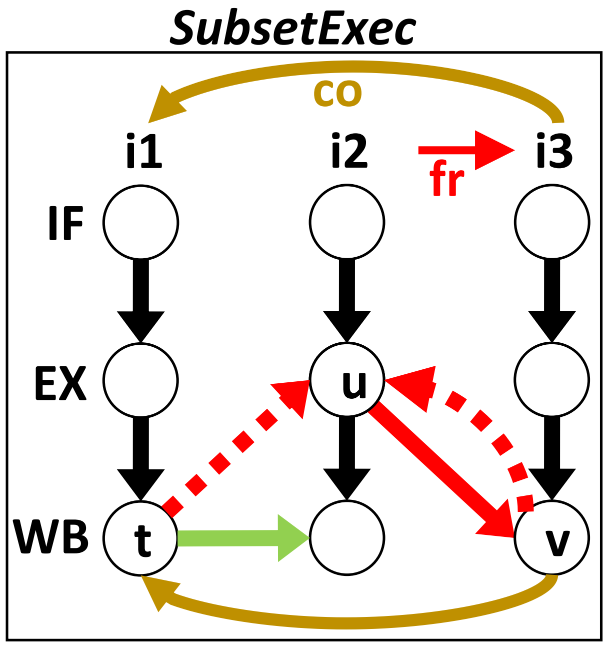


Same cycle is checked 3 times!

<u>Procedure:</u> If all ISA-level cycles containing edge r_i have been checked, do not peel off r_i edges when checking subsequent cycles

The Adequate Model Over-Approximation

- Addition of an instruction can make unobservable execution observable!
- Need to work with over-approximation of microarchitectural constraints
- PipeProof sets all `exists` clauses to true as its over-approximation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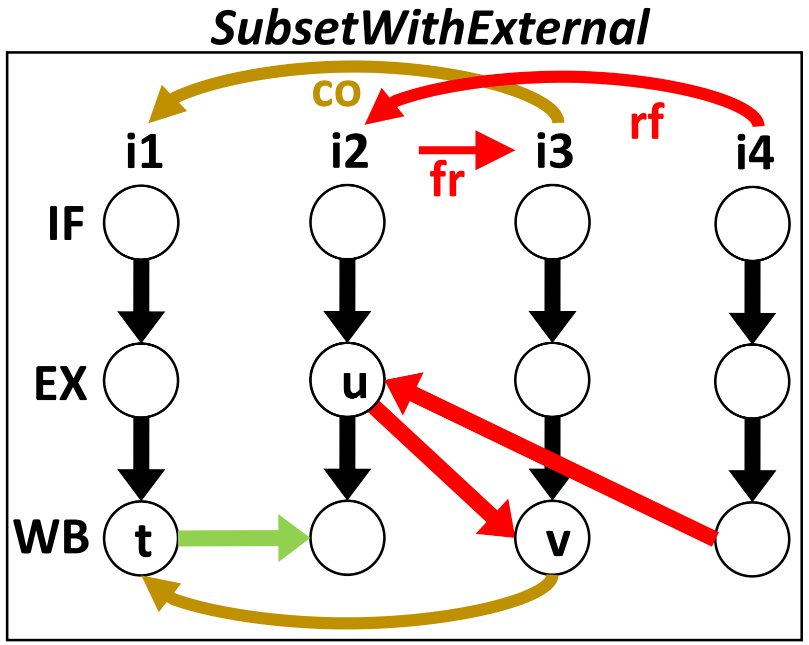
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