CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface

Yatin A. Manerkar, Daniel Lustig,
Michael Pellauer*, and Margaret Martonosi

Princeton University *NVIDIA

MICRO-48

Coherence and Consistency

At a high level:

- **Coherence Protocols:** Propagation of writes to other cores
- **Consistency Models:** Ordering rules for visibility of reads and writes

Coherence and Consistency

Coherence Verifiers

Consistency Verifiers

Arch. Level

Coherence and Consistency

Coherence Verifiers

Consistency Verifiers

Arch. Level

Coherence and consistency often interwoven

µarch. Level

Coherence and Consistency

Coherence Verifiers

Ignore consistency even when protocol affects consistency!

Consistency Verifiers

Assume abstract coherence instead of protocol in use!

Arch. Level

Coherence and consistency often interwoven

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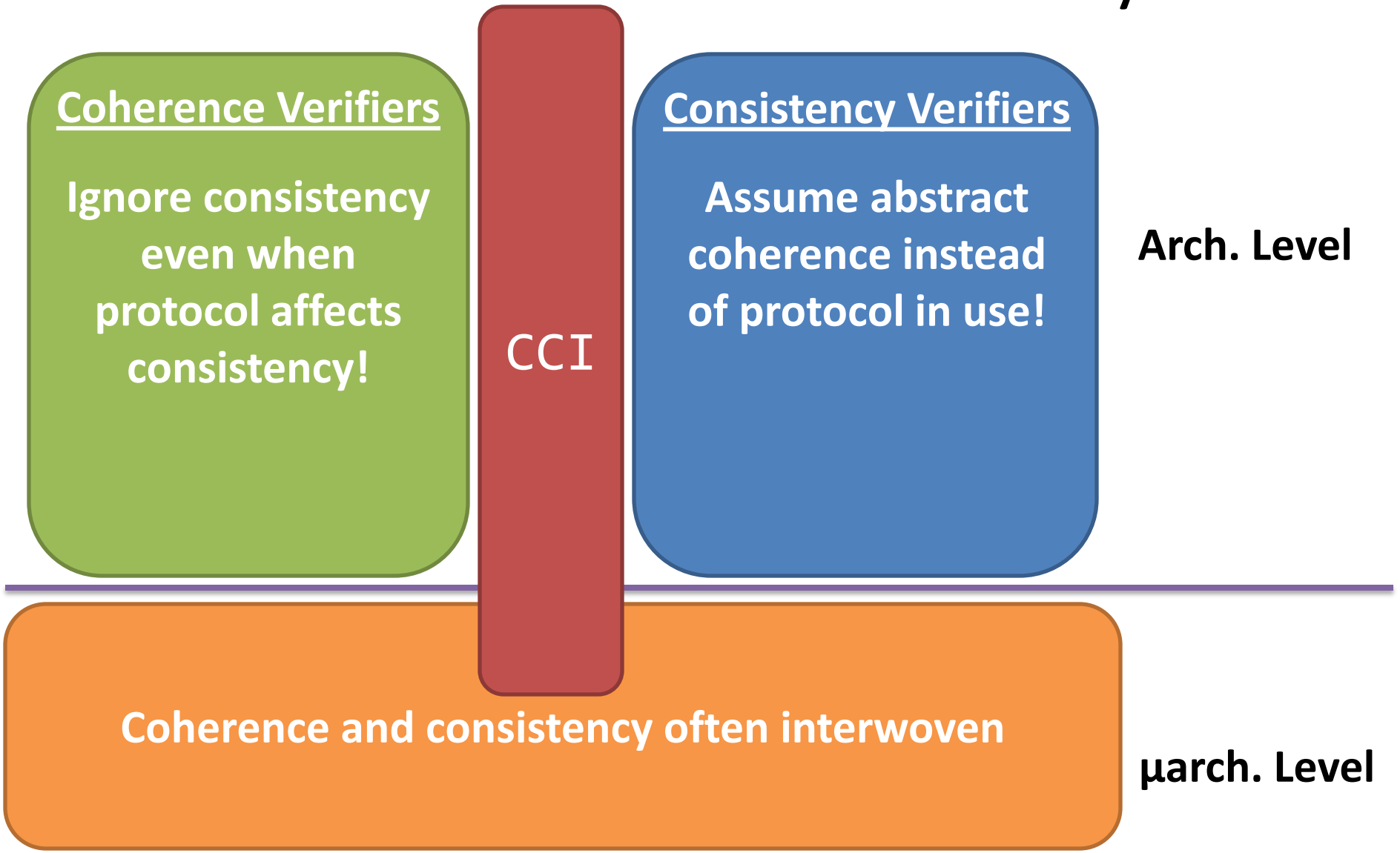
Coherence and Consistency



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Individual Opt. → **No violation**

Combination of Opts. → **Violation!**

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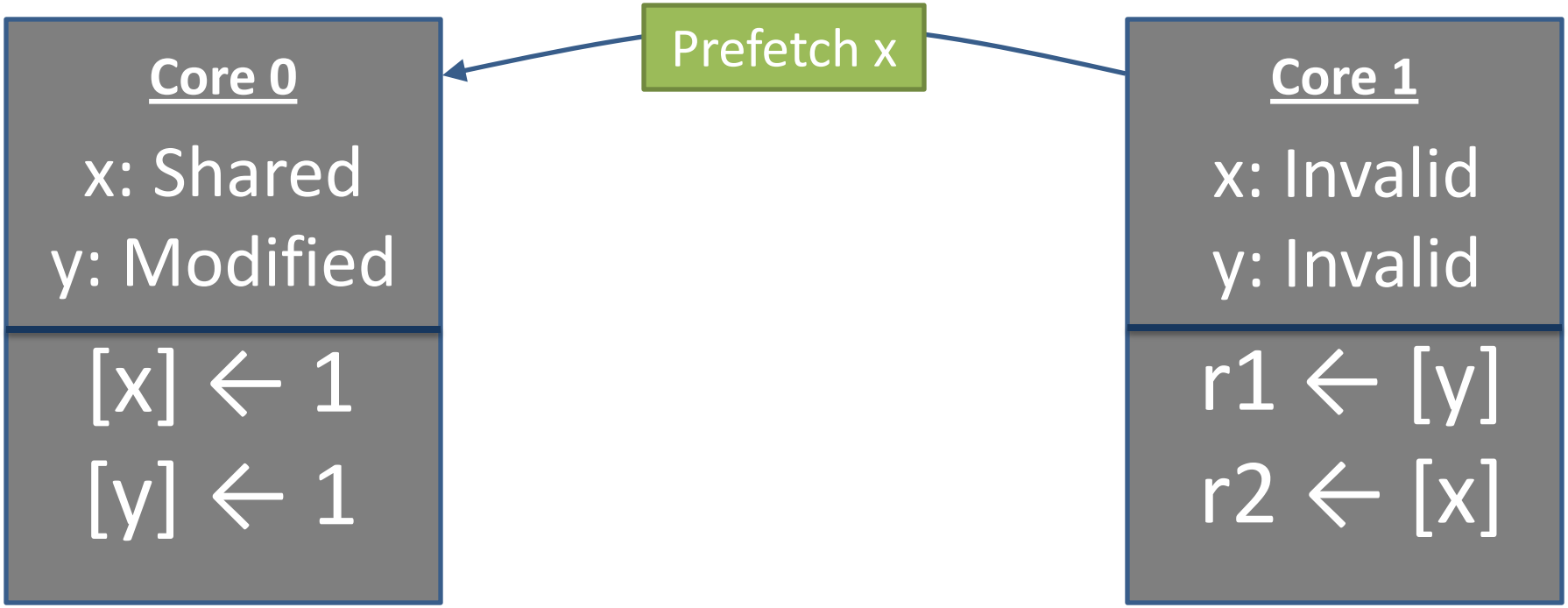

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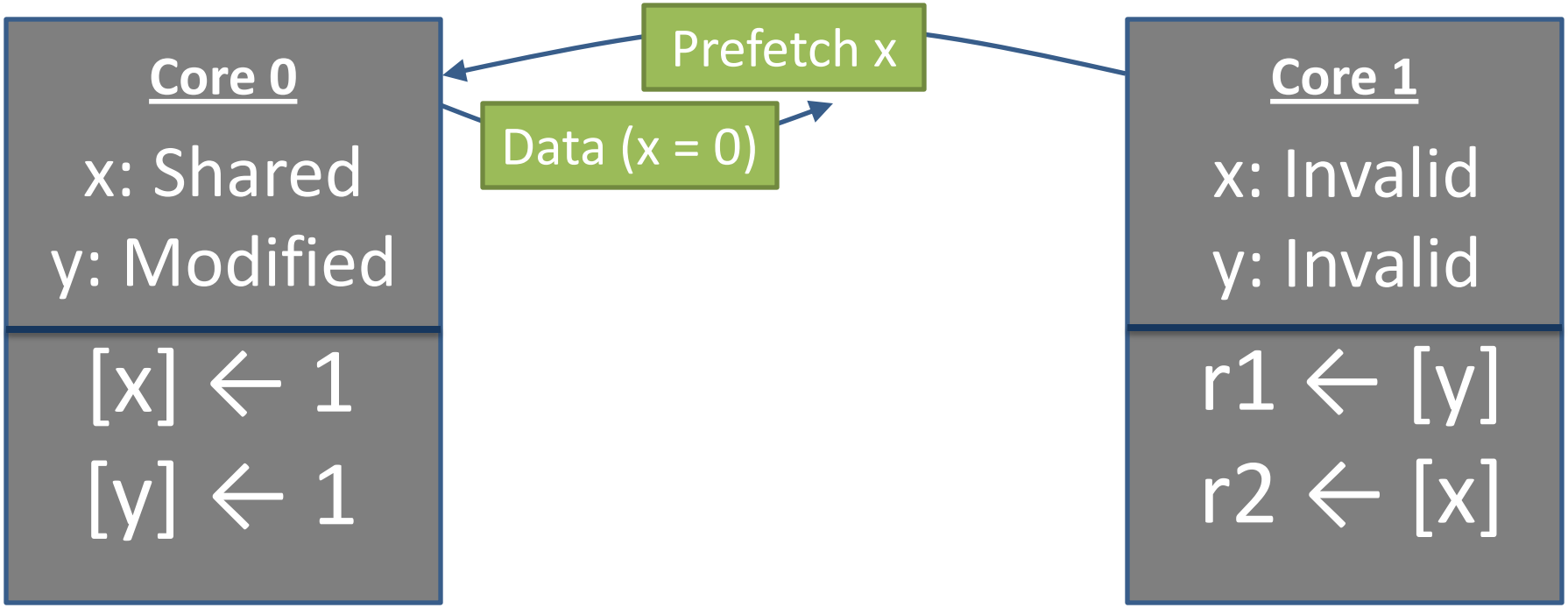

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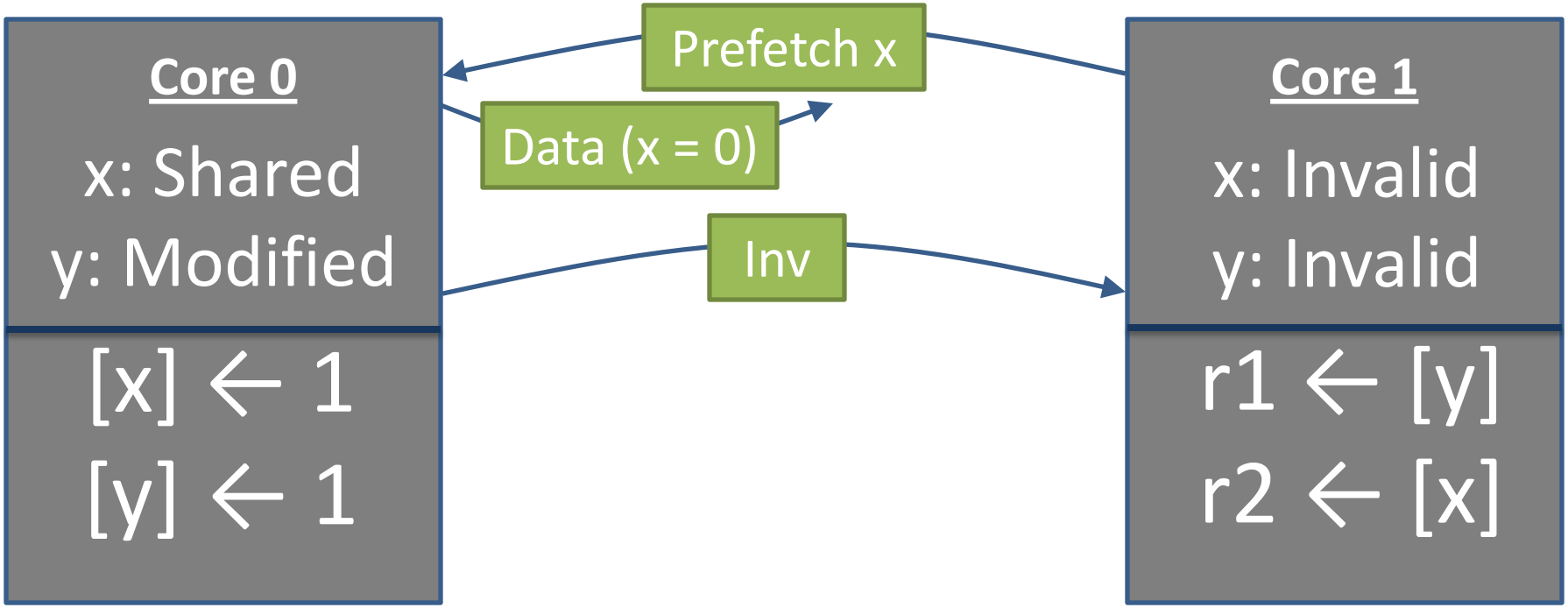

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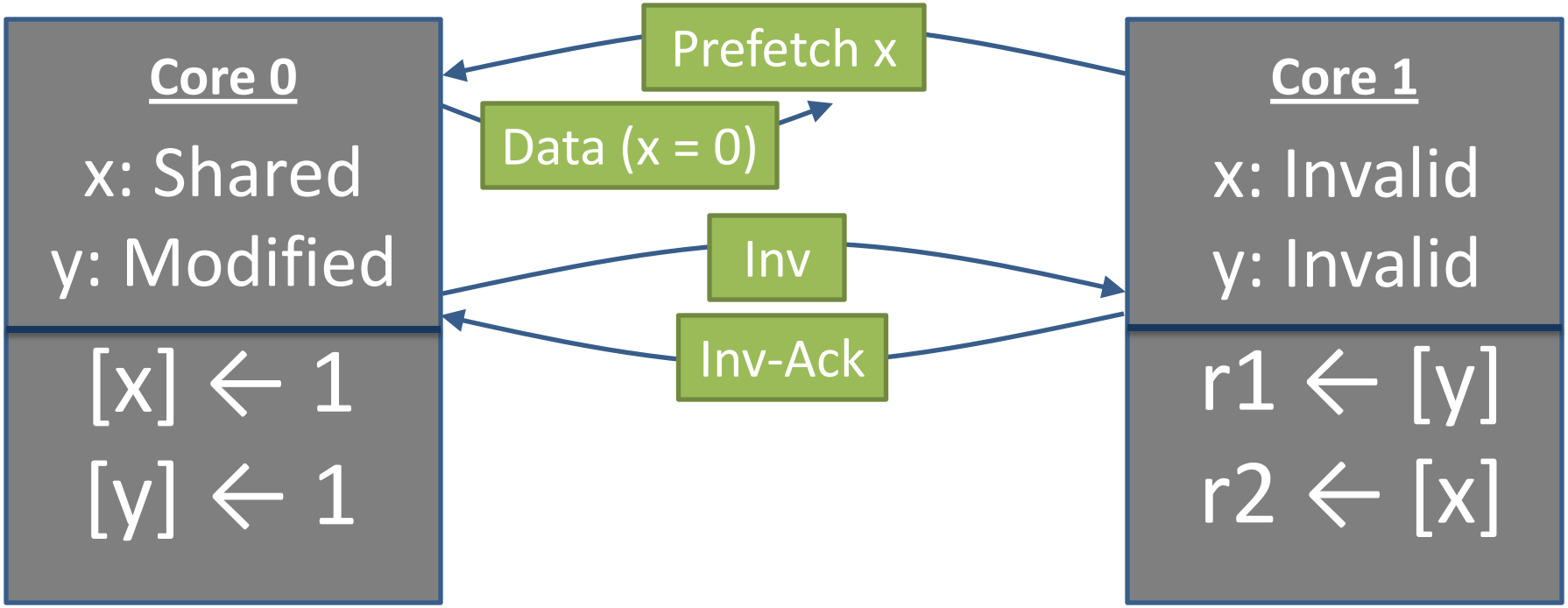

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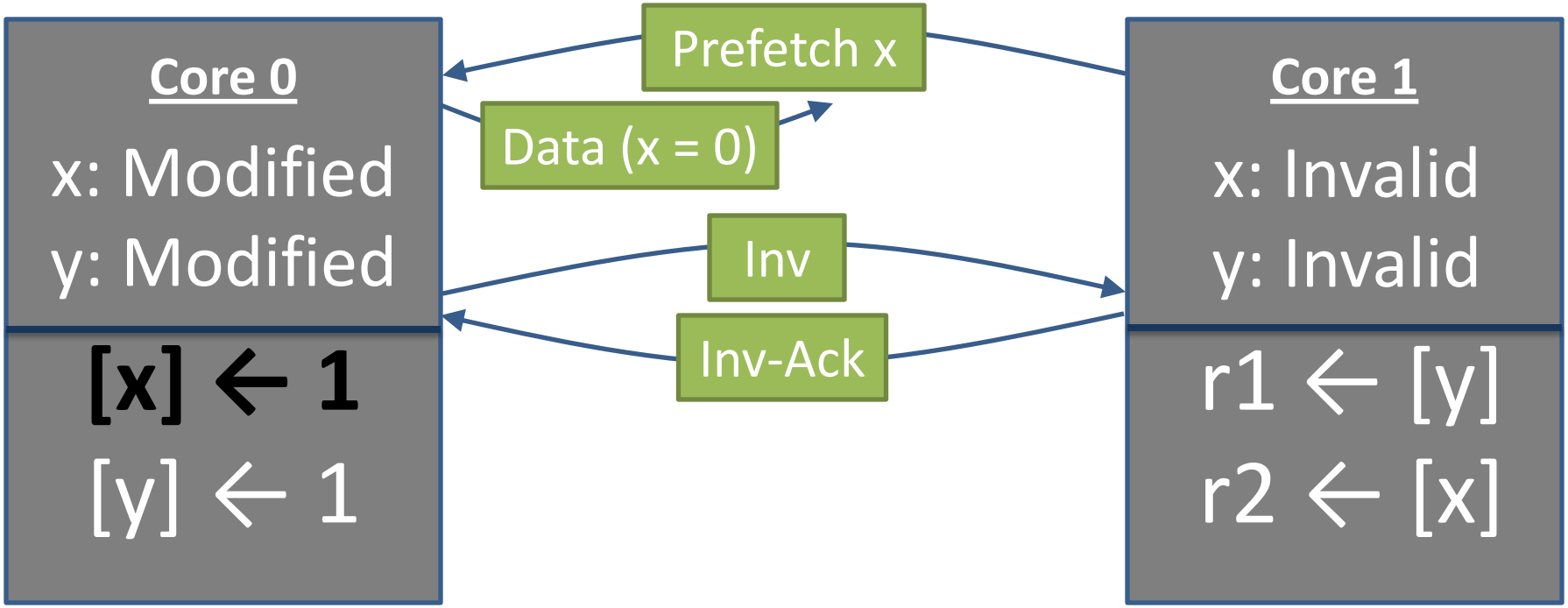

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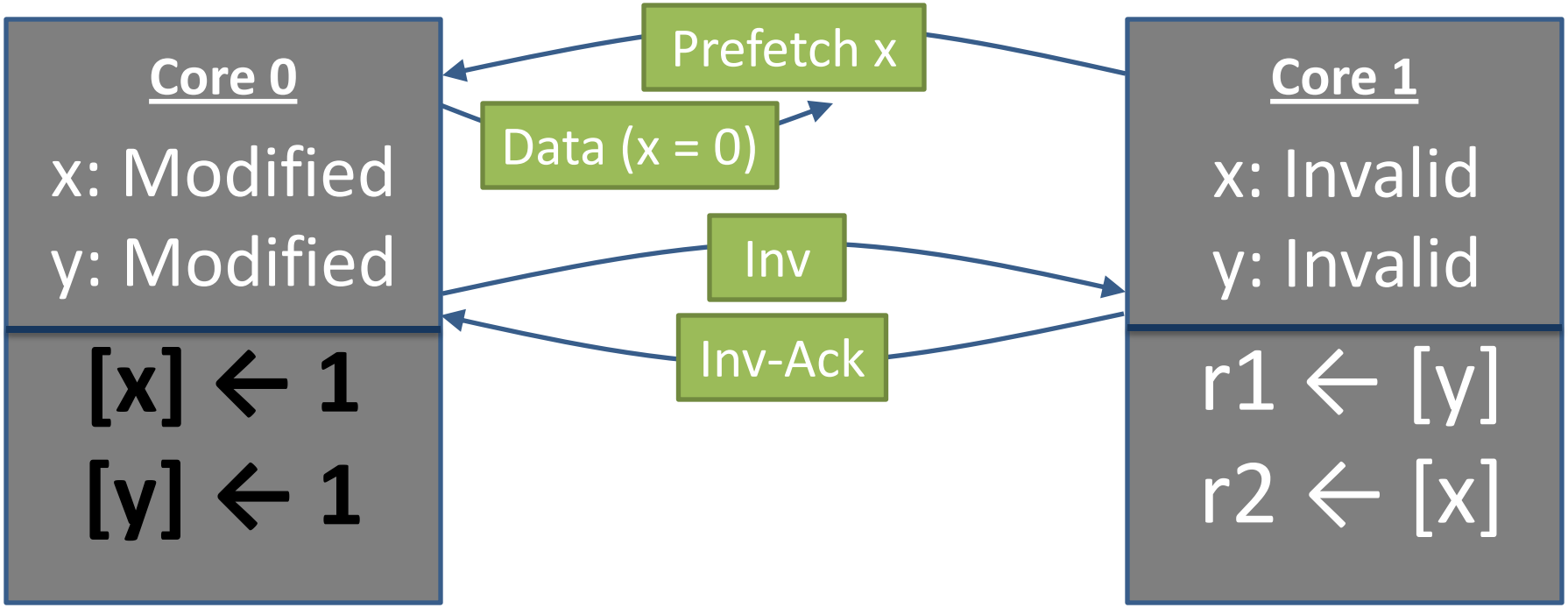

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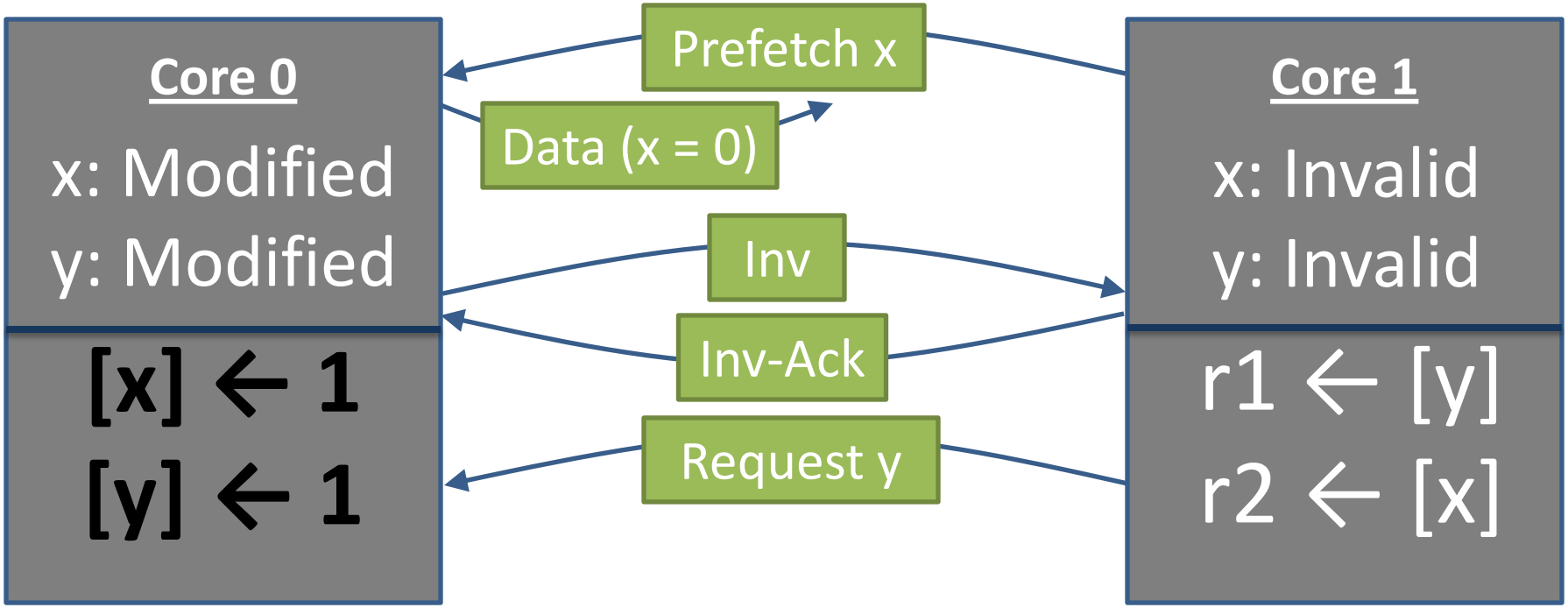

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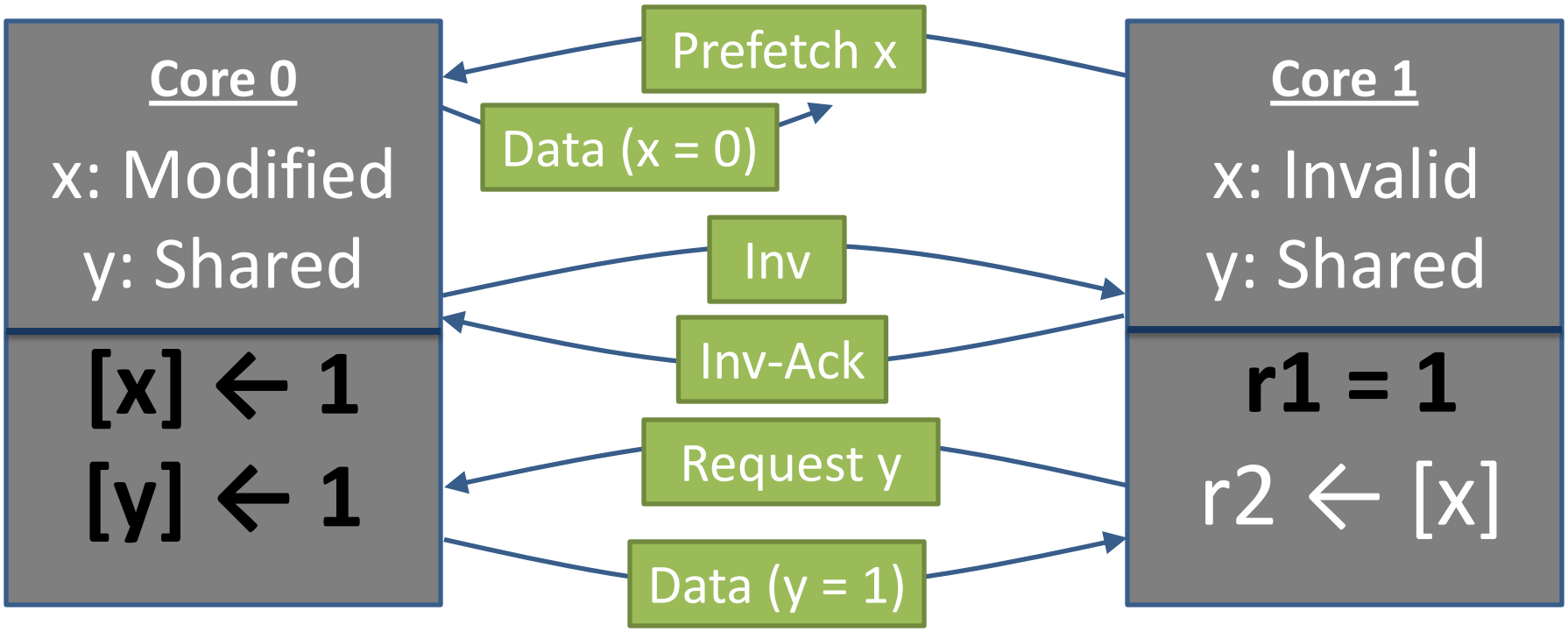

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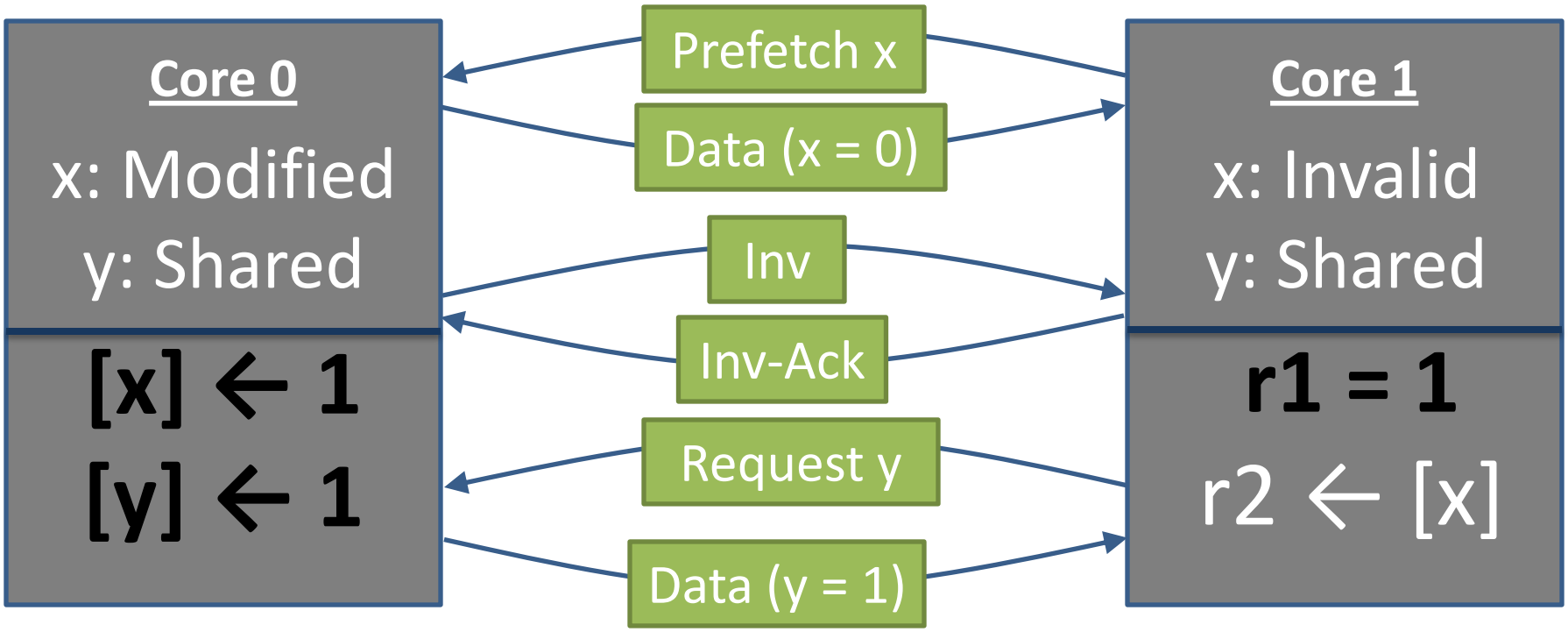

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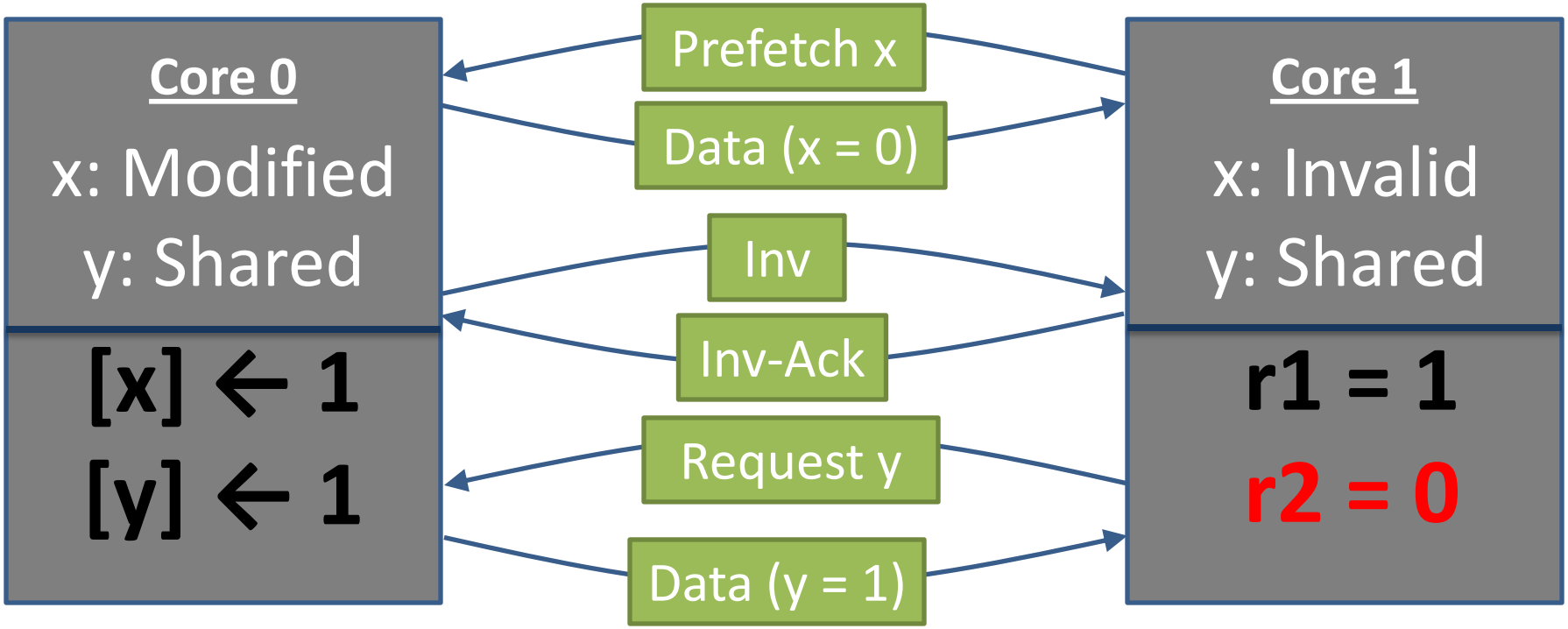
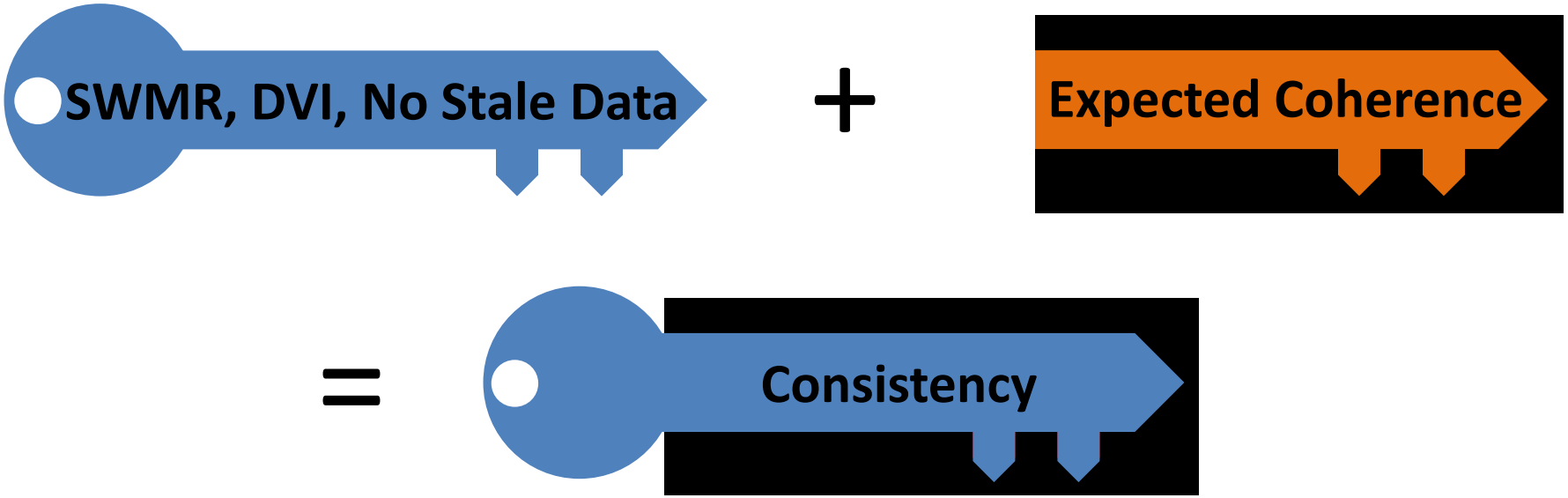


The Coherence-Consistency Interface (CCI)



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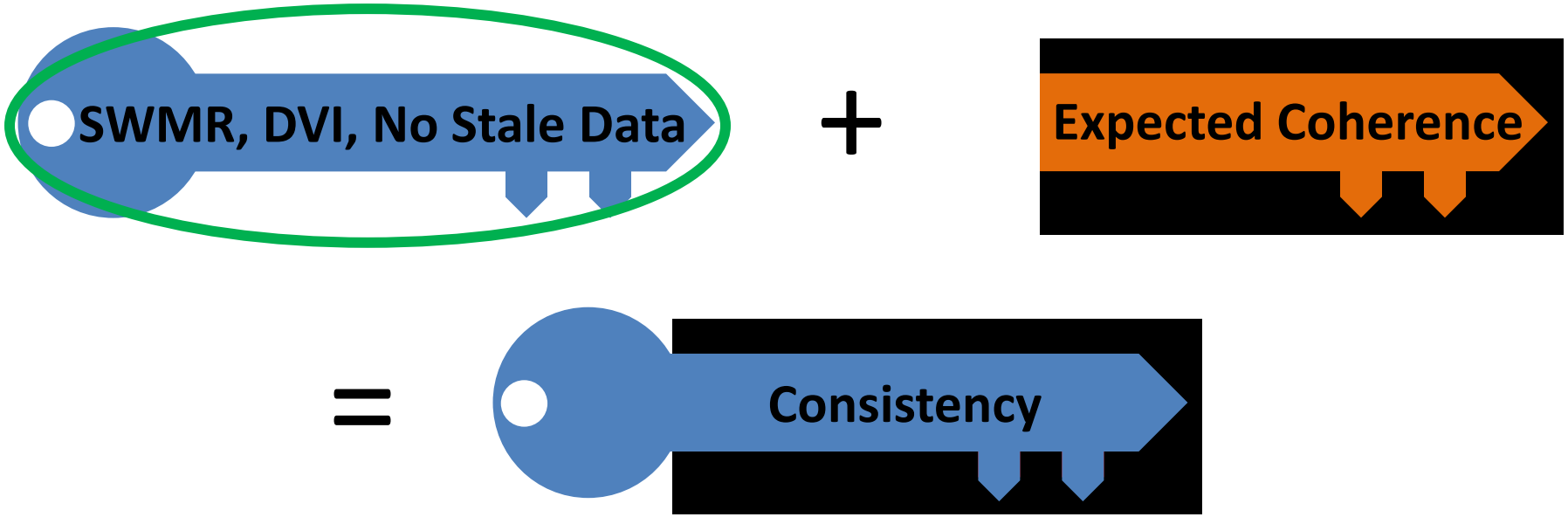

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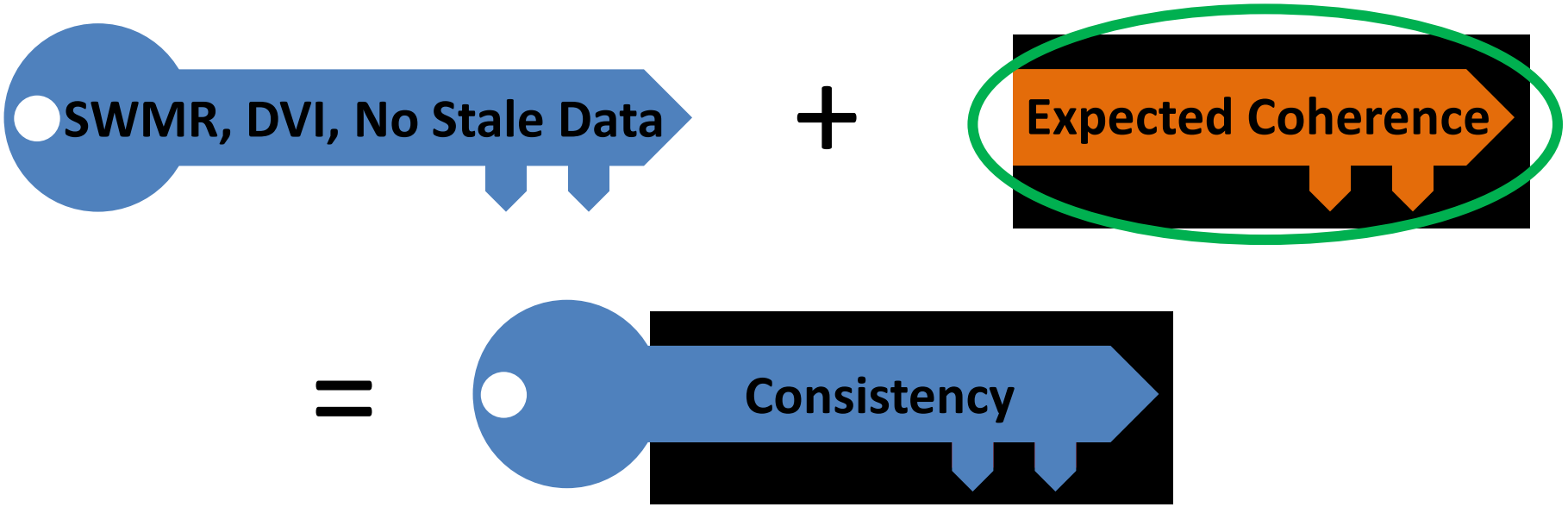

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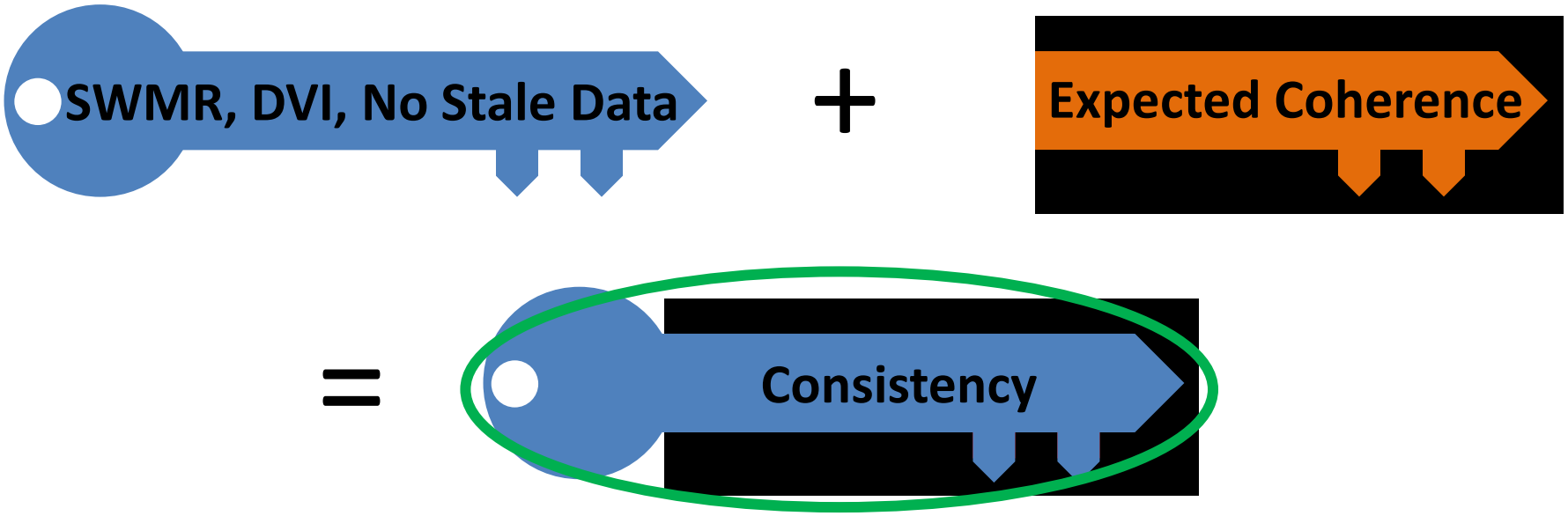

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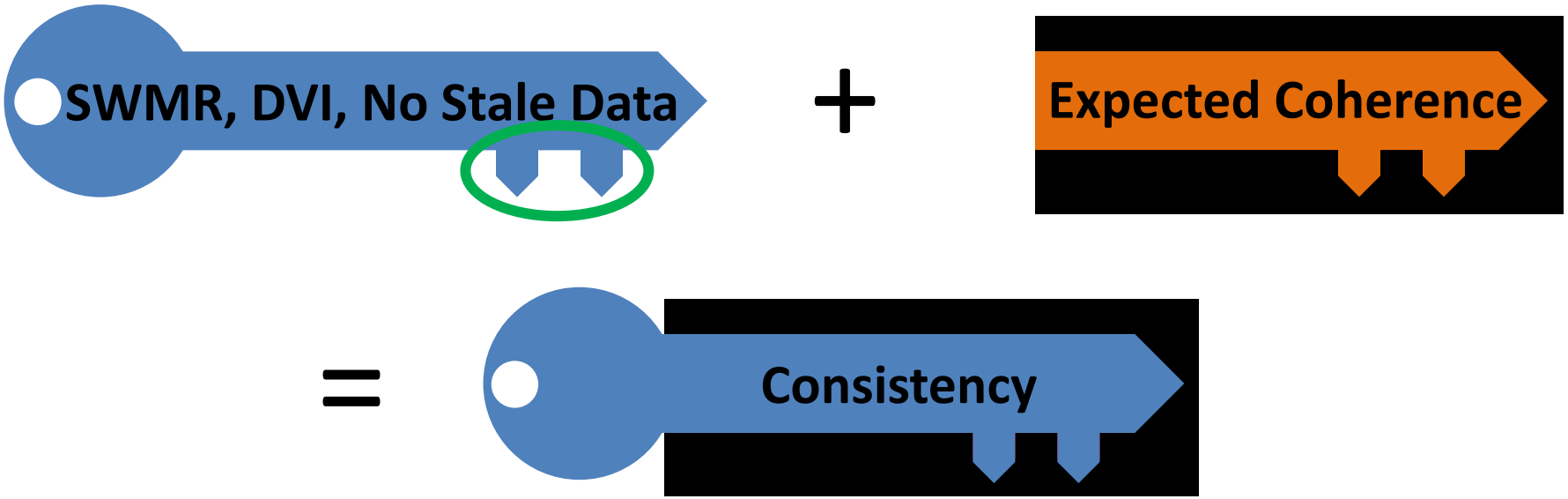

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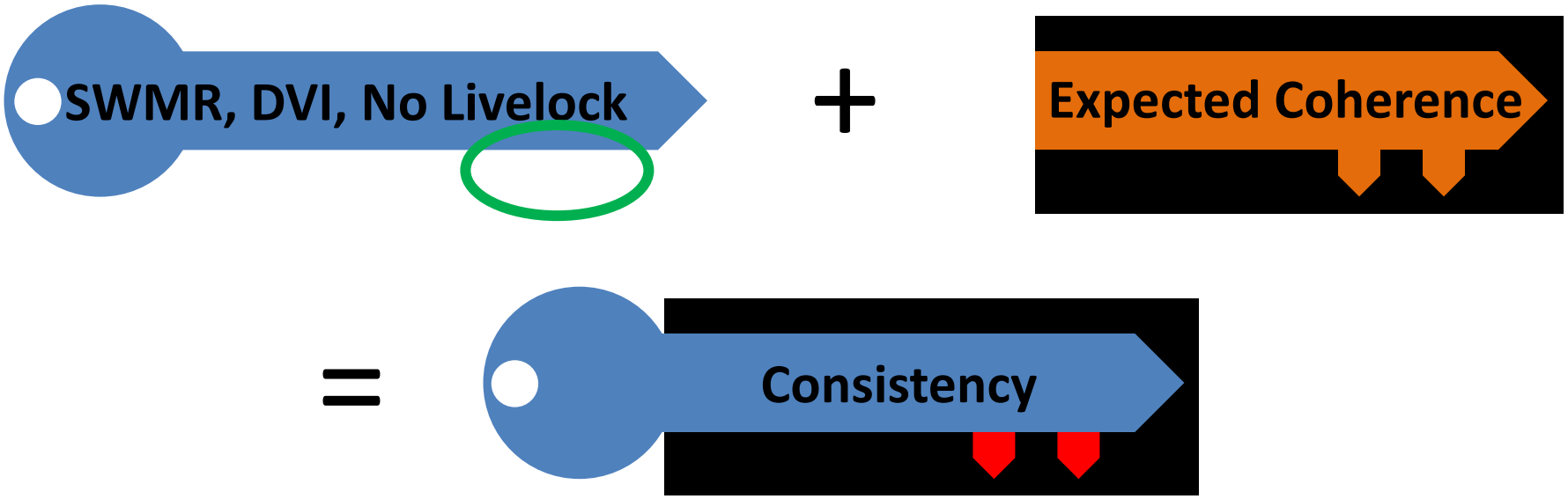

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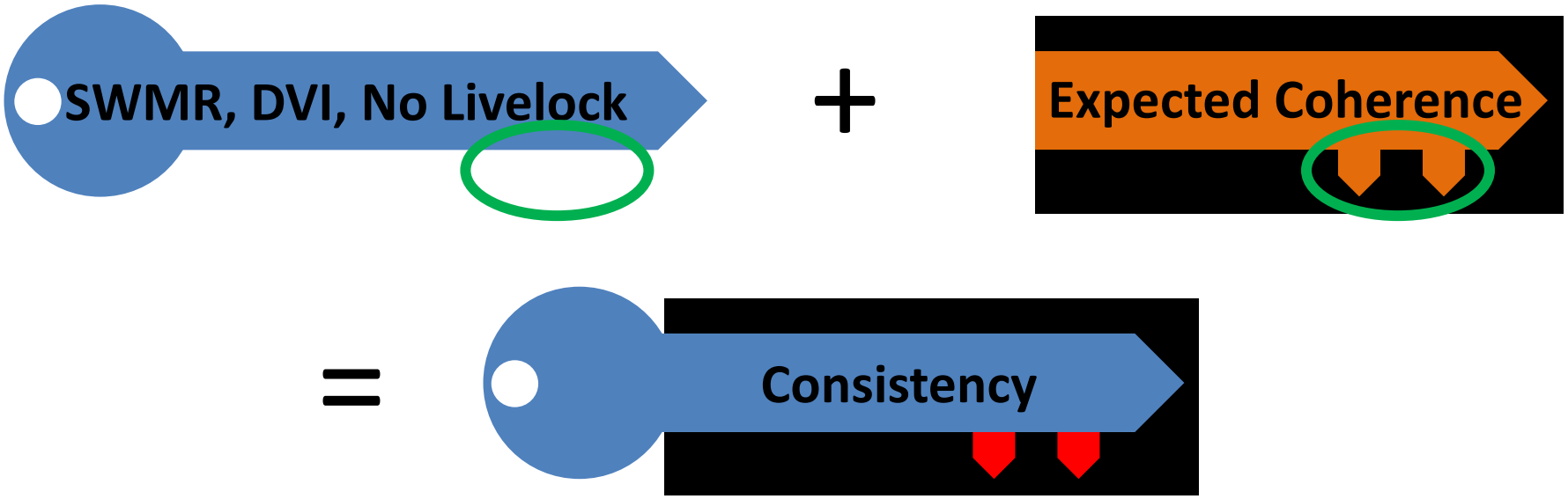

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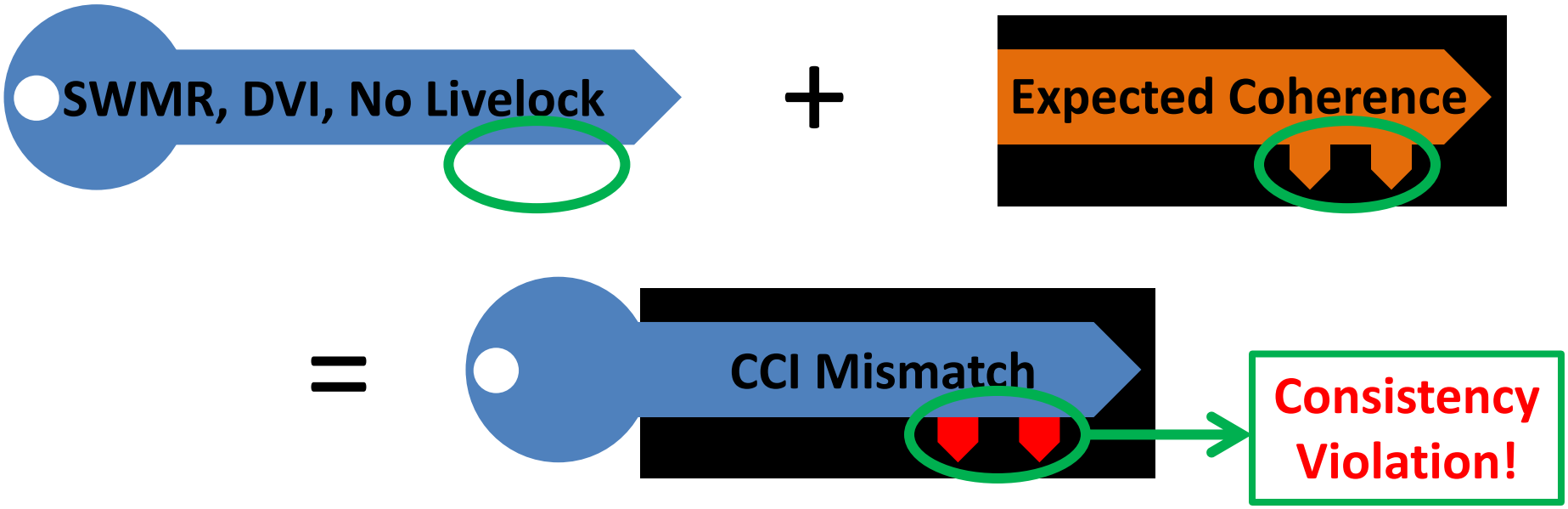

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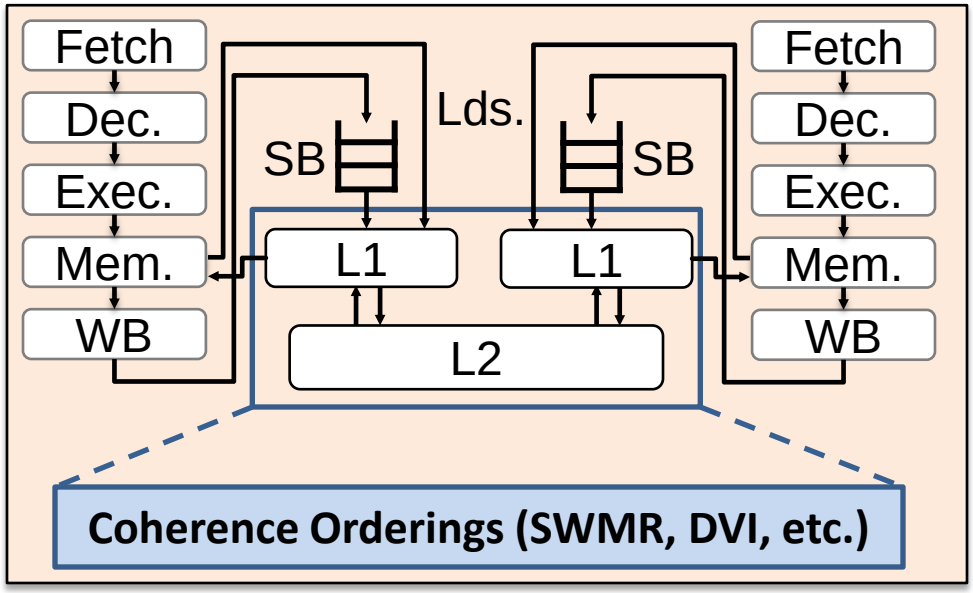
Our Work: CCICheck

Static CCI-aware consistency verification



Microarch spec

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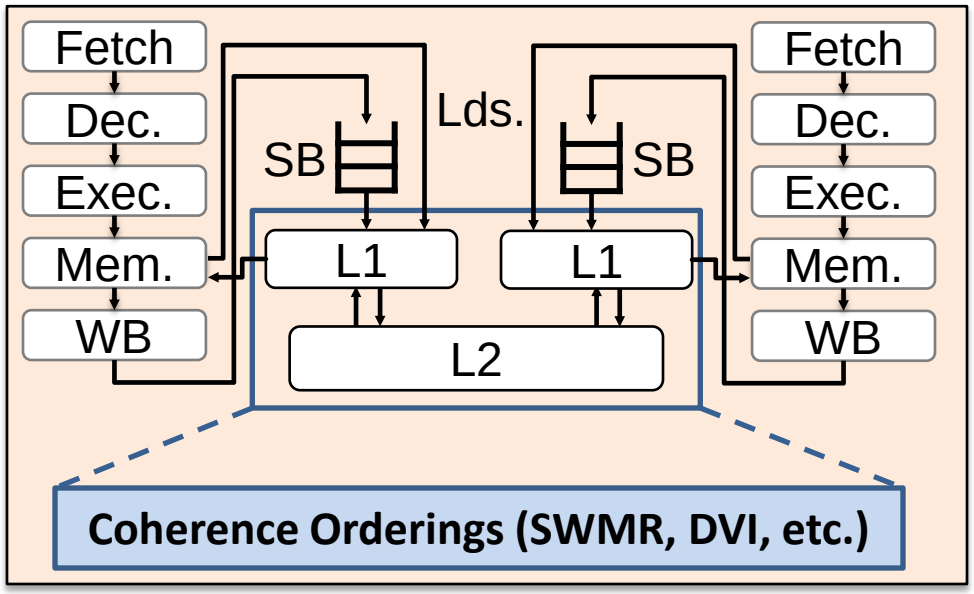

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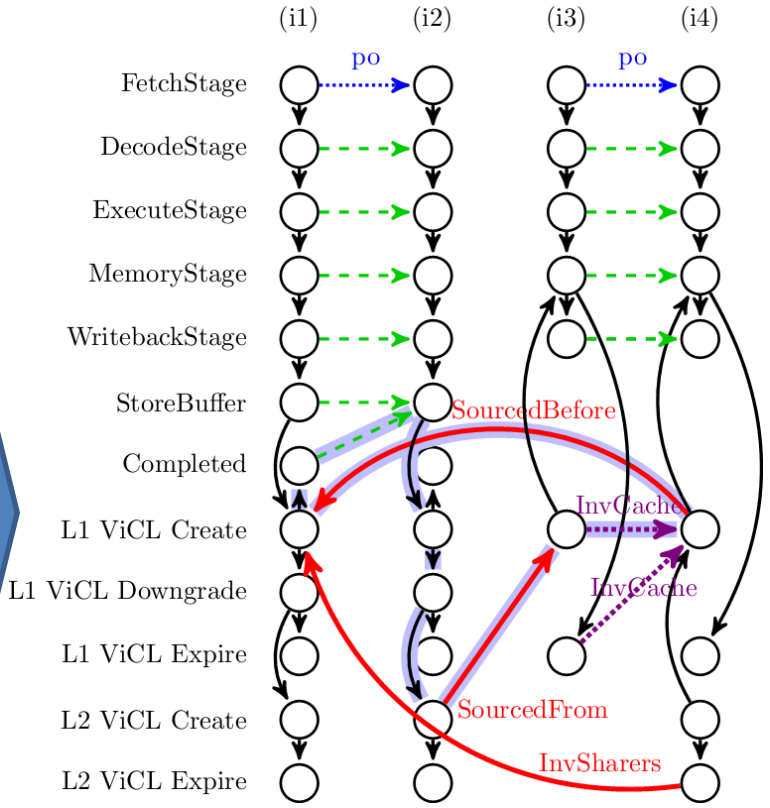
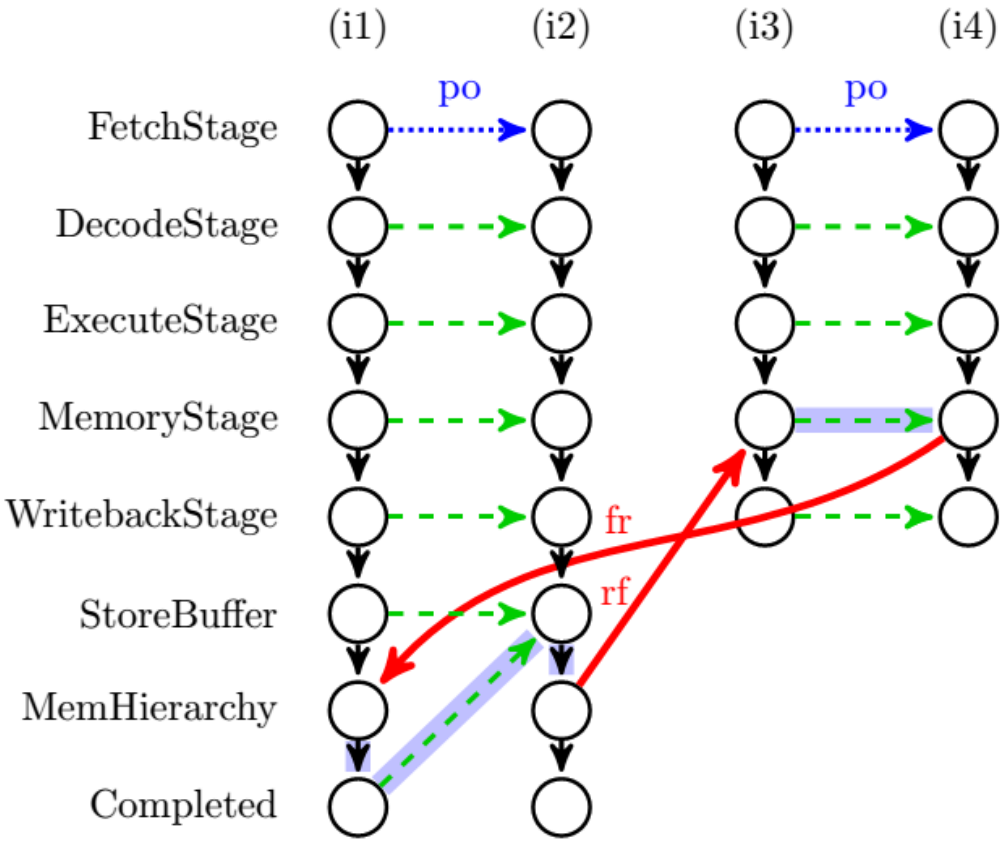


Microarchitectural happens-before (μhb) graph

Background: PipeCheck



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- **Exhaustive enumeration** of executions using μhb graphs
- **Cyclic graph →forbidden by μarch**
- **Acyclic graph →allowed by μarch**

[Lustig et al. MICRO-47]

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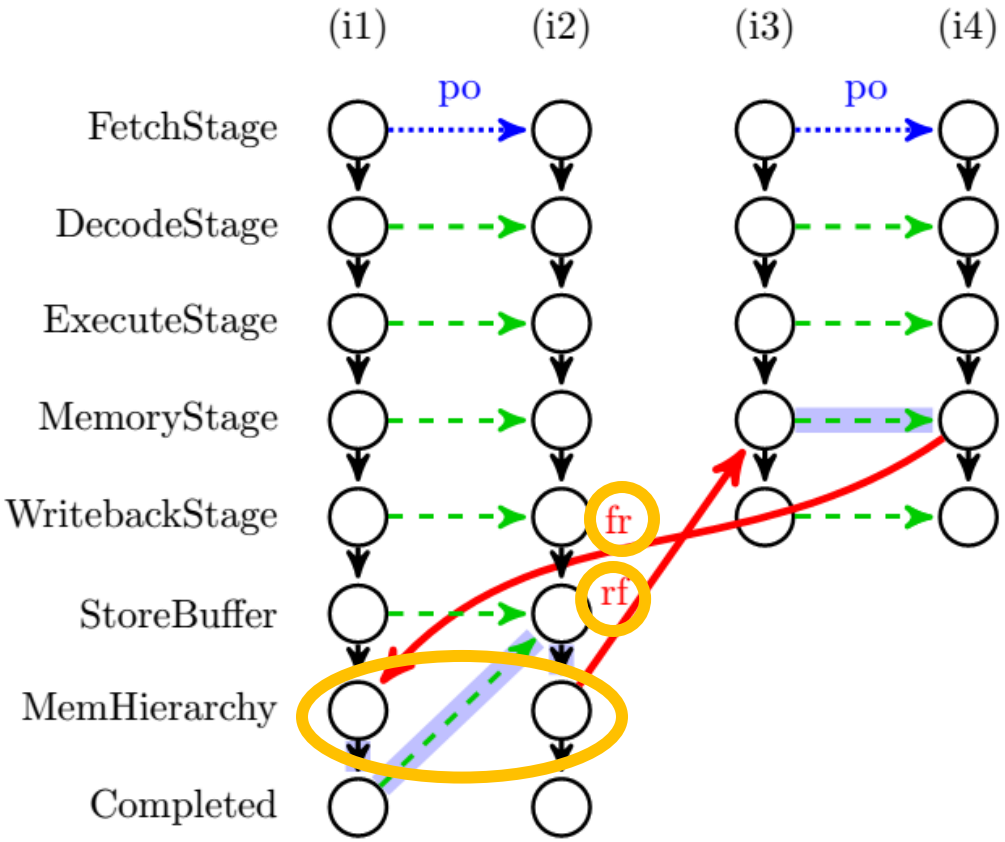

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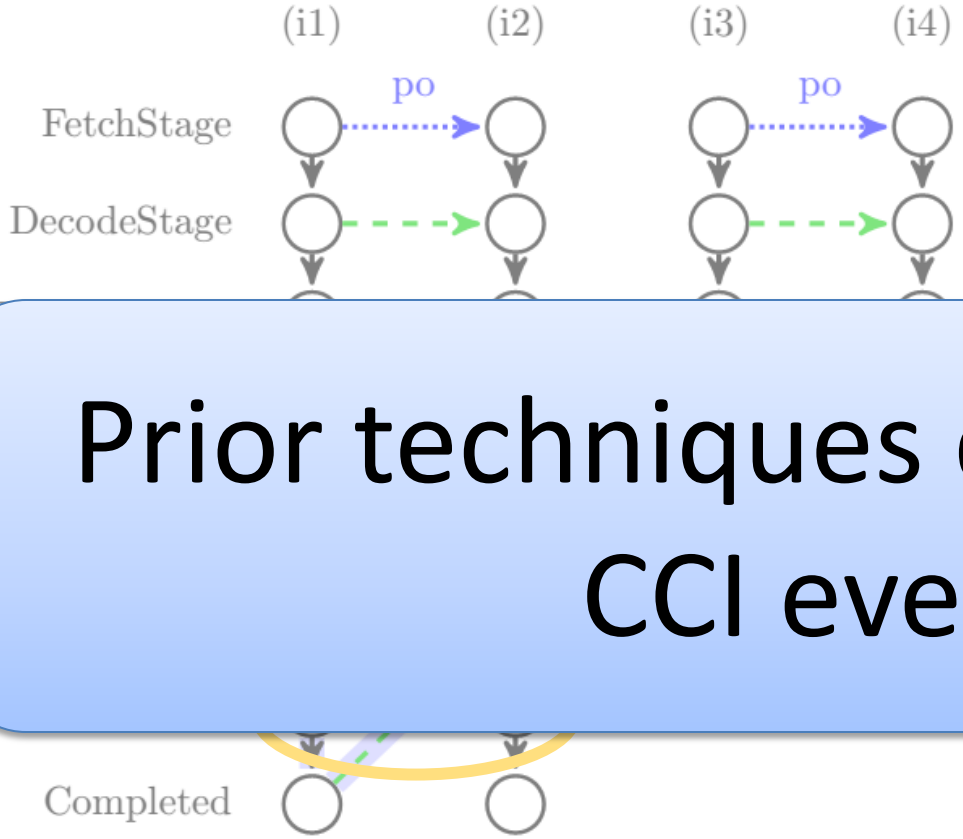

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Prior techniques cannot model CCI events!

- **Acyclic graph →allowed by μarch**

[Lustig et al. MICRO-47]

Modelling CCI Events

- Need to model **per-cache occupancy**
  - Lazy coherence and partial incoherence (e.g. GPUs)
- Need to model **coherence transitions** that relate to consistency (e.g. Peekaboo)

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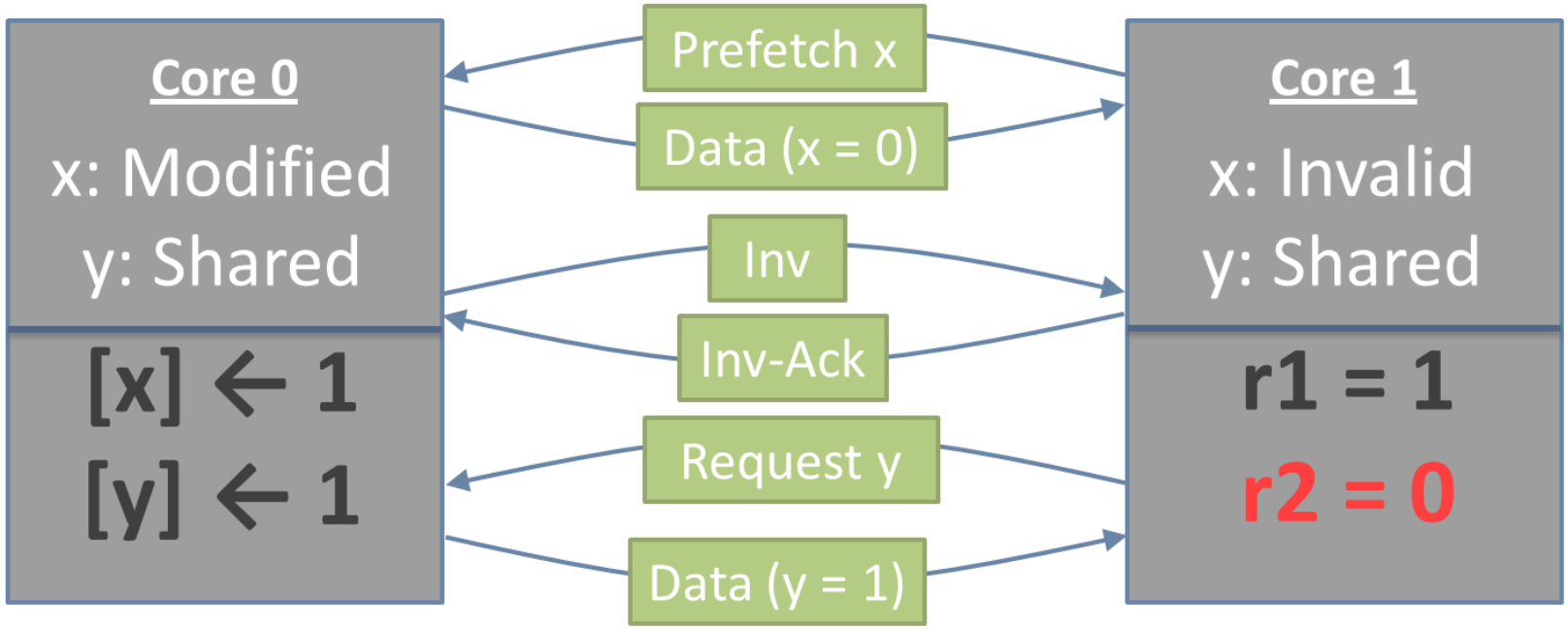

ViCL: Value in Cache Lifetime

- 4-tuple:

  (cache_id, address, data_value, generation_id)

- **cache_id** and **generation_id** uniquely identify each cache line
- A ViCL 4-tuple maps on to the period of time over which the cache line serves the data value for the address
- ViCLs start at a **ViCL Create** event and end at a **ViCL Expire** event

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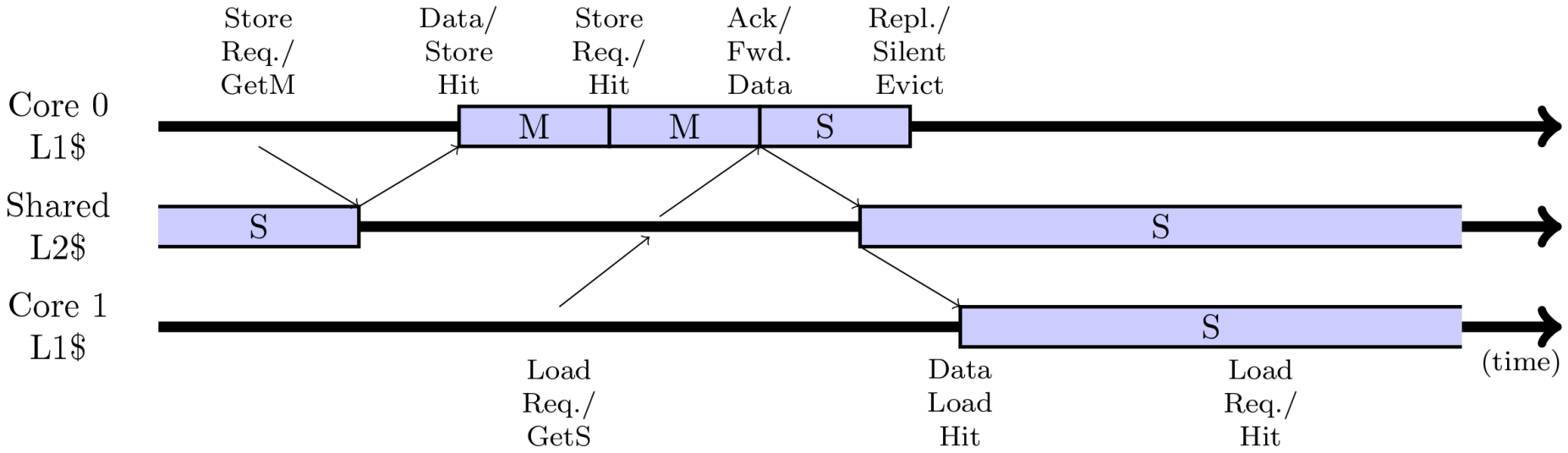

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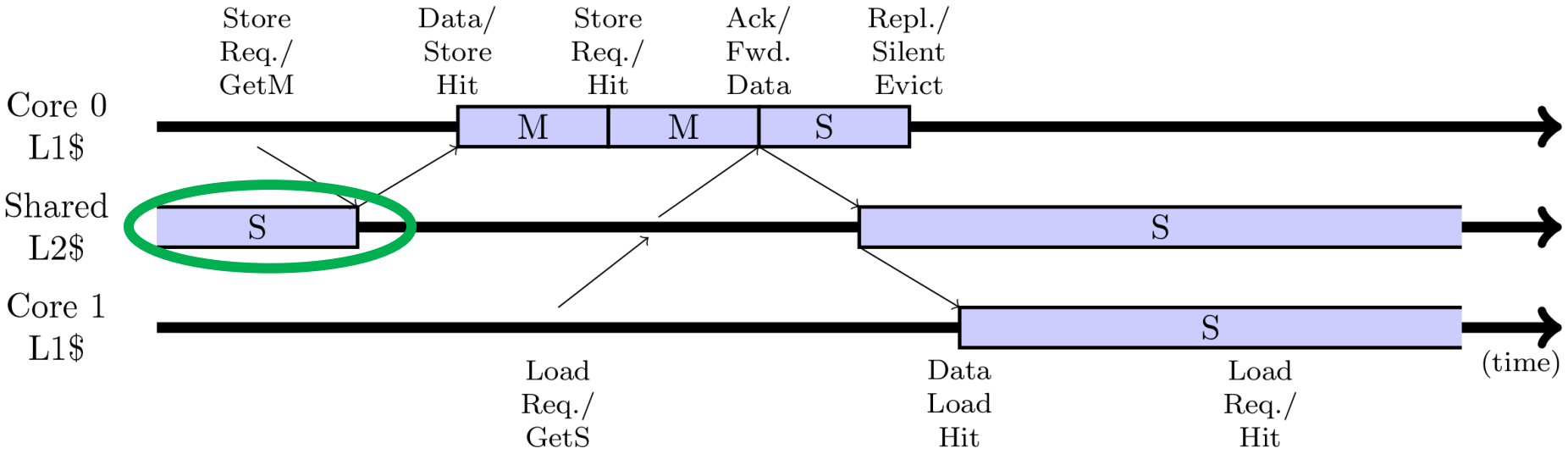

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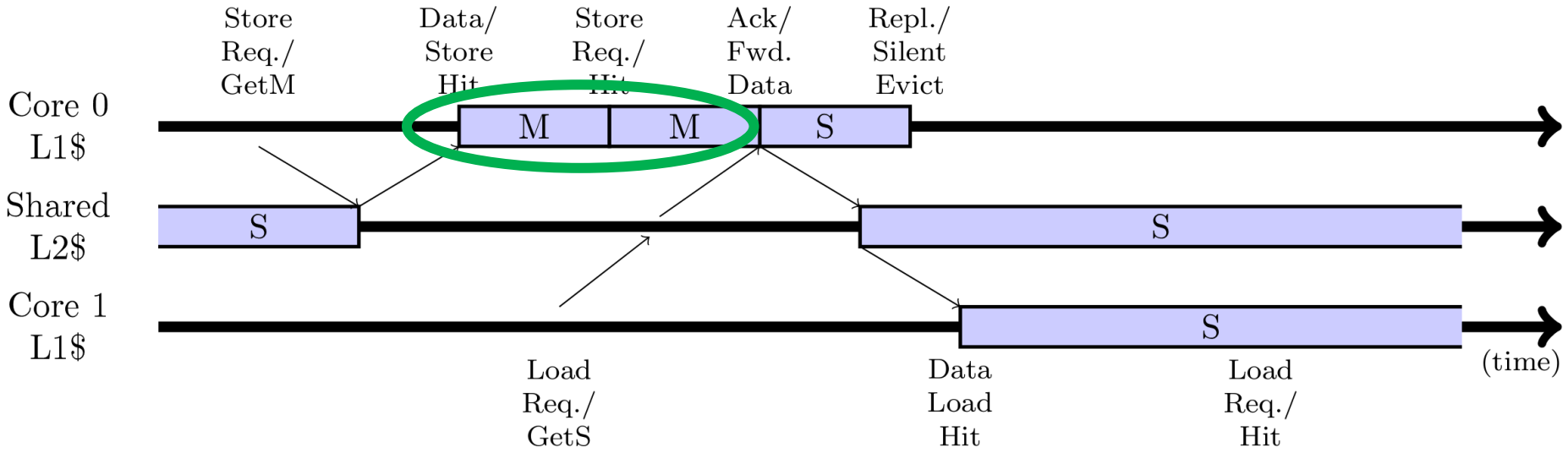

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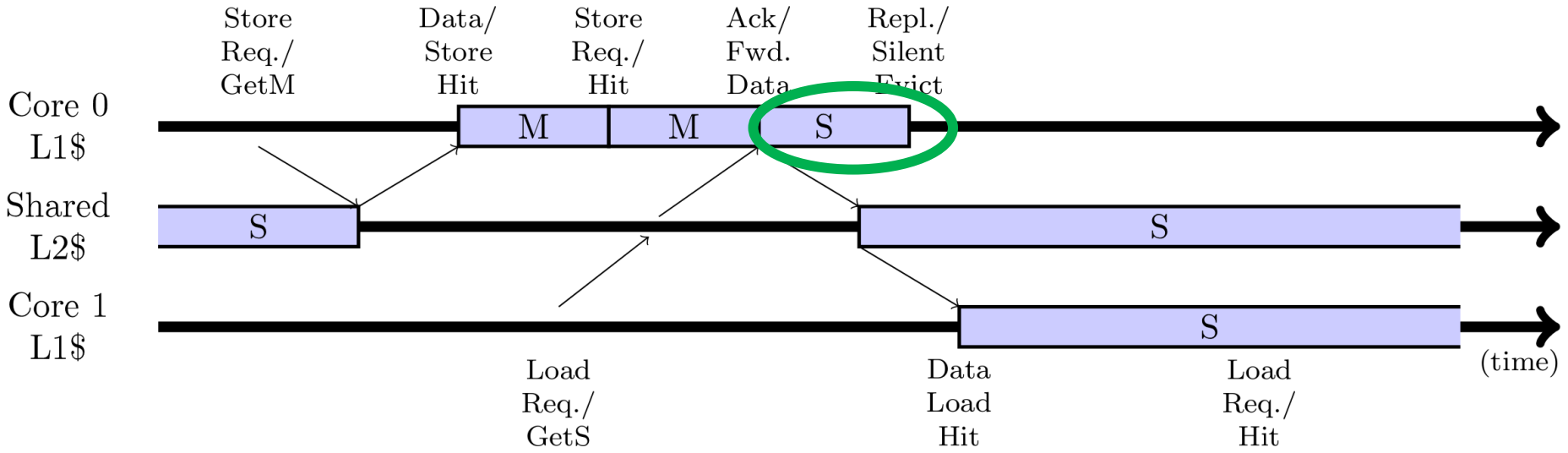

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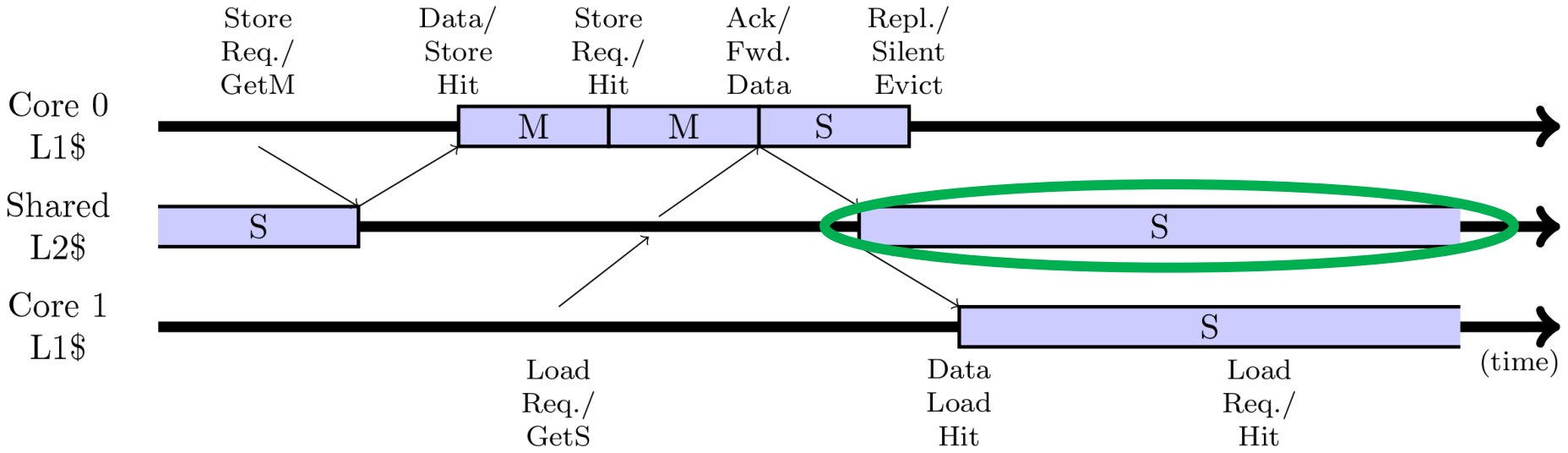

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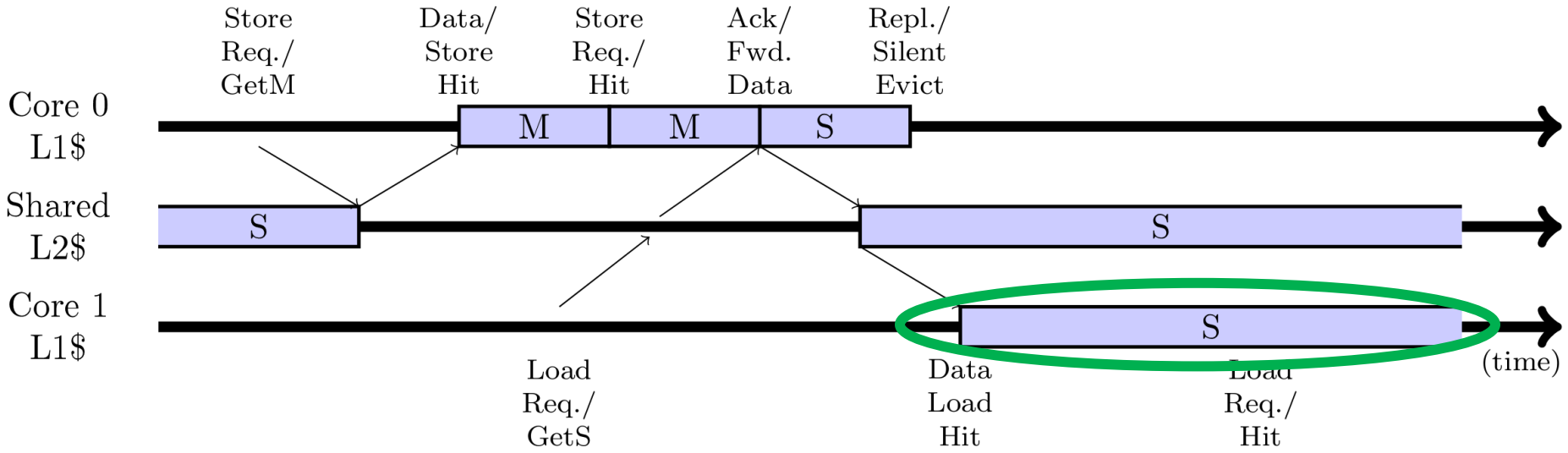
In TSO: r1=2, r2=2 Allowed	

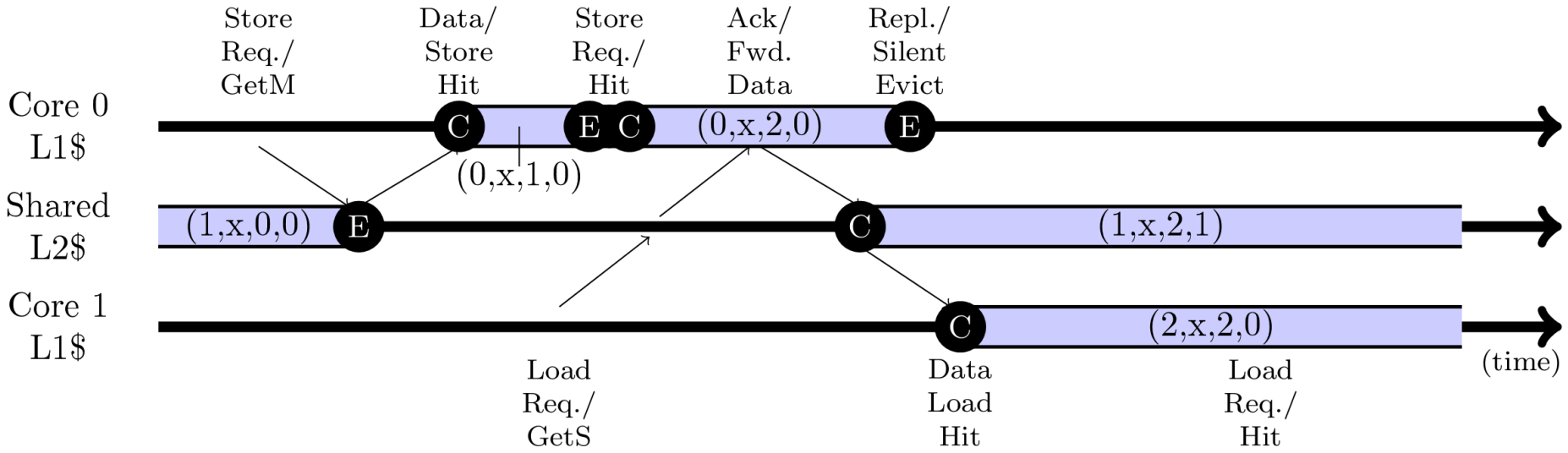


ViCL: Value in Cache Lifetime

Now with ViCLs

Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
(i2) St [x] ← 2	(i4) Ld r2 ← [x]
In TSO: r1=2, r2=2 Allowed	



ViCL Nodes

C ViCL Create

E ViCL Expire

ViCL (cache id, addr, data, gen. id)

ViCL: Value in Cache Lifetime

Now with ViCLs

Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
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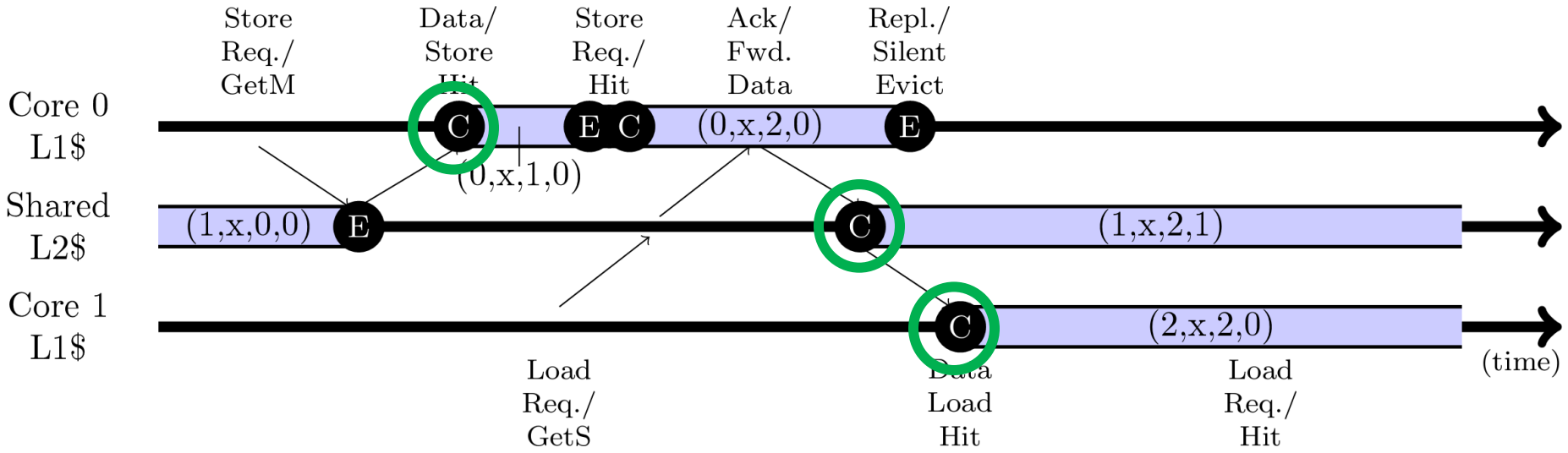

ViCL Nodes

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ViCL (cache id, addr, data, gen. id)

ViCL: Value in Cache Lifetime

Now with ViCLs

Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
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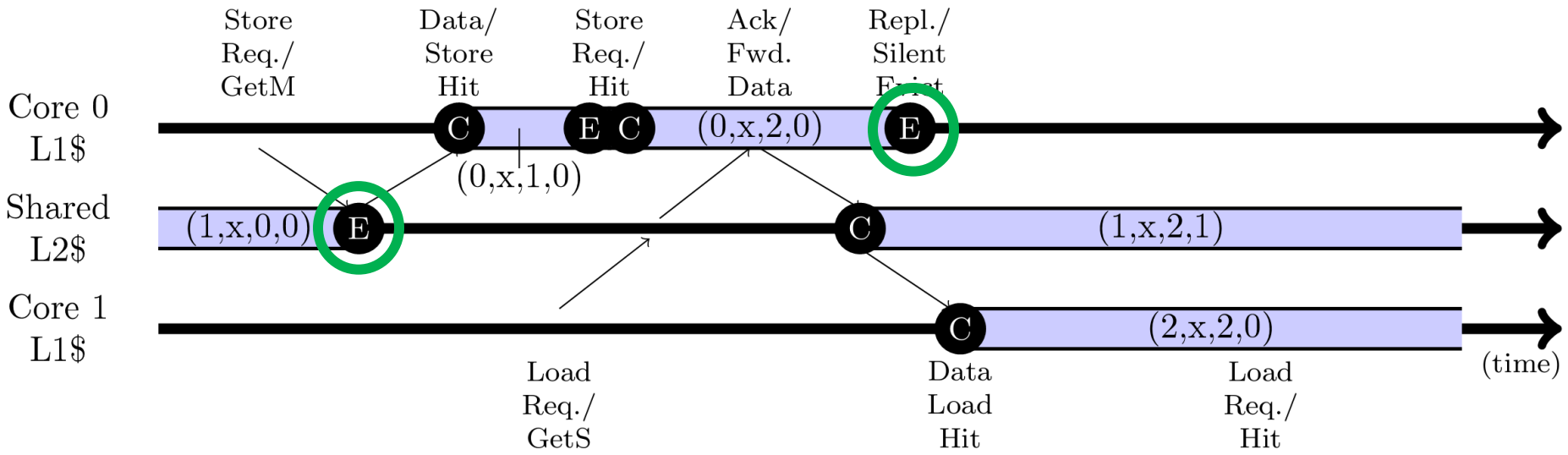

ViCL Nodes

C ViCL Create

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ViCL (cache id, addr, data, gen. id)

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Now with ViCLs

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Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
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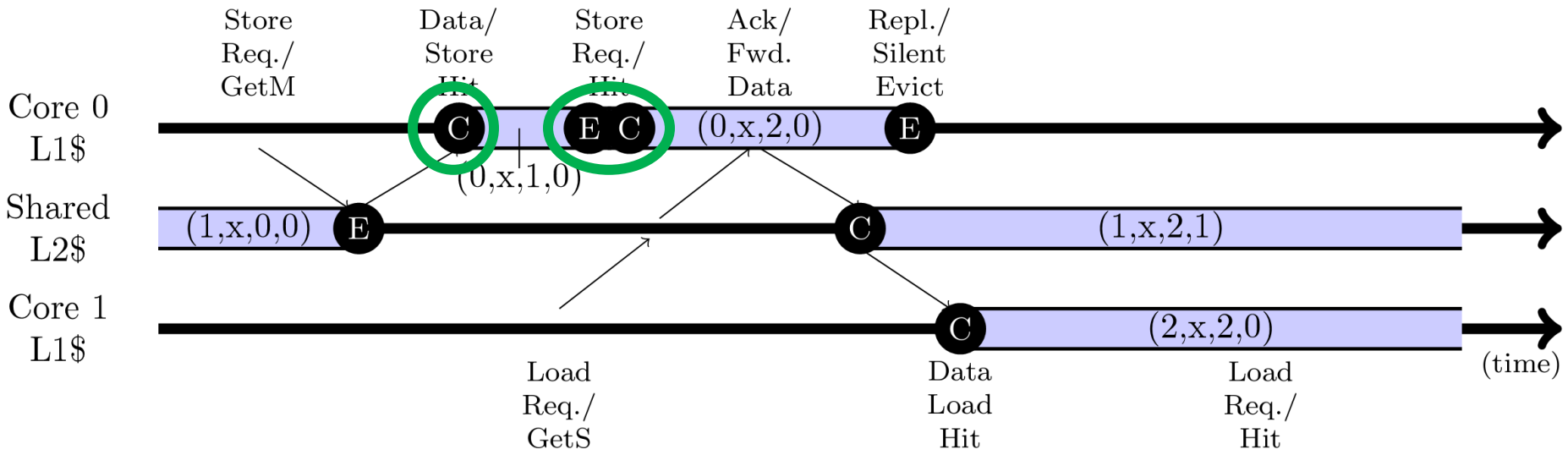

ViCL Nodes

C ViCL Create

E ViCL Expire

ViCL (cache id, addr, data, gen. id)

ViCL: Value in Cache Lifetime

Can model requests, downgrades, etc.

Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
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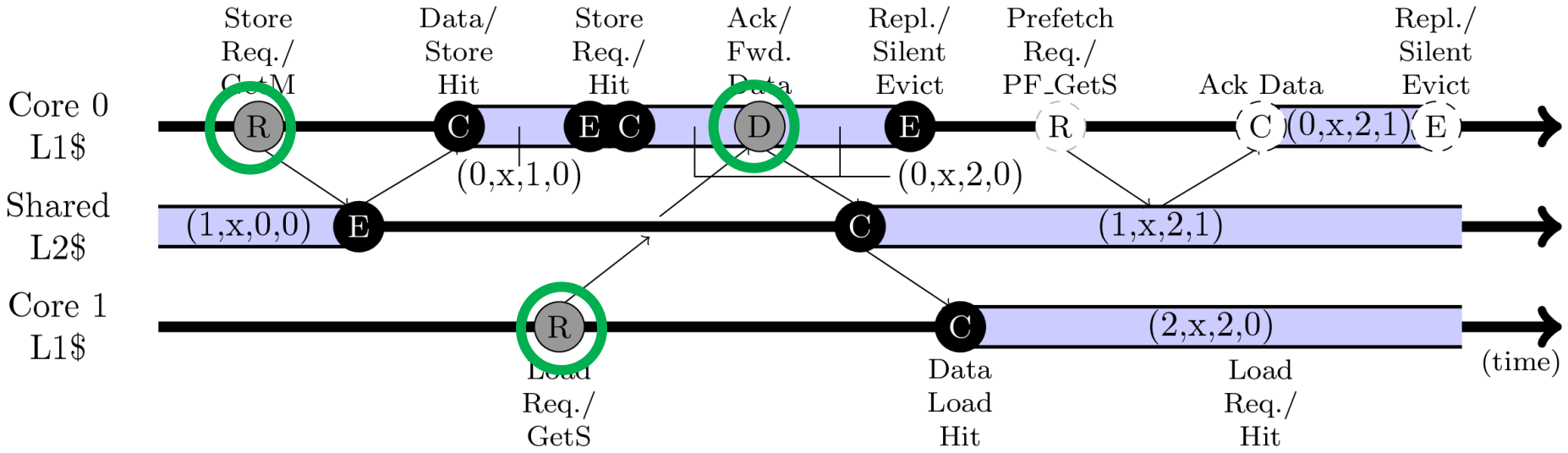


Always Enumerated

C ViCL Create

E ViCL Expire

Enumerated as Needed

R $ Line Request

D $ Line Downgrade

Not Enumerated

C ViCL Create

E ViCL Expire

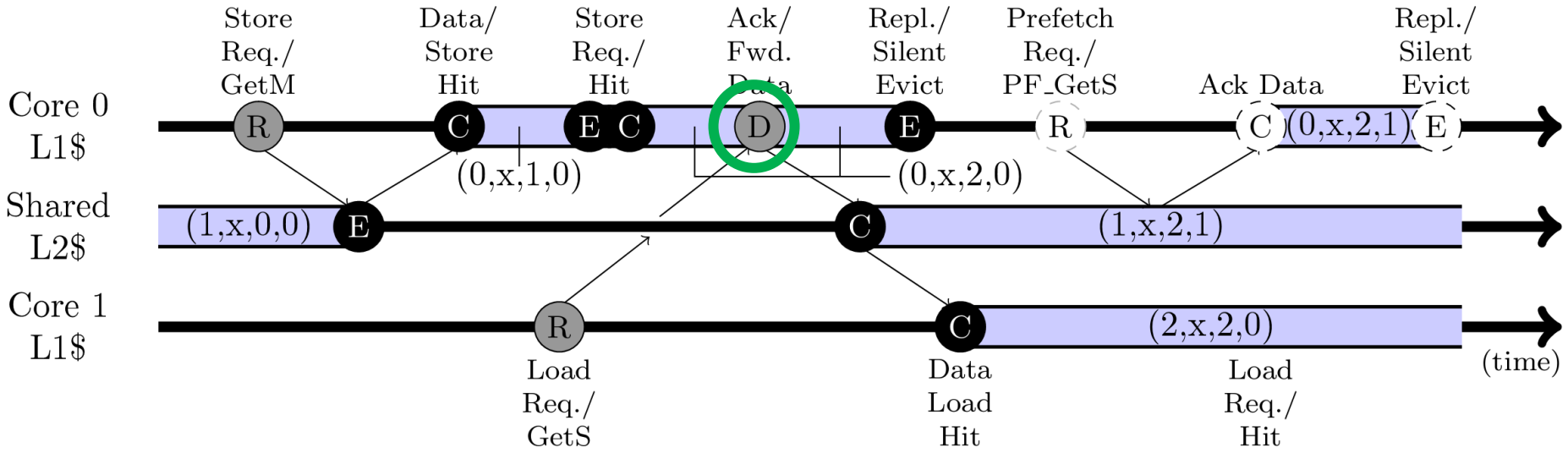
R $ Line Request

ViCL: Value in Cache Lifetime

Can model requests, downgrades, etc.

Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
(i2) St [x] ← 2	(i4) Ld r2 ← [x]
In TSO: r1=2, r2=2 Allowed	



Always Enumerated

C ViCL Create — E ViCL Expire

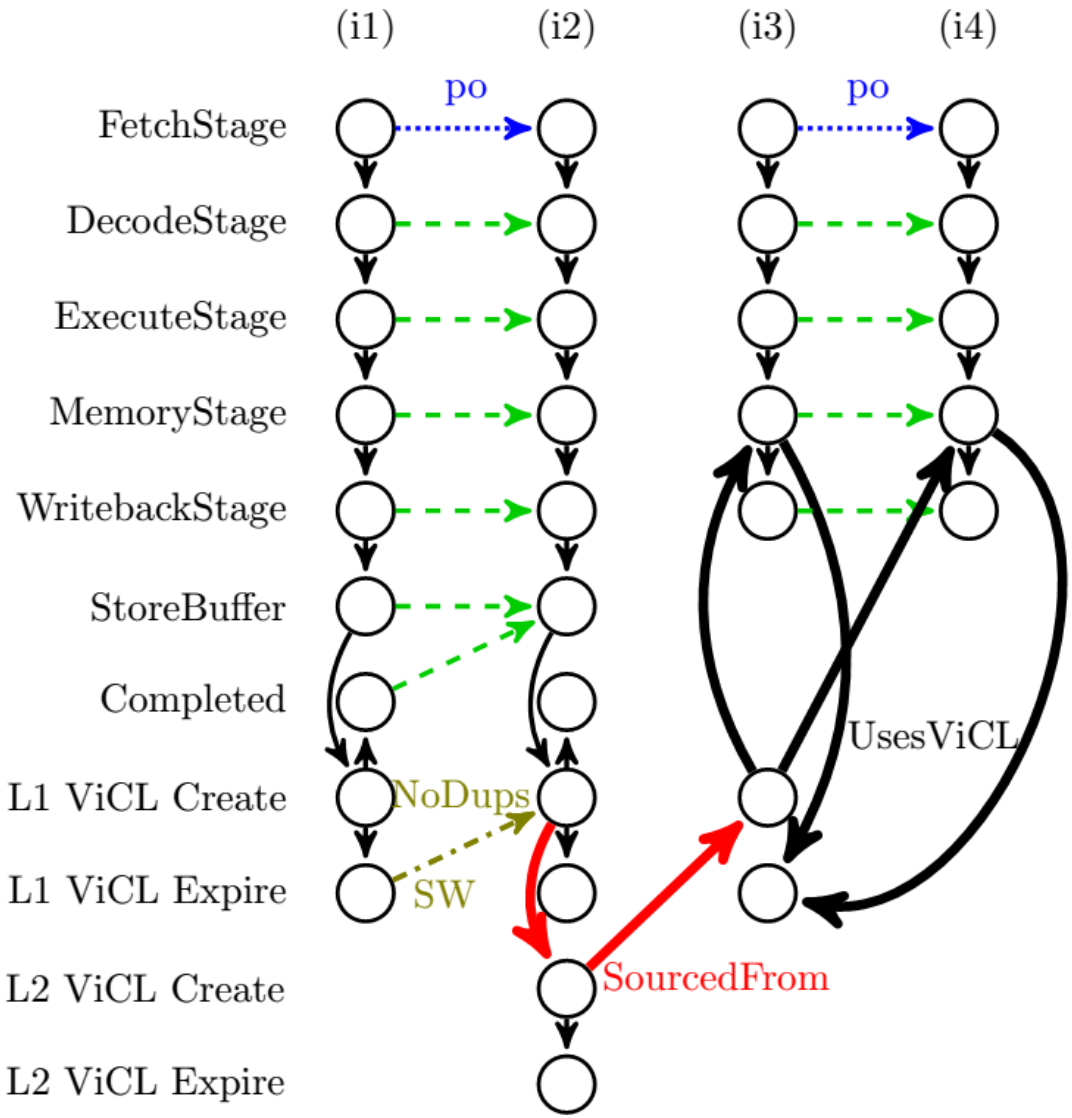
Enumerated as Needed

R $ Line Request — D $ Line Downgrade

Not Enumerated

(C) ViCL Create — (E) ViCL Expire — (R) $ Line Request

ViCLs in μhb Graphs



Litmus Test **co-mp**

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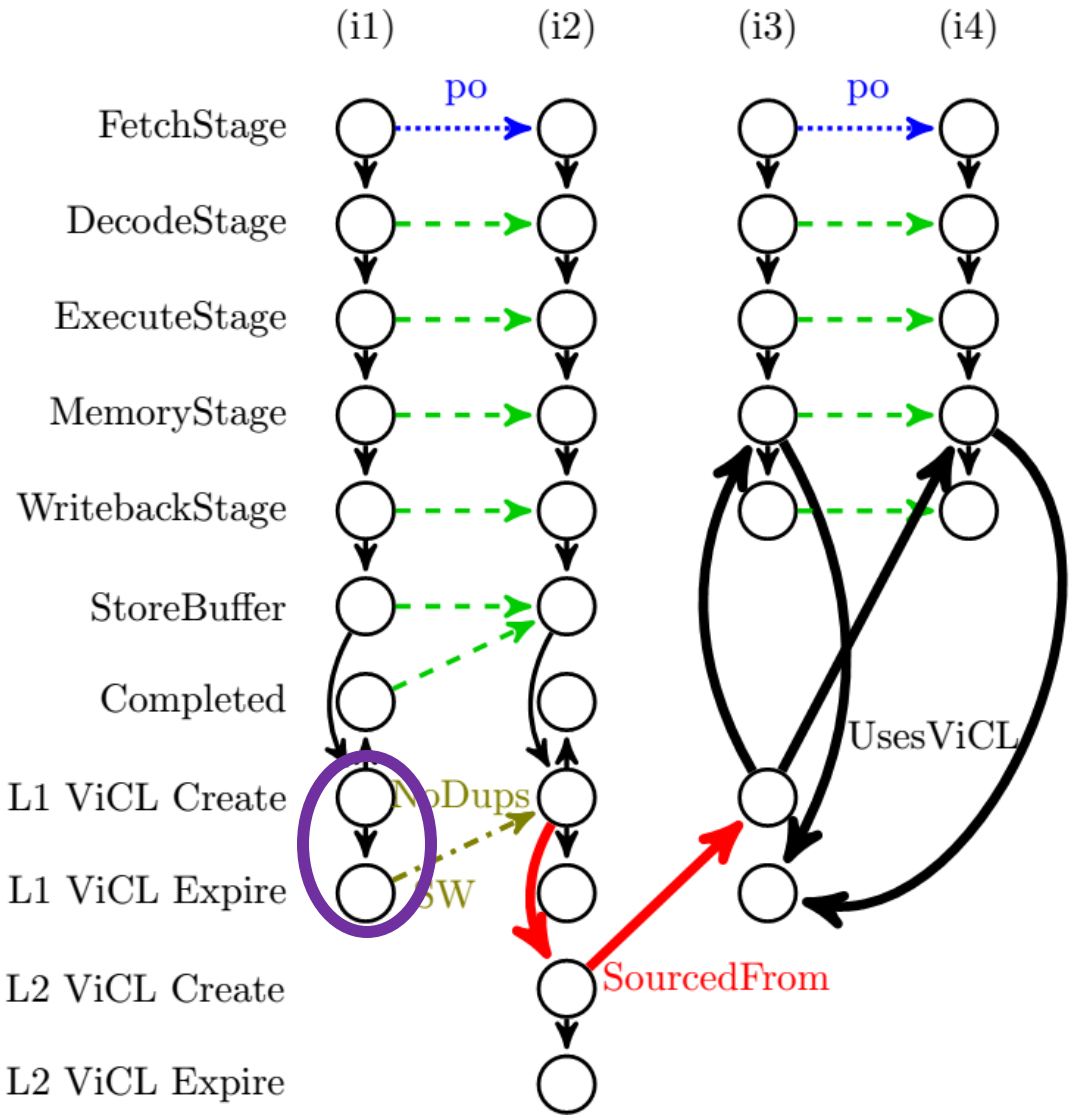
(i1) St [x] ← 1 (i2) St [x] ← 2	(i3) Ld r1 ← [x] (i4) Ld r2 ← [x]
In TSO: r1=2, r2=2 Allowed	

- Use pipeline model from PipeCheck, but add ViCL nodes and edges

ViCLs in μhb Graphs

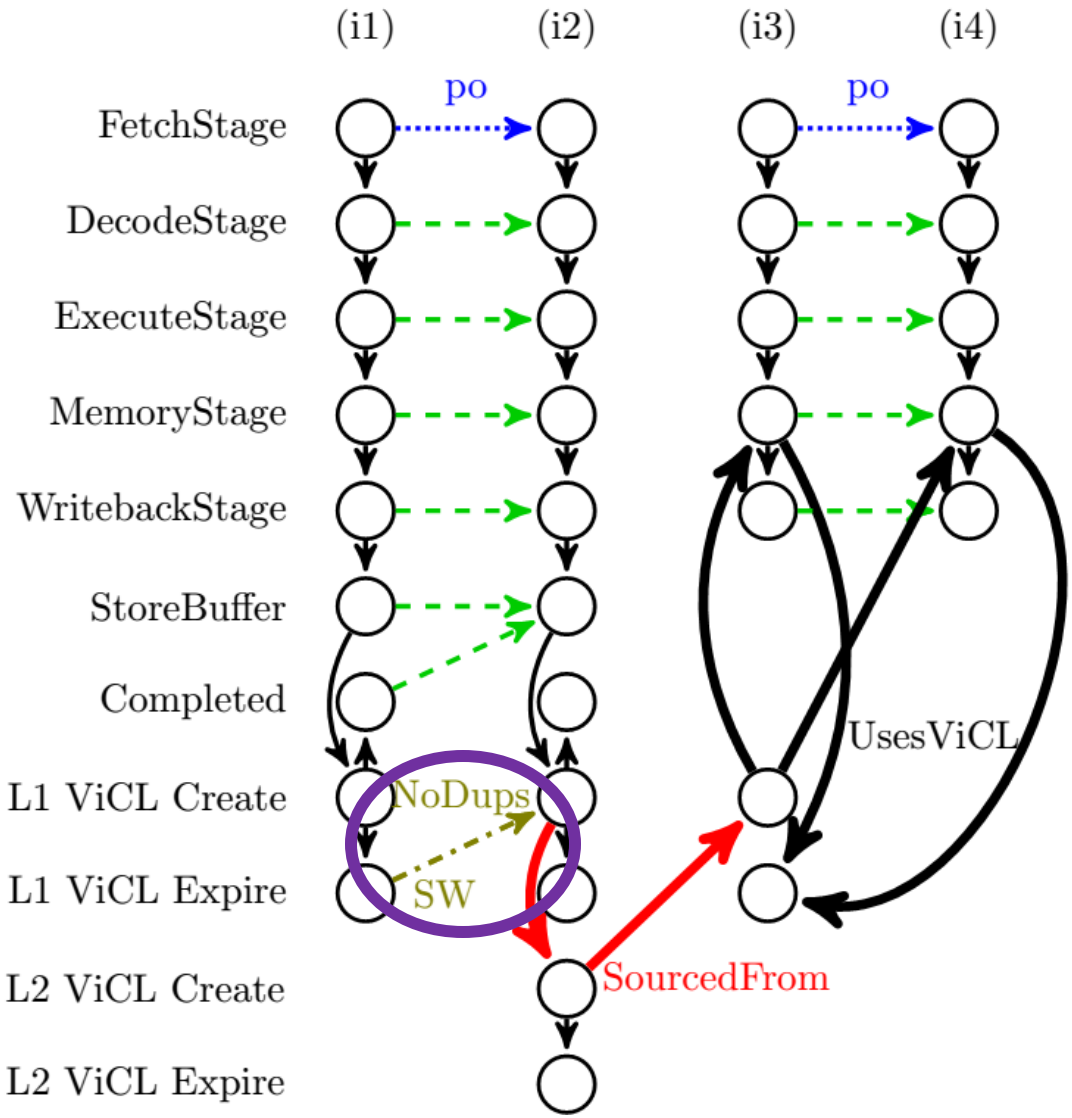


Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1 (i2) St [x] ← 2	(i3) Ld r1 ← [x] (i4) Ld r2 ← [x]
In TSO: r1=2, r2=2 Allowed	

- Use pipeline model from PipeCheck, but add ViCL nodes and edges

ViCLs in μhb Graphs



Litmus Test **co-mp**

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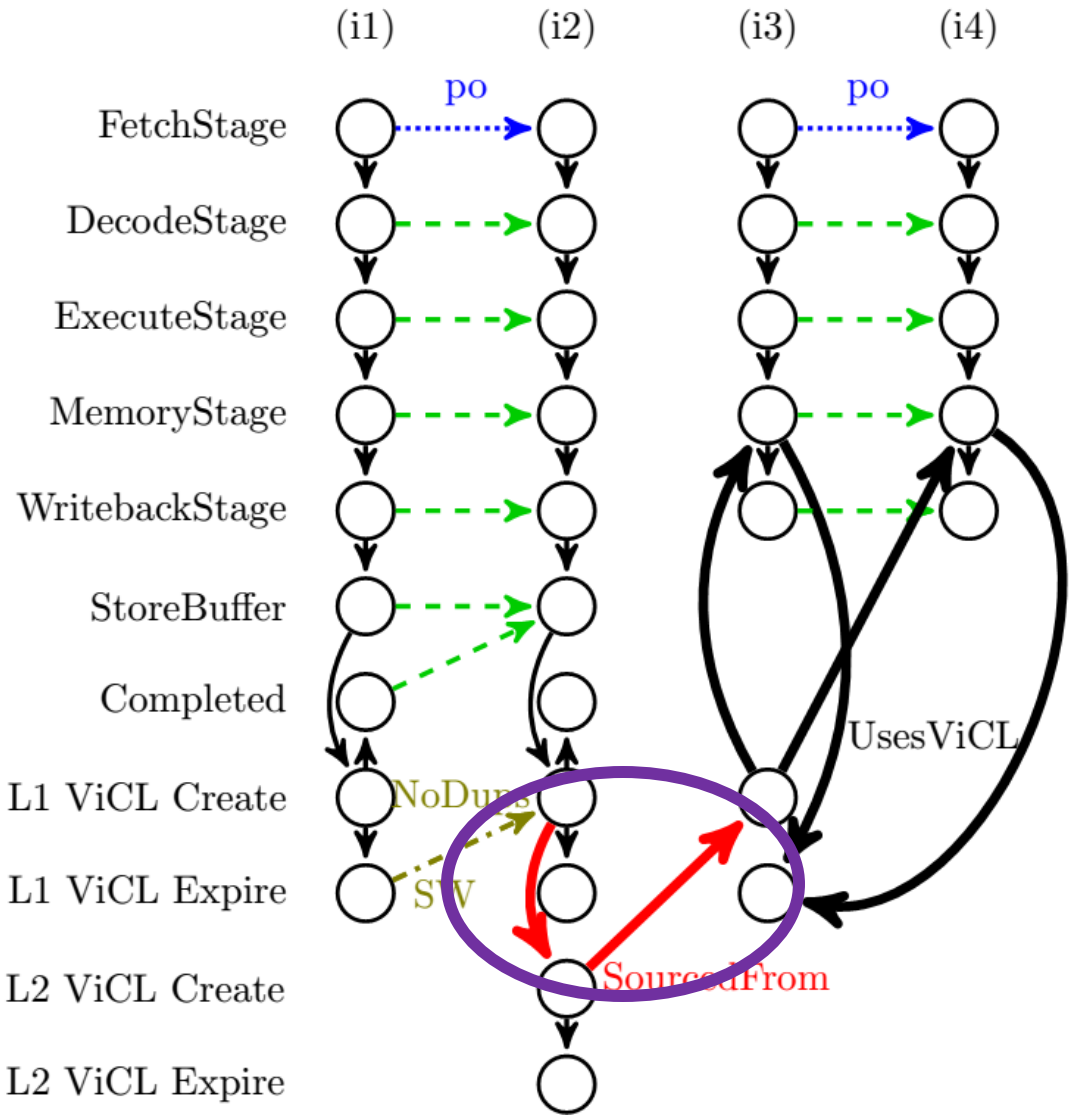
In TSO: r1=2, r2=2 Allowed	

- Use pipeline model from PipeCheck, but add ViCL nodes and edges

ViCLs in μhb Graphs

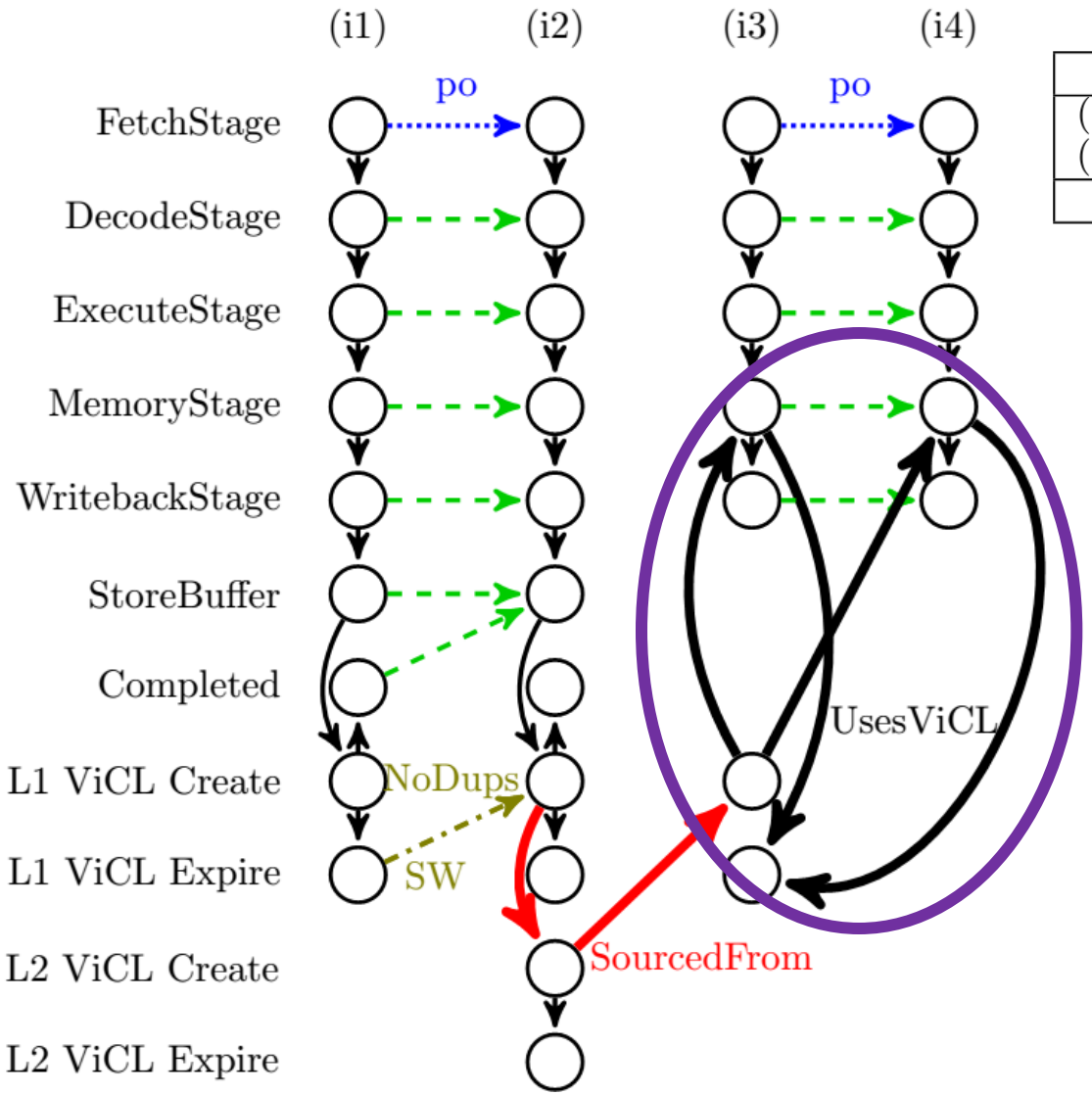


Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1 (i2) St [x] ← 2	(i3) Ld r1 ← [x] (i4) Ld r2 ← [x]
In TSO: r1=2, r2=2 Allowed	

- Use pipeline model from PipeCheck, but add ViCL nodes and edges

ViCLs in μhb Graphs

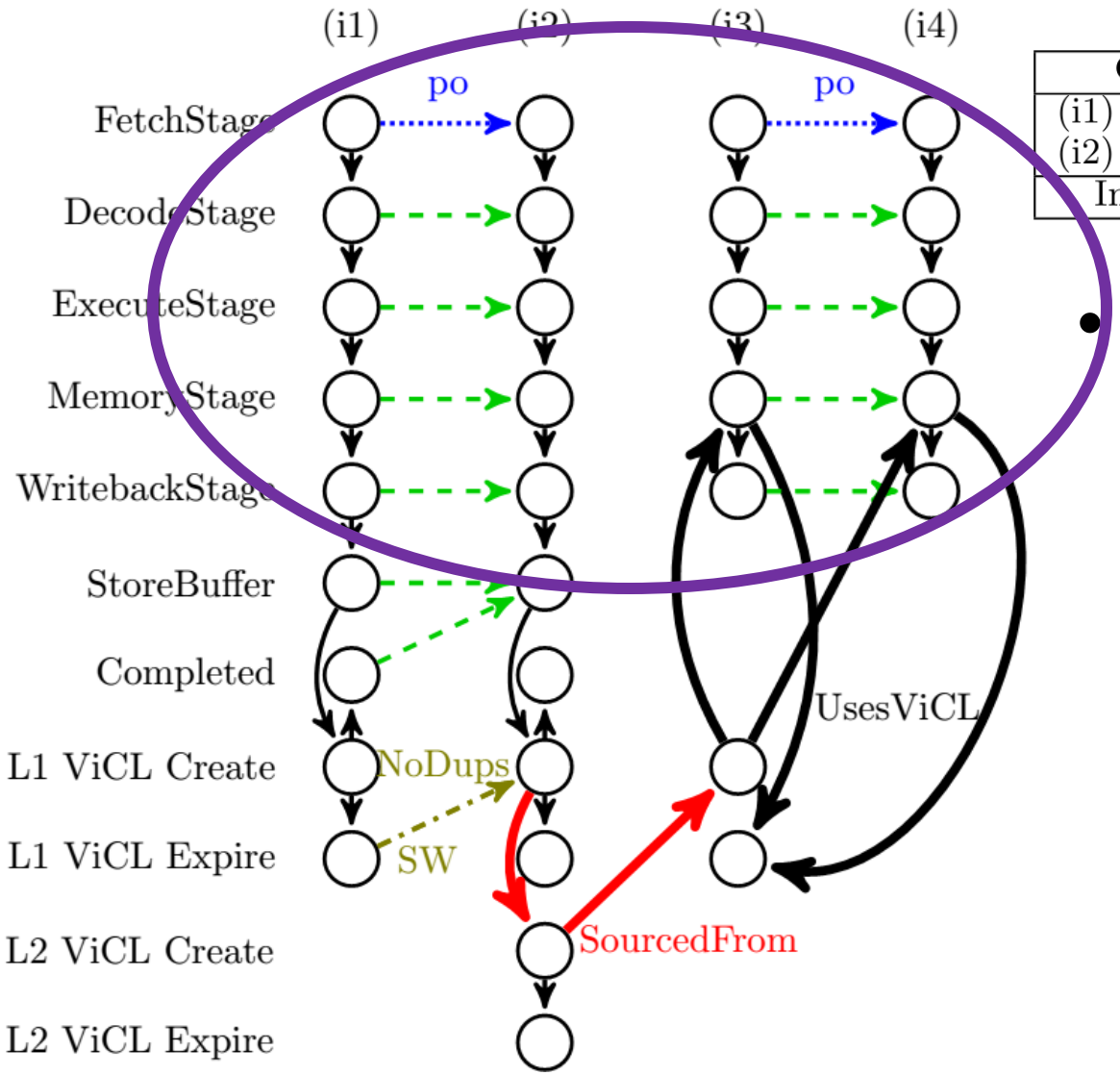


Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1 (i2) St [x] ← 2	(i3) Ld r1 ← [x] (i4) Ld r2 ← [x]
In TSO: r1=2, r2=2 Allowed	

- Use pipeline model from PipeCheck, but add ViCL nodes and edges

ViCLs in μhb Graphs



Litmus Test **co-mp**

Core 0	Core 1
(i1) St [x] ← 1	(i3) Ld r1 ← [x]
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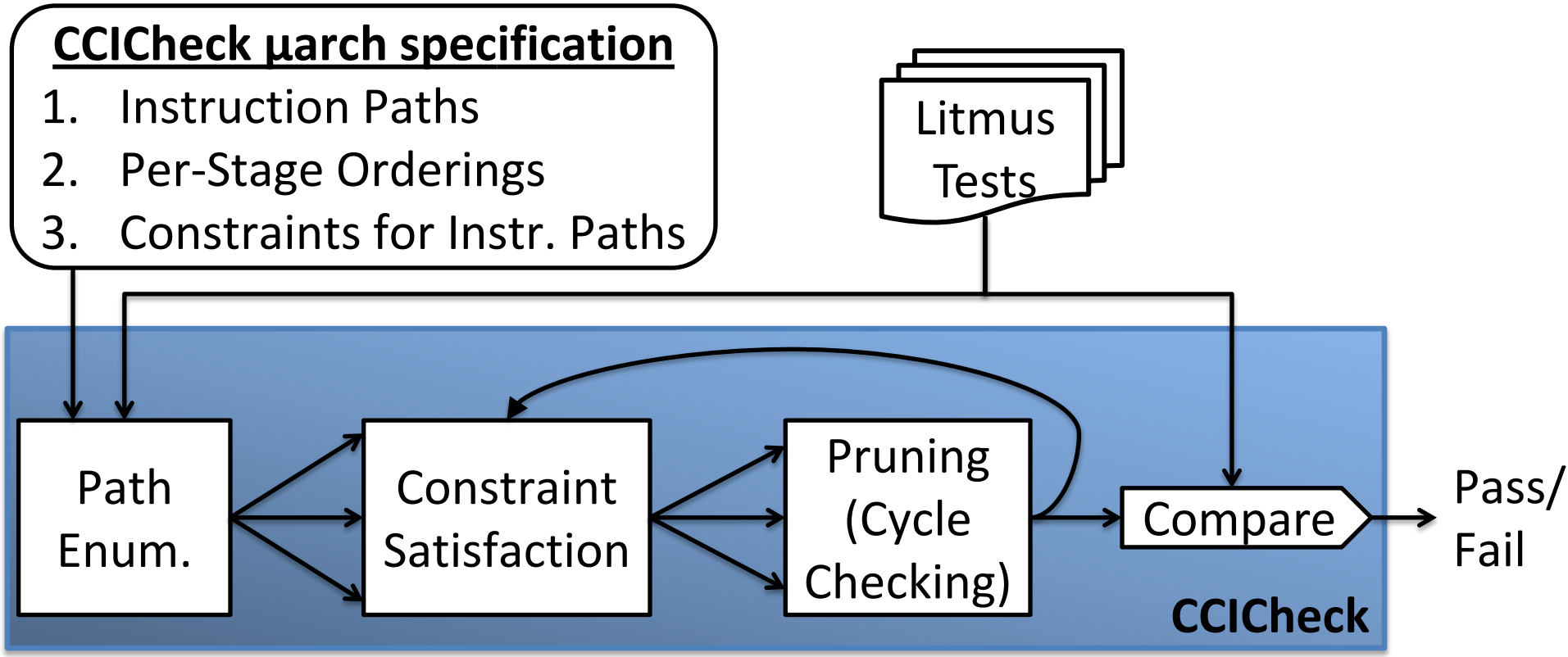
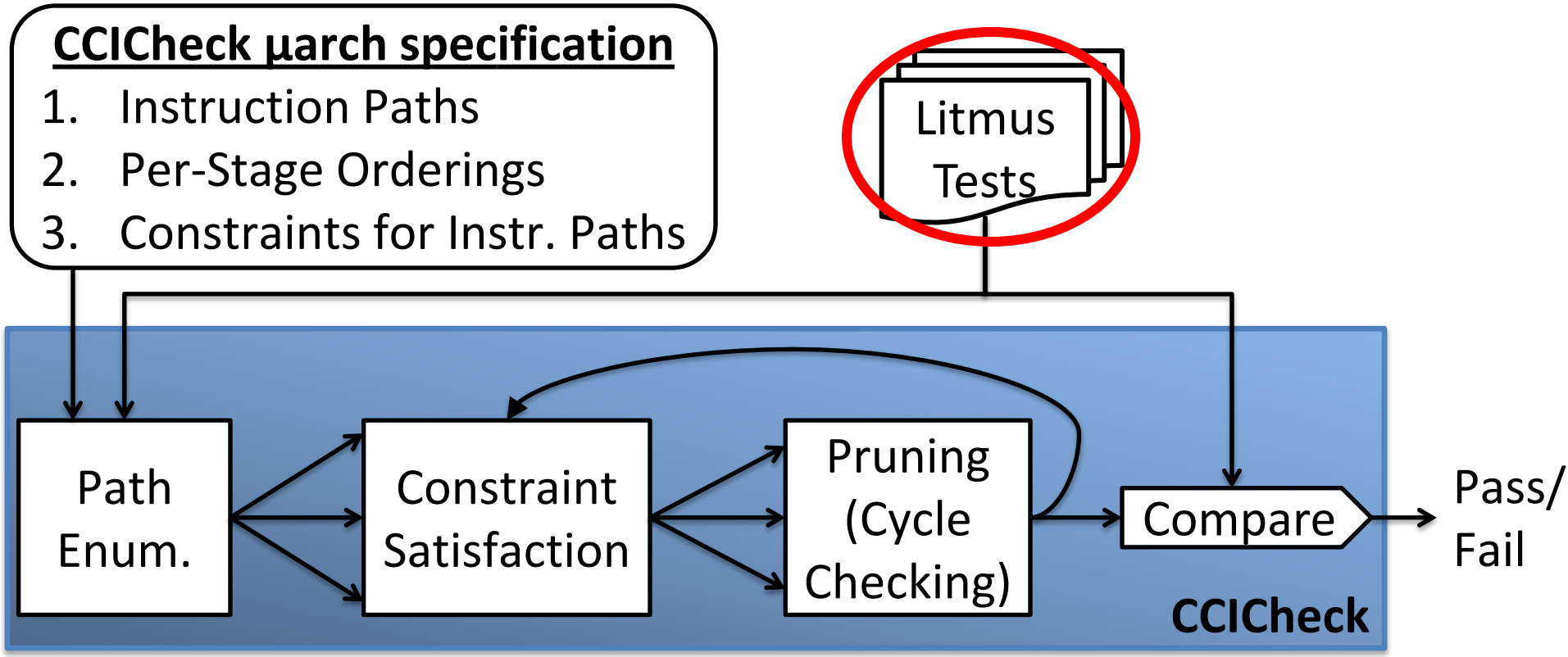
- Use pipeline model from PipeCheck, but add ViCL nodes and edges

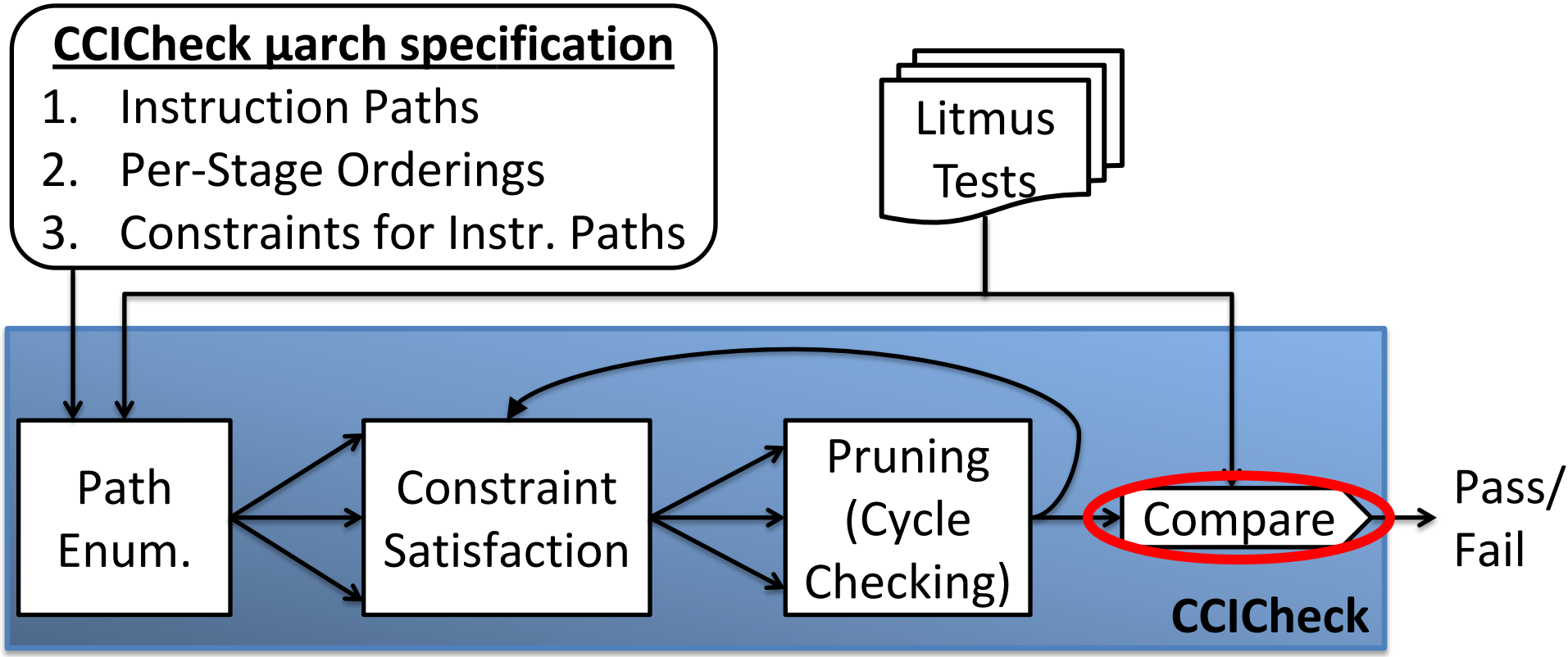
CCICheck Toolflow



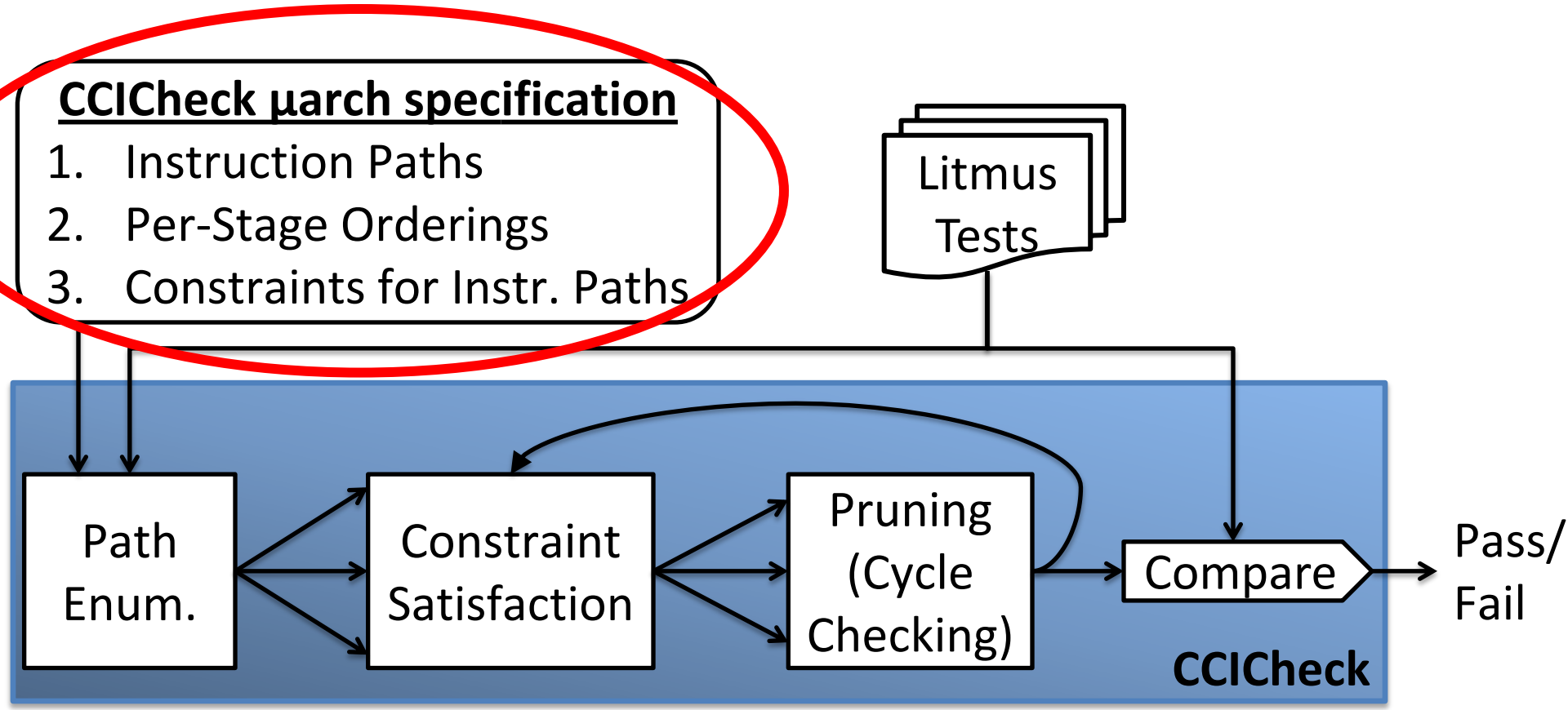
CCICheck Toolflow



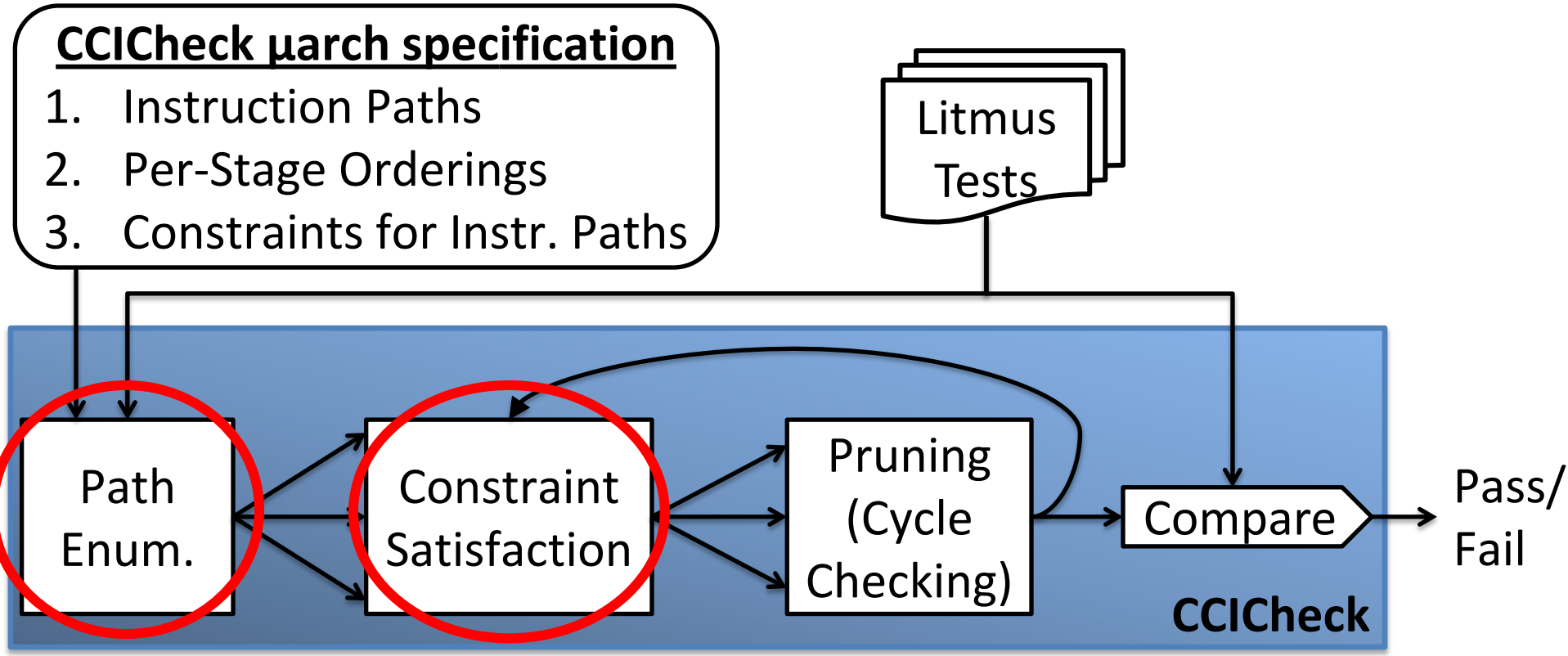
CCICheck Toolflow



CCICheck Toolflow



CCICheck Toolflow



Path Enumeration

Thread	
(i1)	St [x] ← 1
(i2)	Ld r1 ← [x]
(i3)	Ld r2 ← [x]
Allowed: r1=1, r2=1	

Constraint Satisfaction

Path Enumeration

Thread	
(i1)	St [x] ← 1
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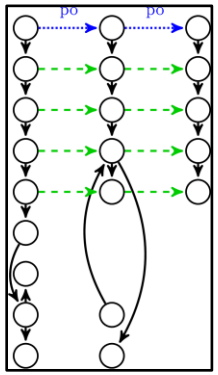
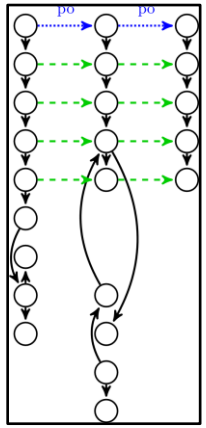
Allowed: r1=1, r2=1	





Constraint Satisfaction

Path Enumeration

Thread	
(i1)	St [x] ← 1
(i2)	Ld r1 ← [x]
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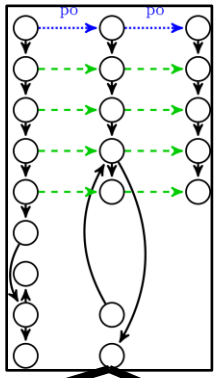
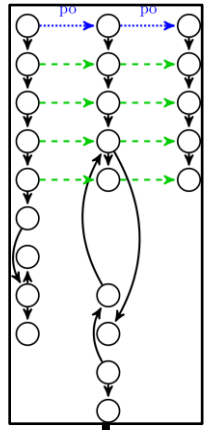
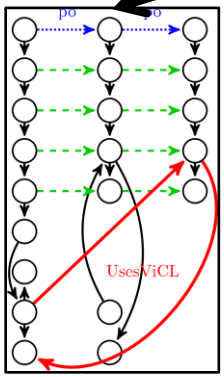
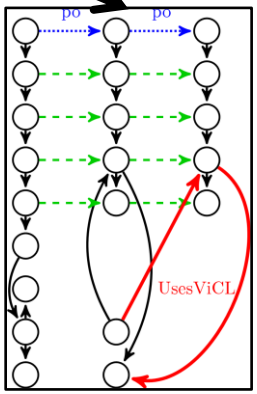
Allowed: r1=1, r2=1	

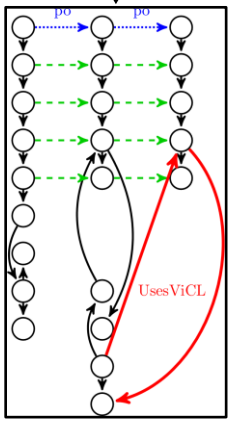




Constraint Satisfaction







Path Enumeration

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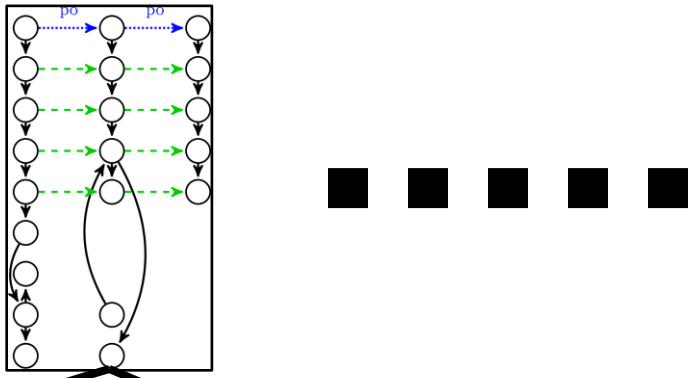
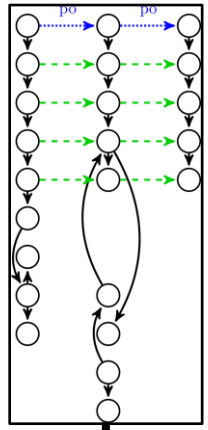
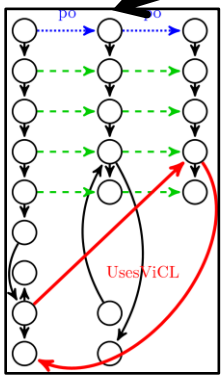
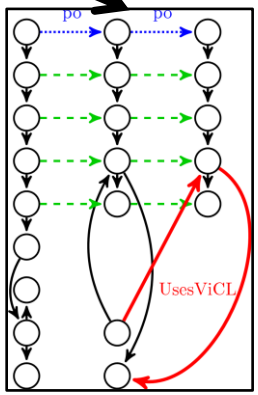
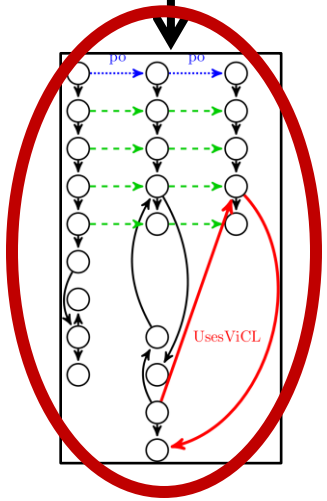




Constraint Satisfaction







Path Enumeration

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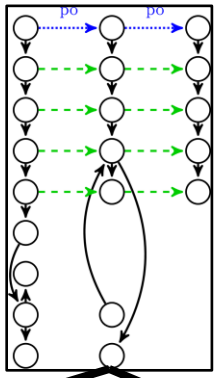
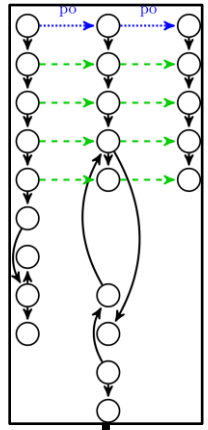
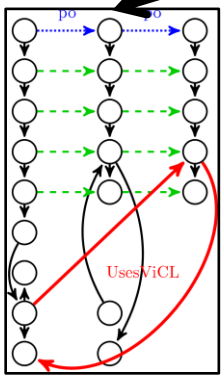
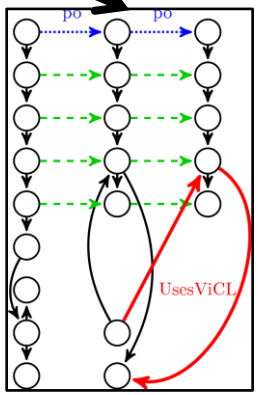
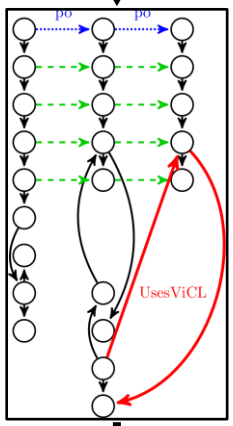




Constraint Satisfaction







Unsatisfiable Constraint → Invalid Scenario

Path Enumeration

Thread	
(i1)	St [x] ← 1
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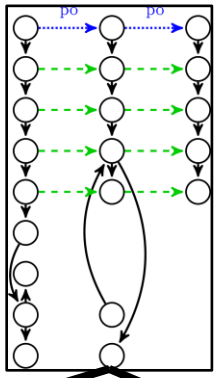
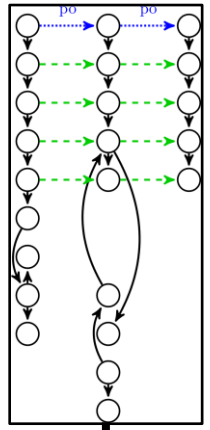
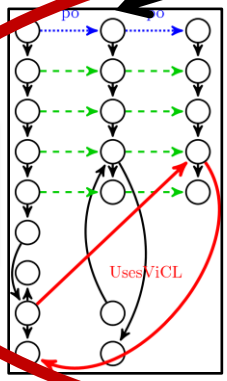
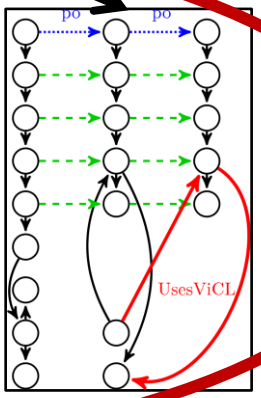
(i3)	Ld r2 ← [x]
Allowed: r1=1, r2=1	

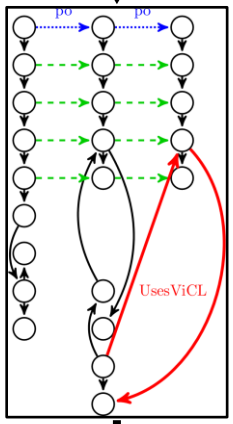




Constraint Satisfaction







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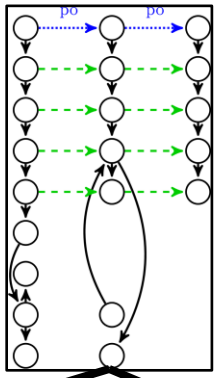
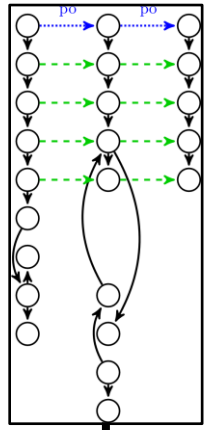
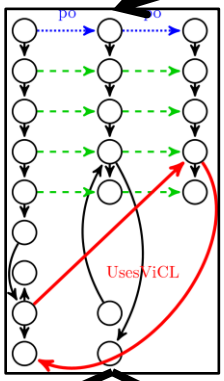
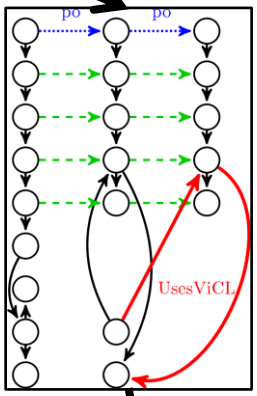
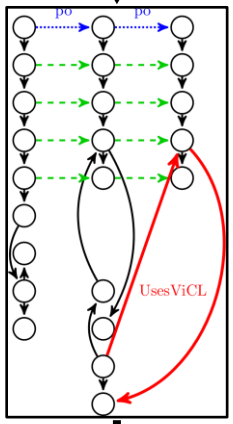


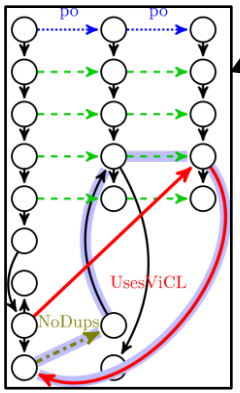


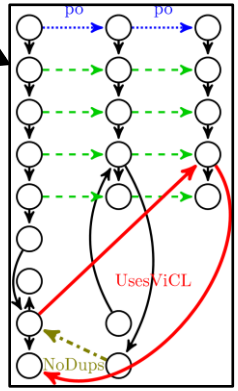
Constraint Satisfaction











Unsatisfiable Constraint → Invalid Scenario

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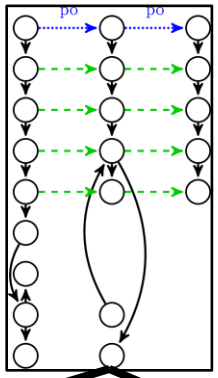
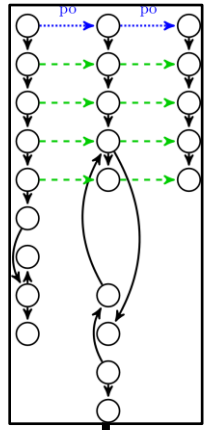
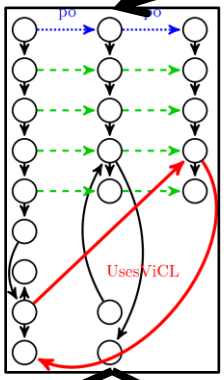
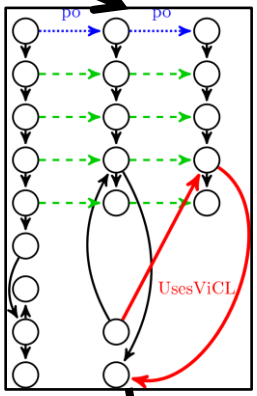
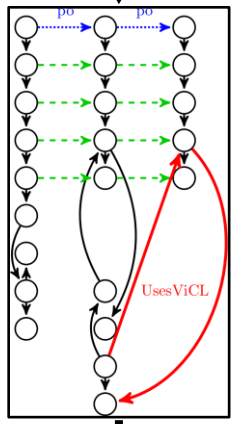


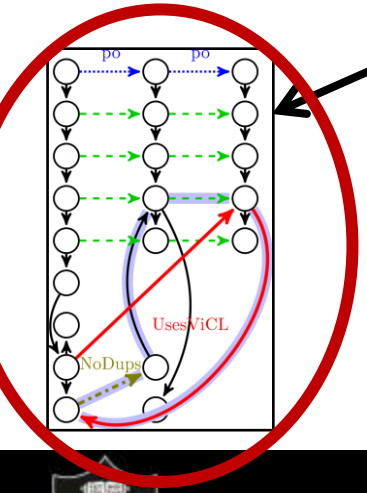


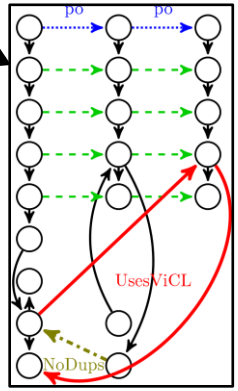
Constraint Satisfaction











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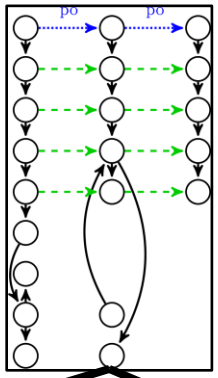

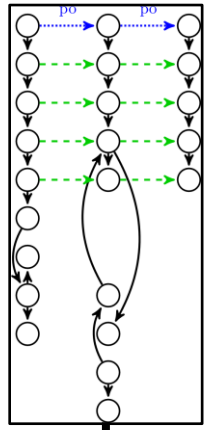

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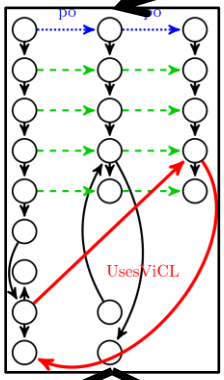
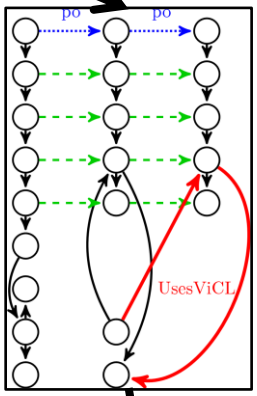
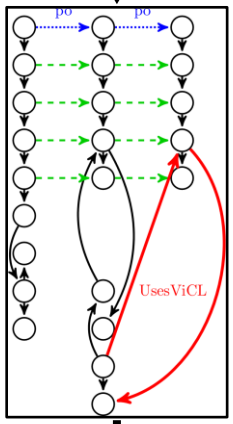
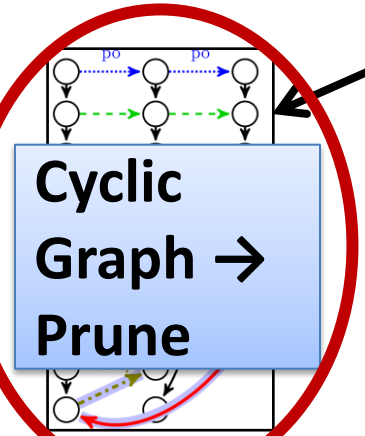
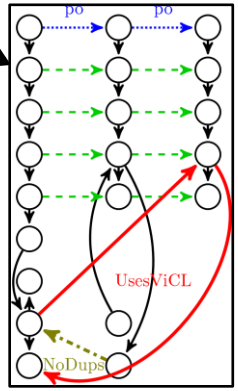








Cyclic Graph → Prune



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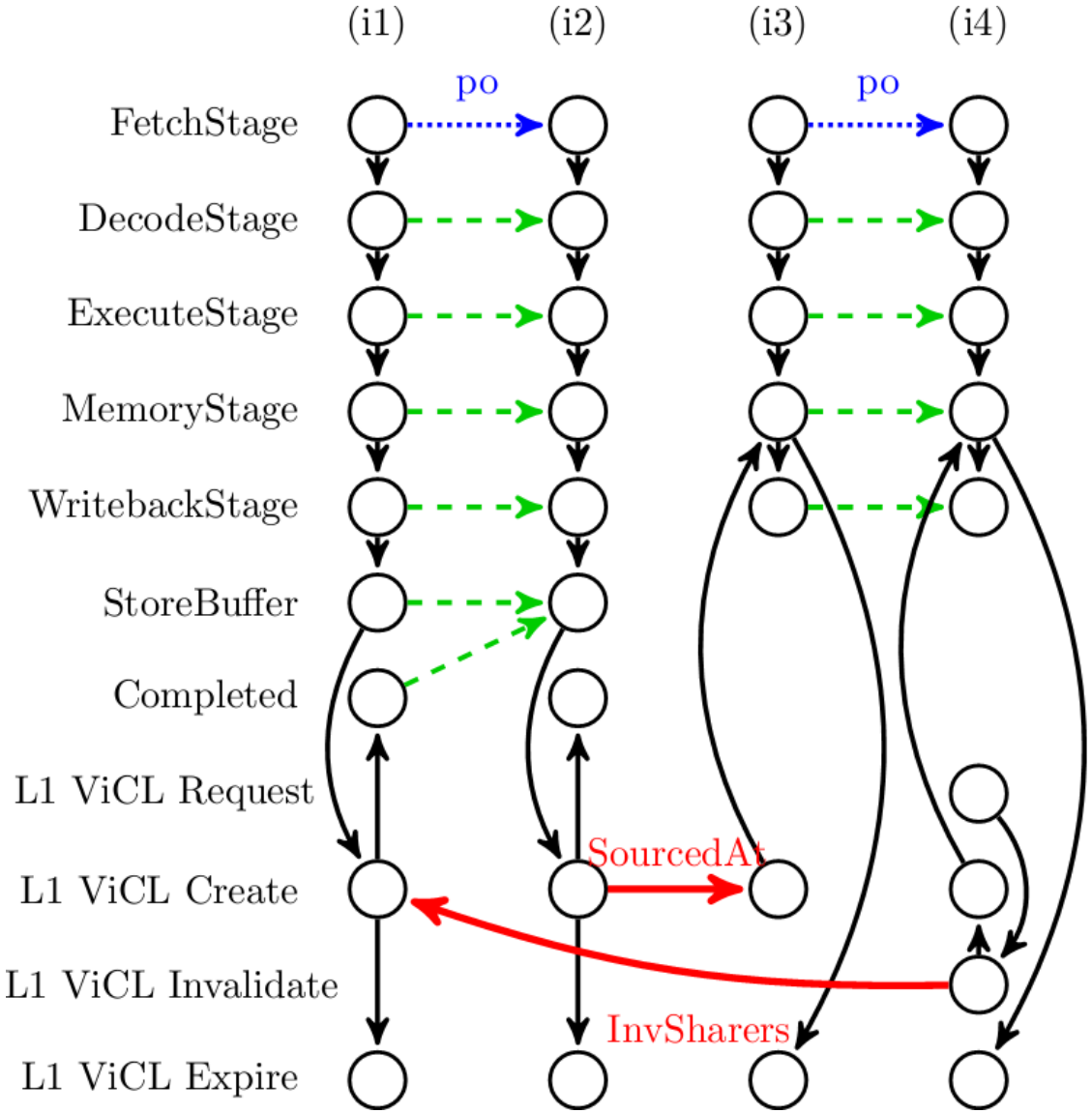
Case Studies and Results

“Peekaboo”



- Livelock prevention mechanism allows use of stale data
- “Peekaboo” edge completes cycle => outcome forbidden
- Consistency maintained

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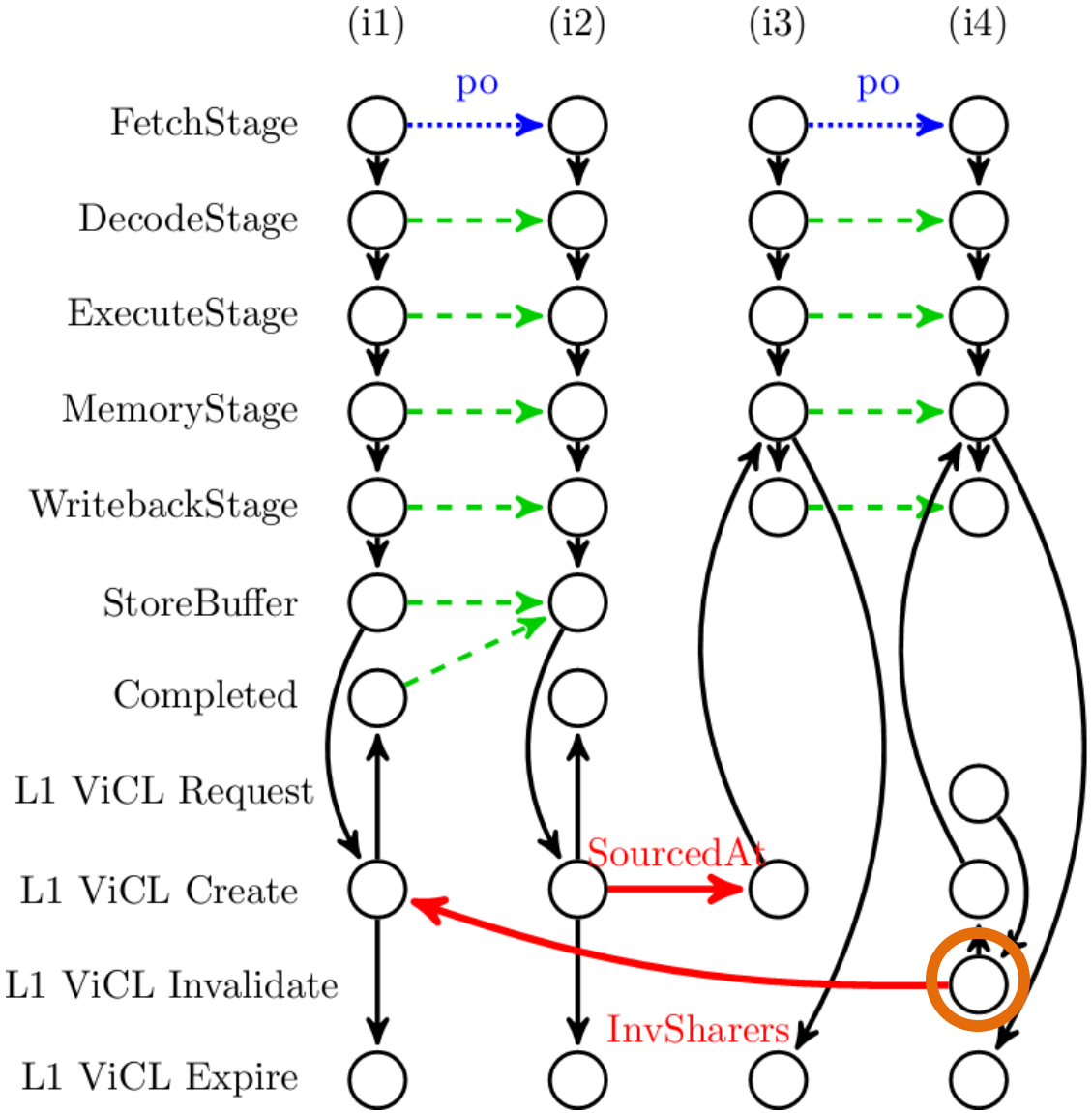

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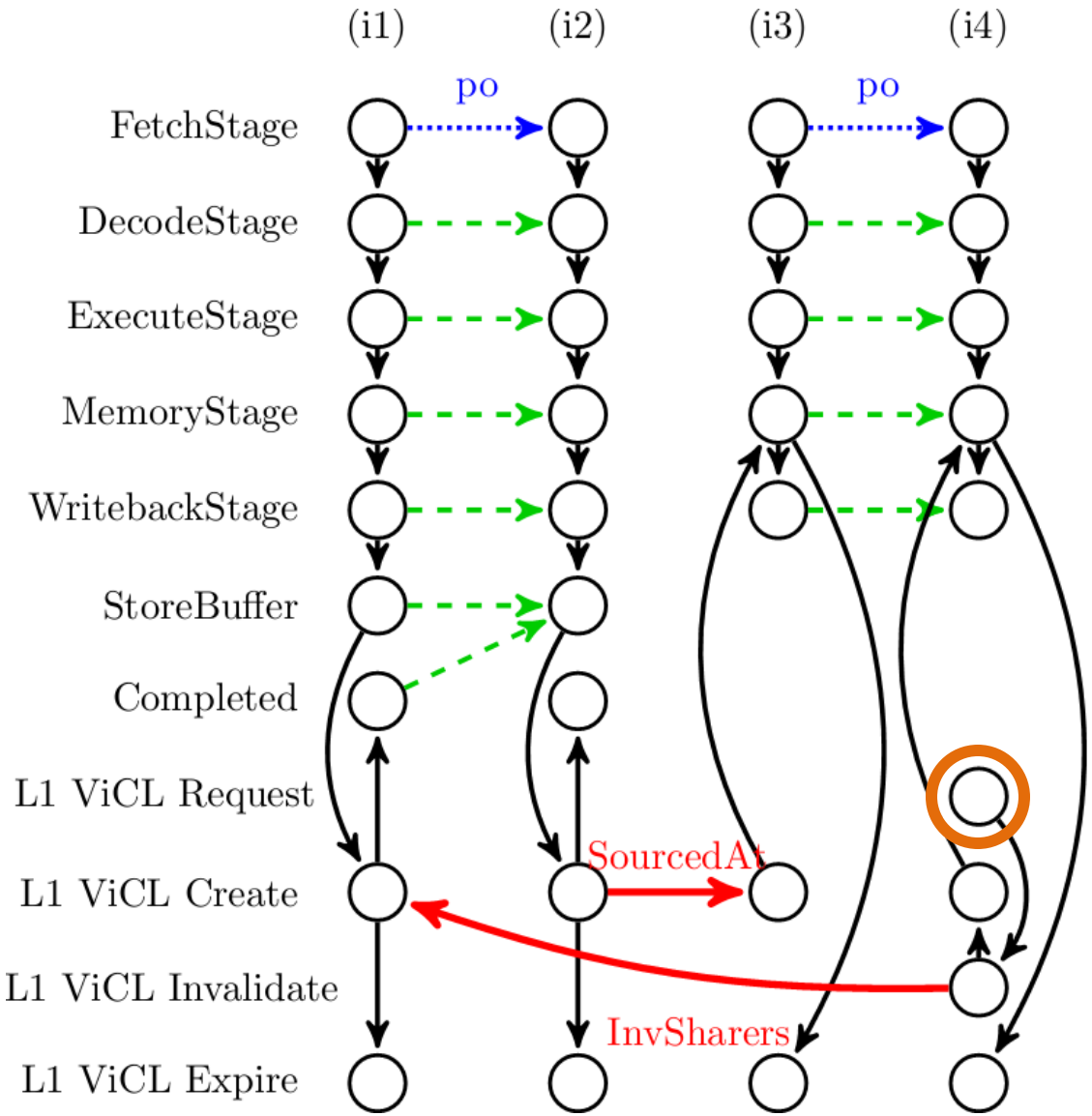

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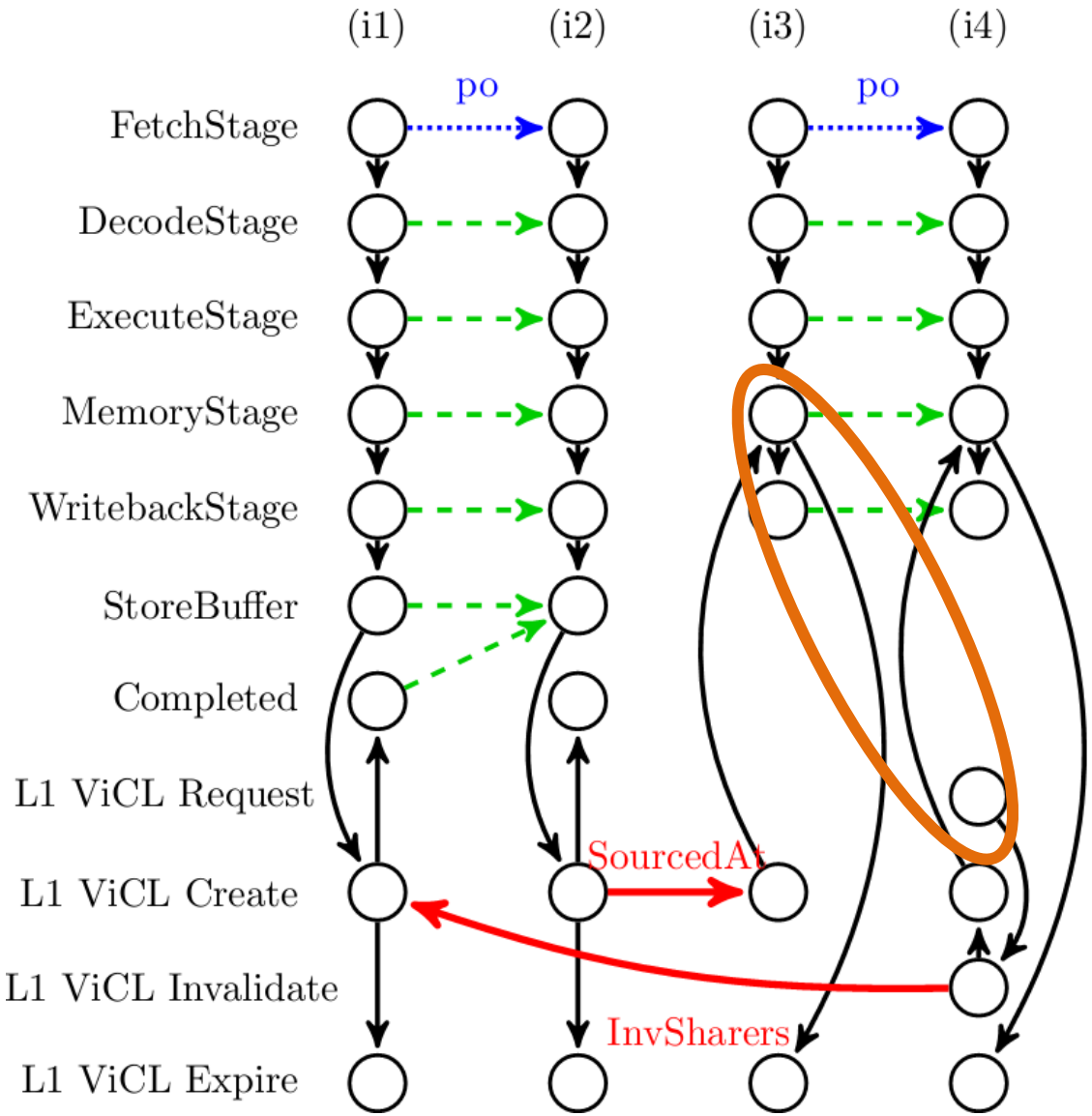

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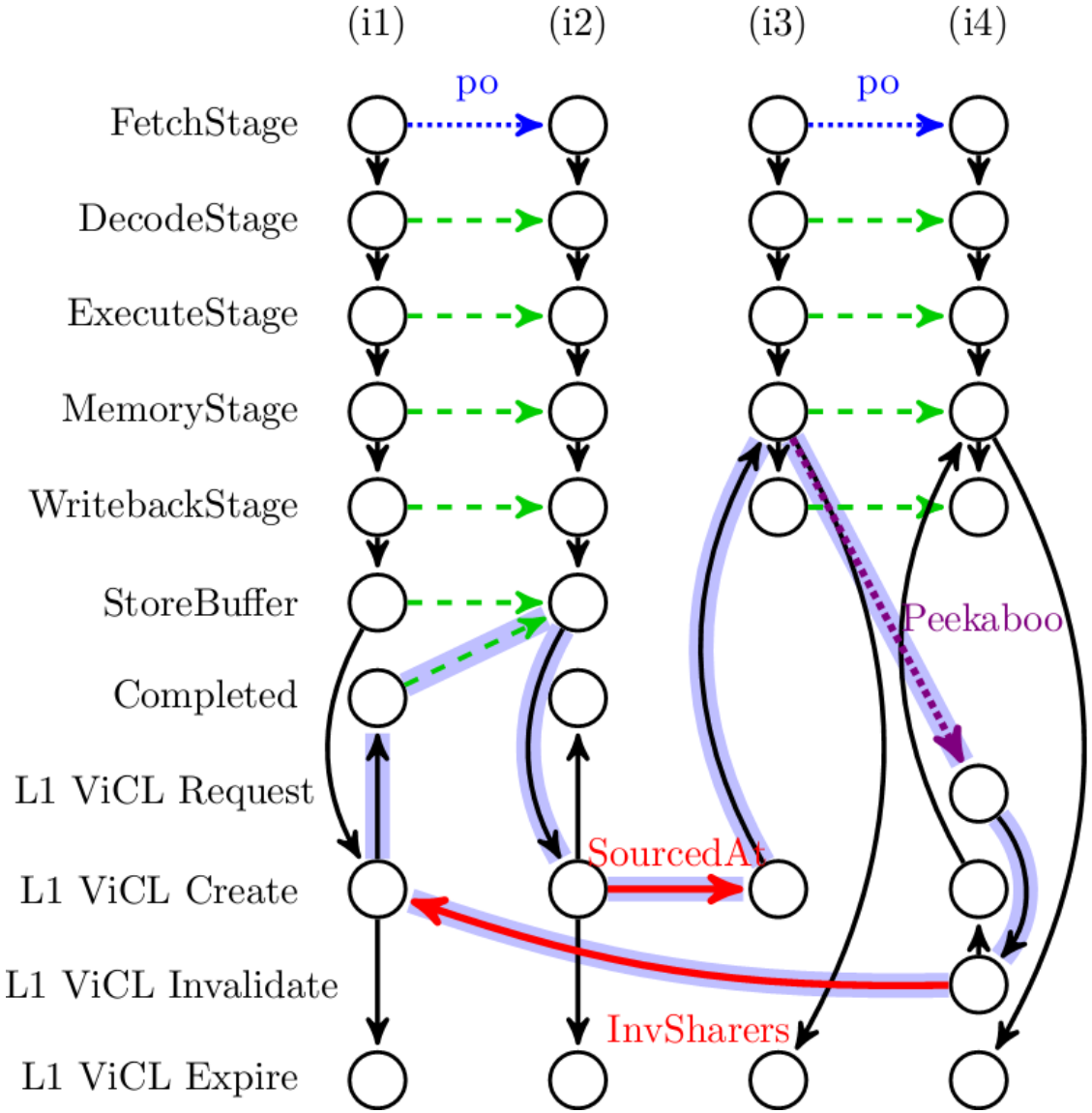

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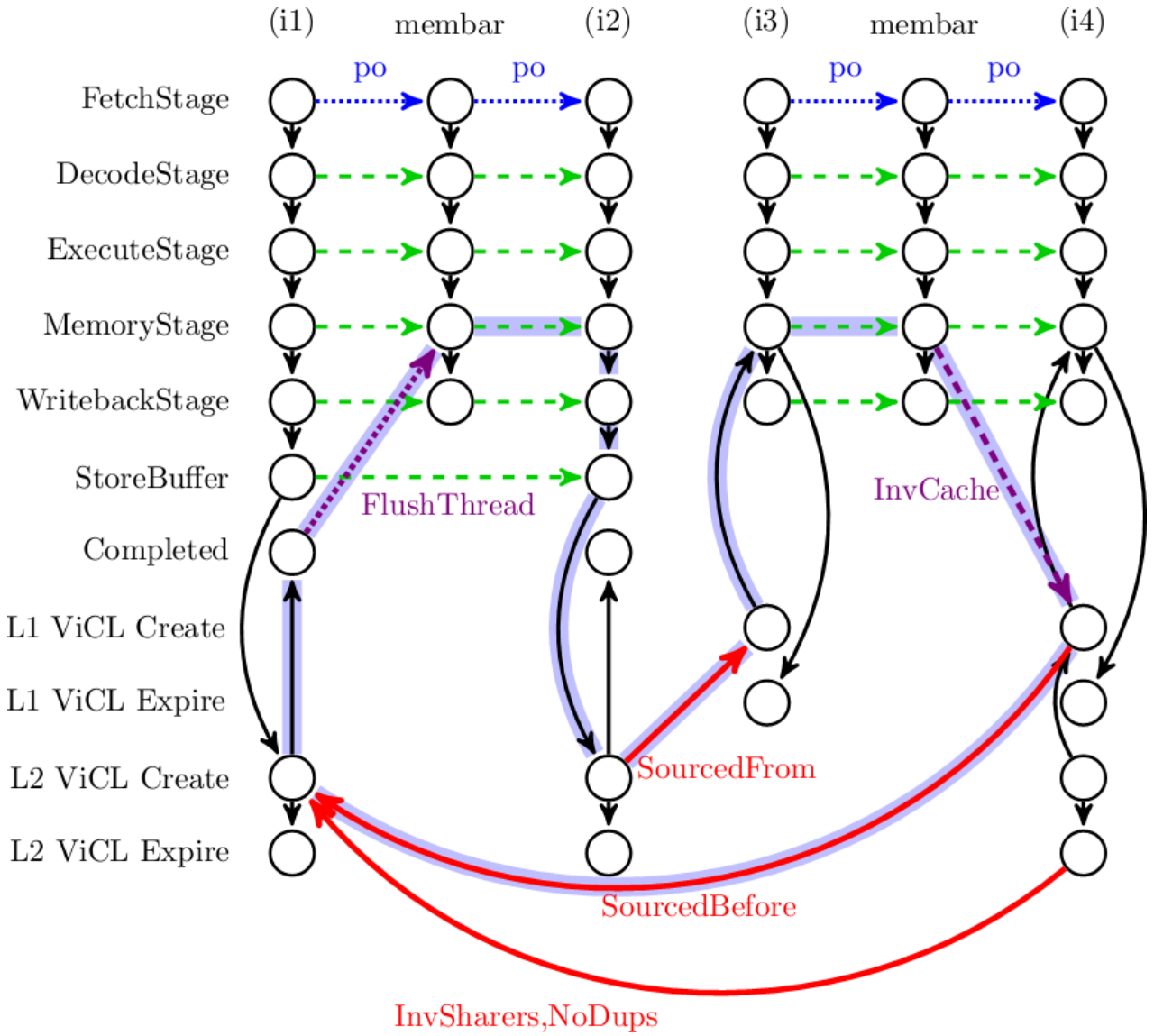
Partial Incoherence: GPUs



- e.g.: **`mp`** with membar fences [Alglave et al. ASPLOS15]
- If fence does not enforce **InvCache** ordering => no cycle

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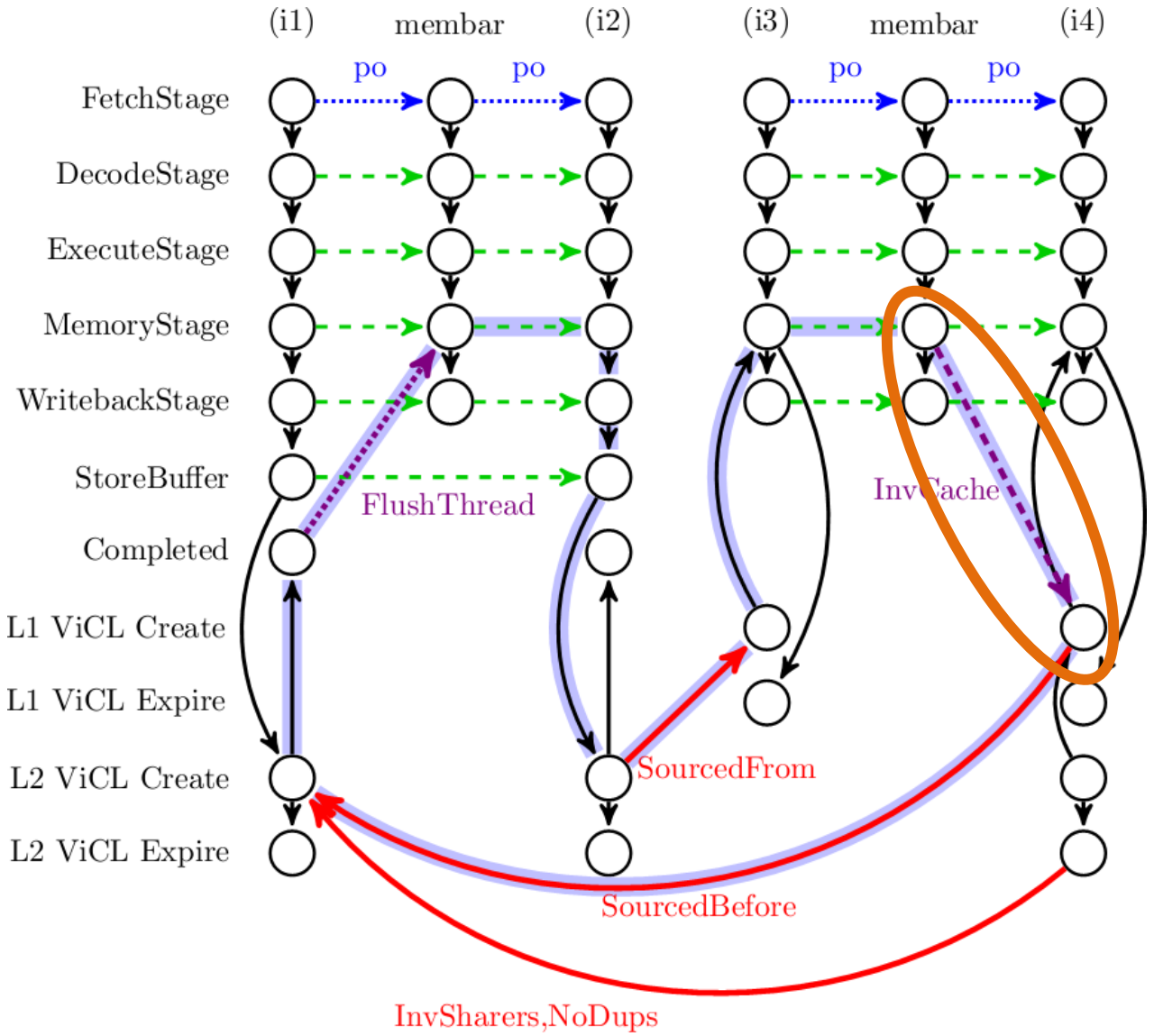

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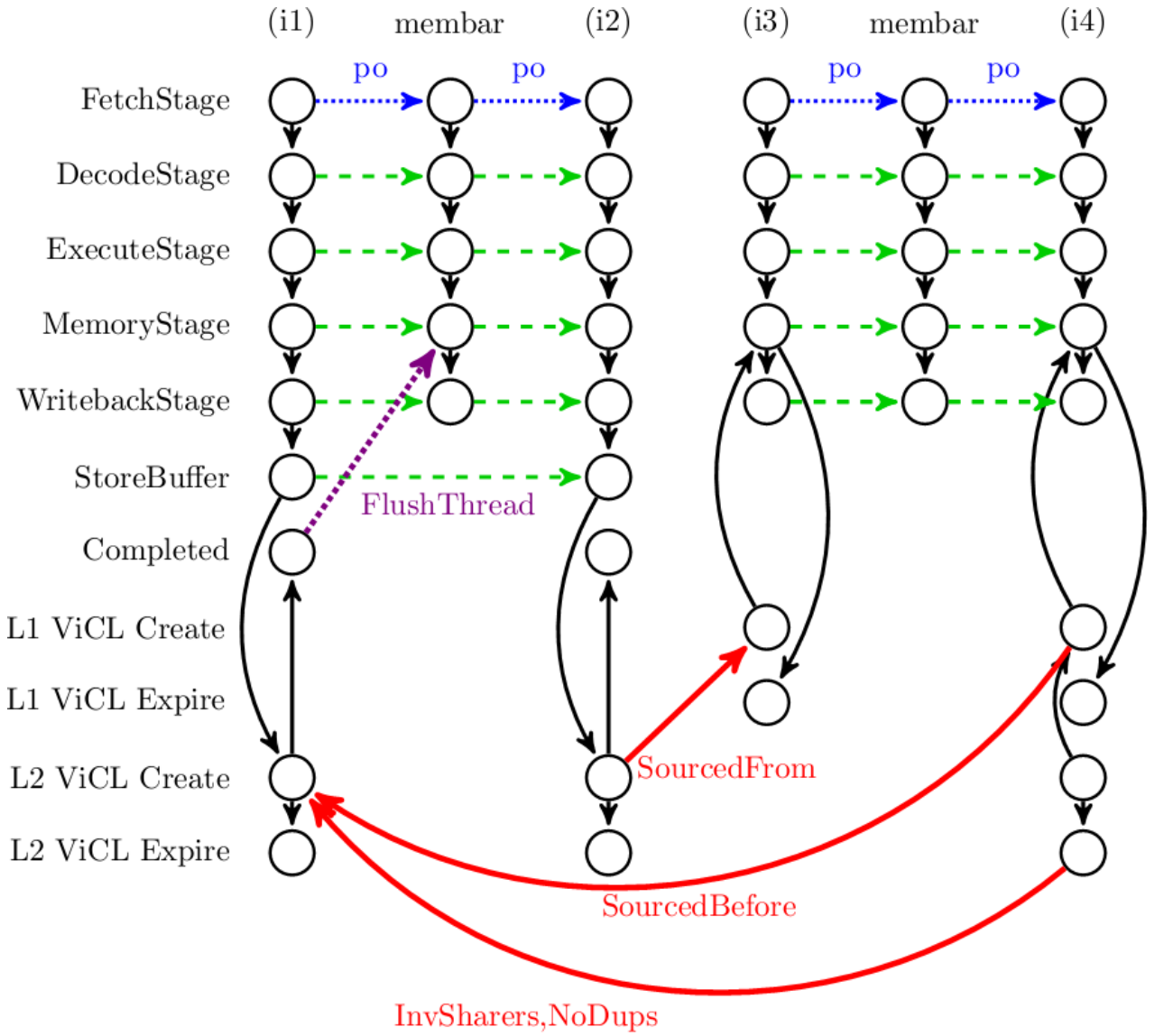

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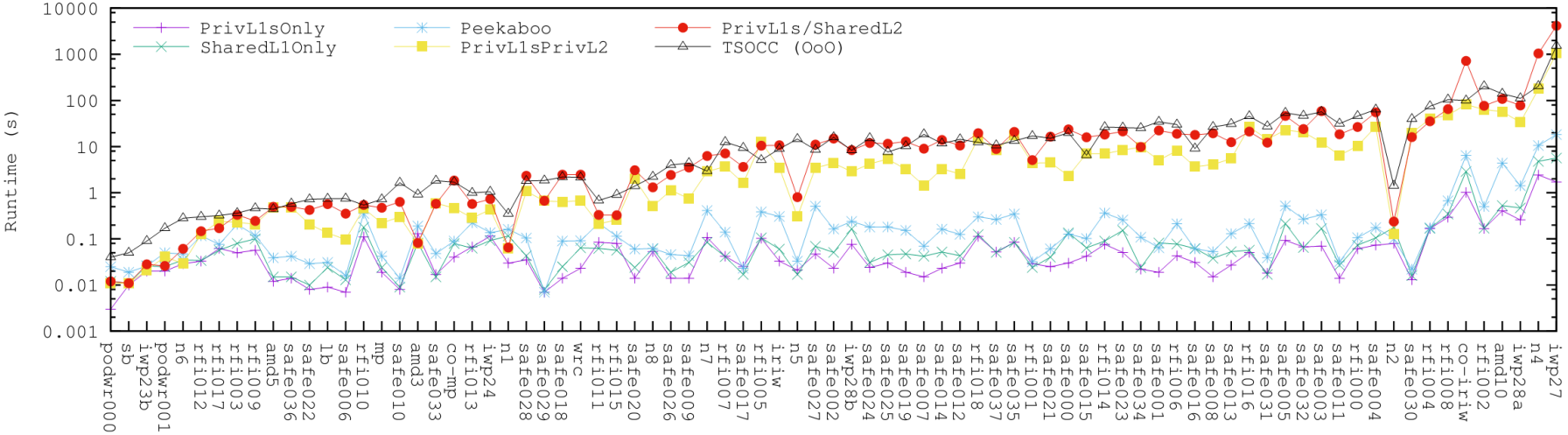
Verification Times



- Runtimes remain reasonable due to intelligent pruning and unsatisfiable constraint detection
- Subsequent research has used SMT solver-based techniques to run most tests in just **seconds**! [ASPLOS 2016]

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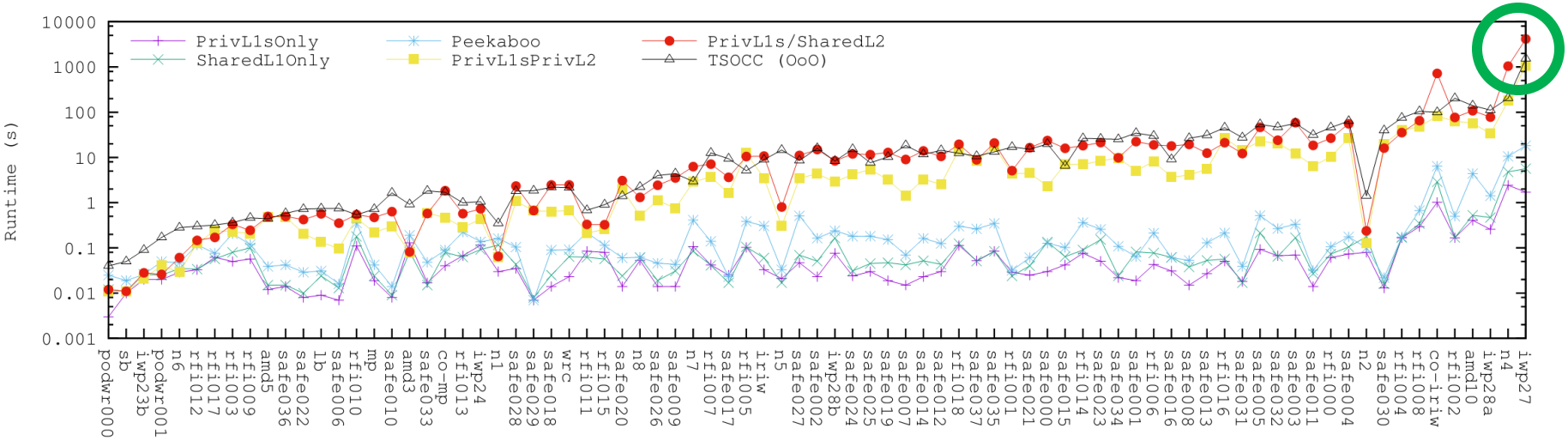

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Conclusion

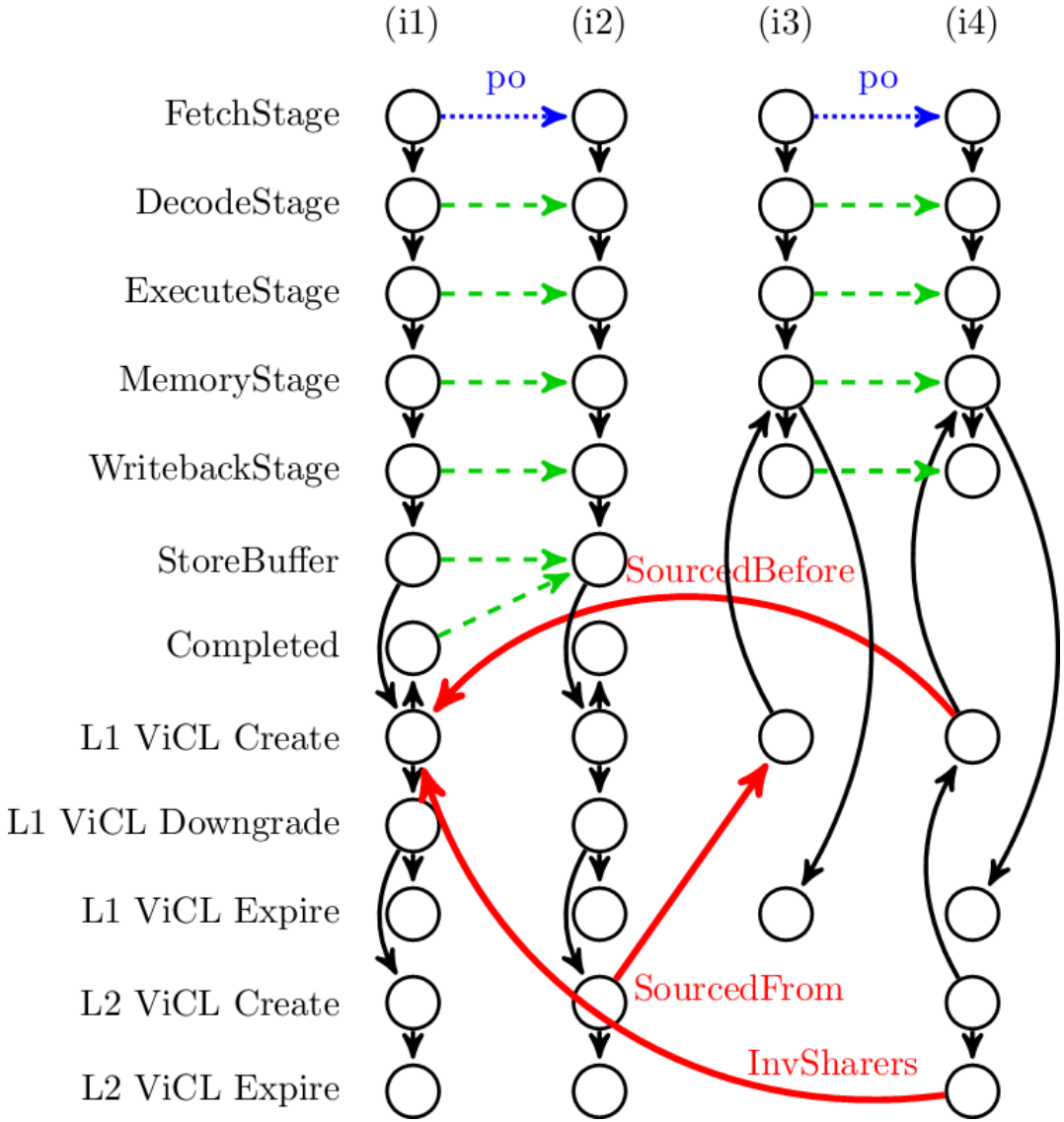
- CCI verification is critical to correct operation of complex parallel systems
- **CCICheck:** static CCI-aware microarchitectural consistency verification
  - Partial incoherence (GPUs), lazy coherence, and more!
- μhb graphs, ViCLs, and constraint-based enumeration
  - **Comprehensive** and **intuitive** μarch modelling
- Allows designers to build correct systems with greater ease and confidence

CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface

Yatin A. Manerkar, Daniel Lustig,
Michael Pellauer, and Margaret Martonosi

Code available at
https://github.com/ymanerka/ccicheck

Lazy Coherence (TSO-CC)



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- Thus, TSO is maintained

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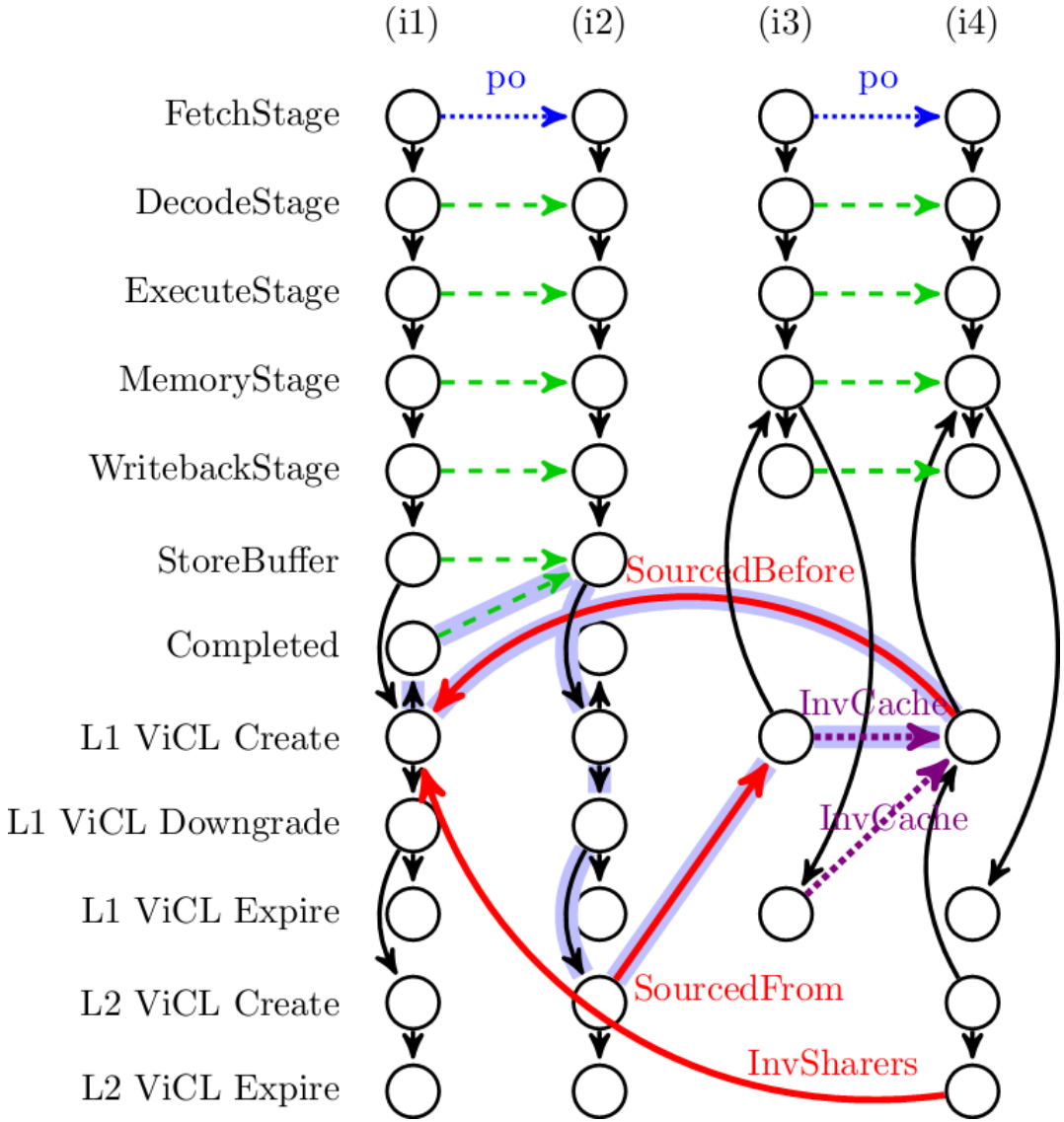

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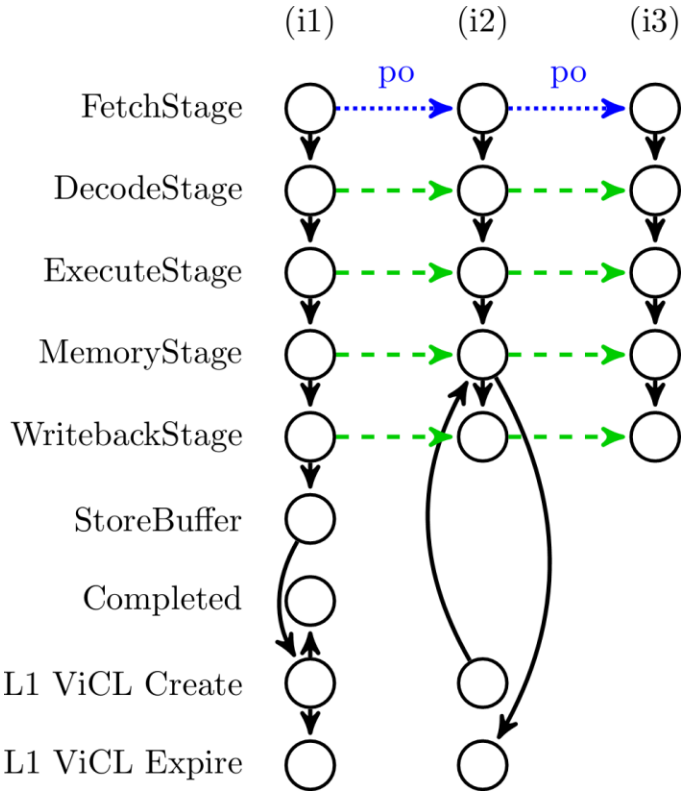

- i3 needs a source for its value
- L1 ViCL with same address and data

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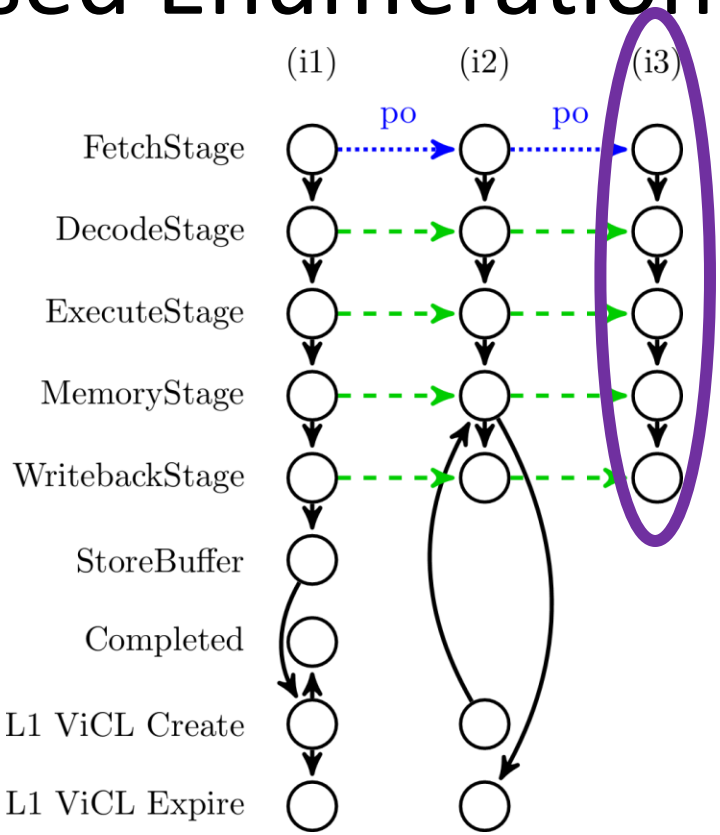

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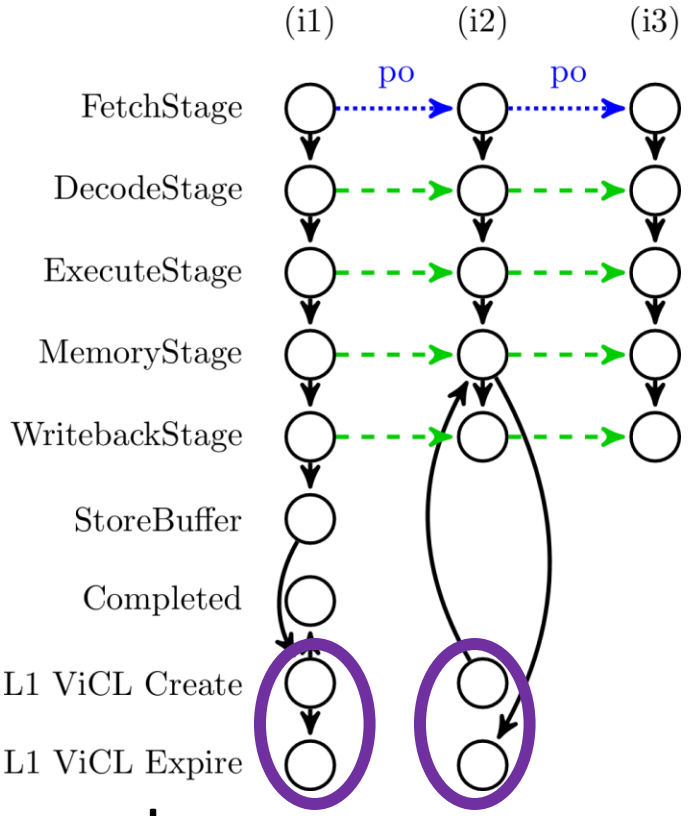

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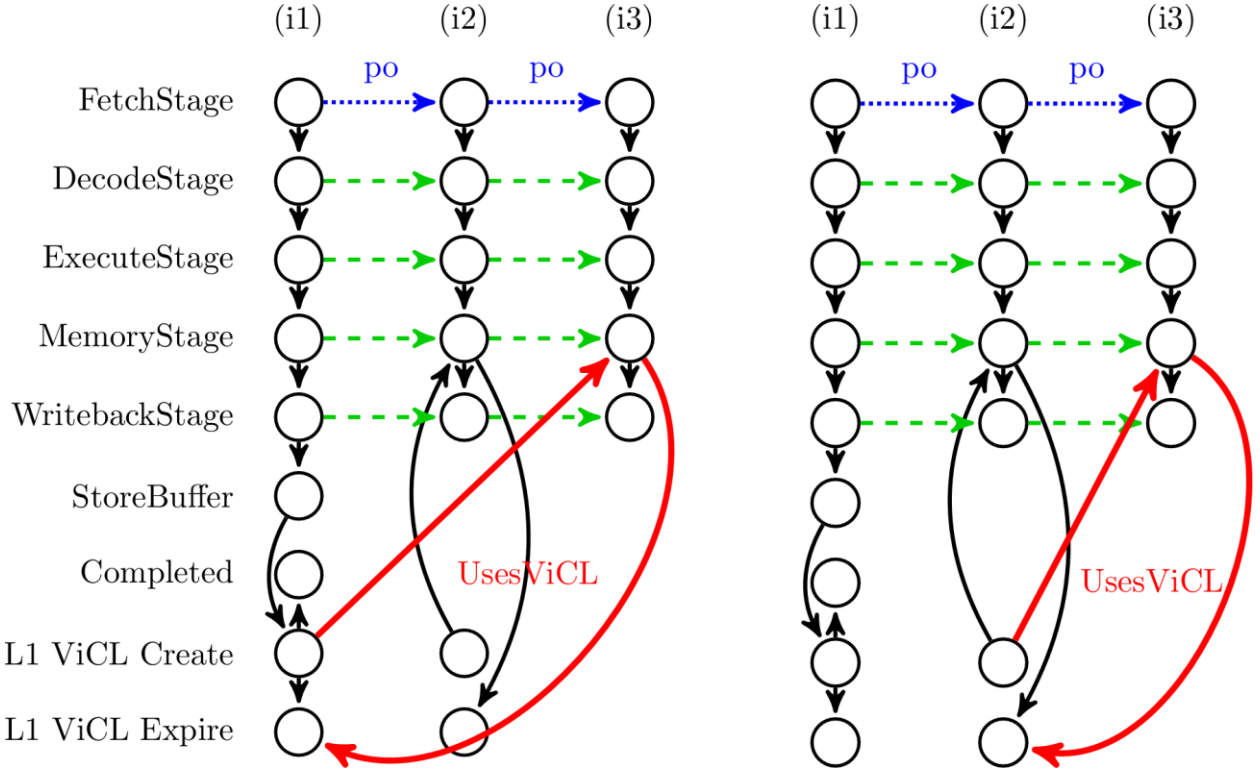

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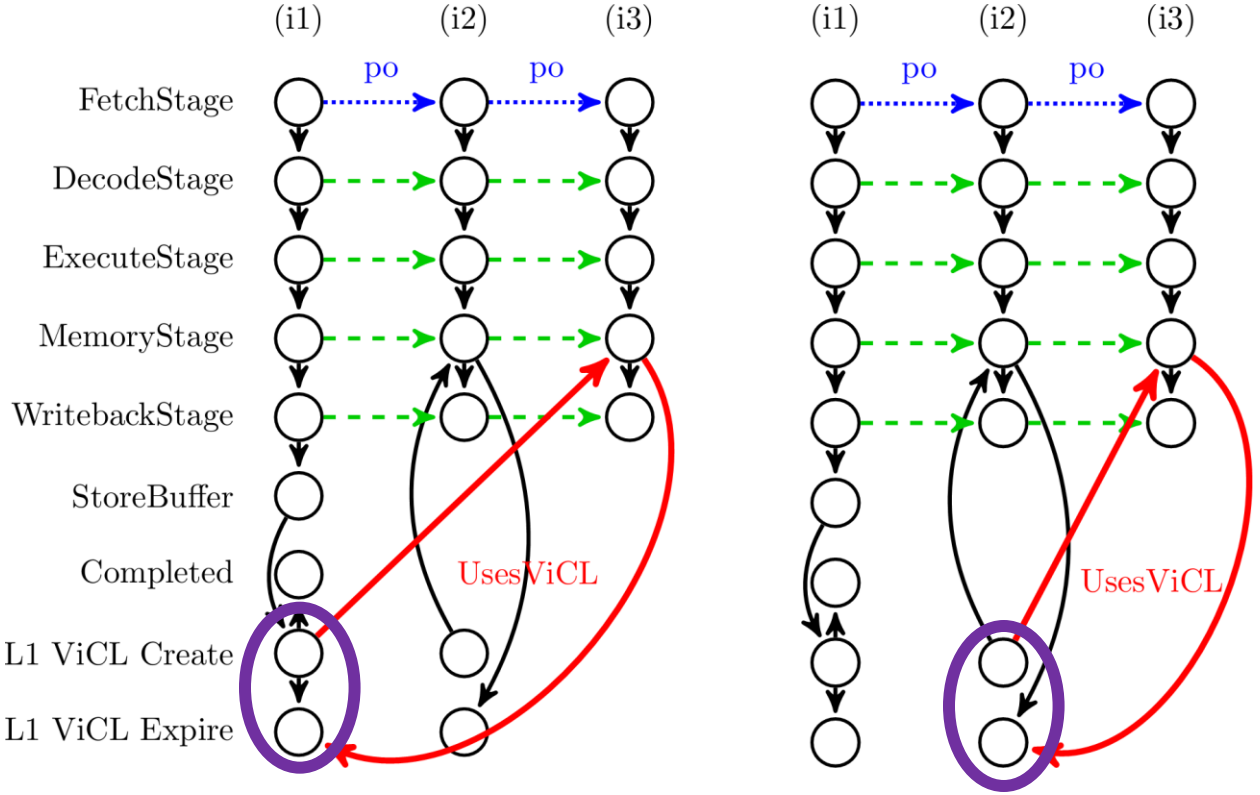

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