

# **Modular, Compositional, and Executable Formal Semantics for LLVM IR**

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## **Outline**

- Motivation & Background
- Introduction to Interaction Trees (ITrees)
- Modeling a simple assembly language (ASM) using ITrees
- Extending ASM to LLVM IR
- Authors' results
- "Group" commentary



## **Formal Models**

#### Sp<u>ecci</u>fyonations

- InformatifLLVM IR
- Used to prove correctness bigged in and Executable Formal Semantics for LLVM IR optimizany he, can alteompilation
	- Only partial correctness

Denotati∂nal ਓeନୀ§ାର୍ଗ୍ୱନ୍ଥeasily "sneak by"

- Formal: ନd de **ଏହା ନାଚାଡ ସା**ଦି<del>ପ</del>୍ରାପ୍ରେ ଜଣି re lan **Model** can prove total correctness  $\bullet$  - FA method of mapping a language into a mathematical object. and designing an equilational theory to prove properties of the language. **programmed in the Engineering Math** 
	- Challenge: coherence of model and implementation



"Specification" by Bing Image Creator

<del>Coq </del>Gallina



#### **Interaction Trees**

CoInductive itree (E : Type -> Type)  $(R : Type)$  : Type :=  $Ret(r: R)$ Tau  $(t : itree E R)$ Vis  $\{A : Type\}$  (e : E A)(k : A -> itree E R).

- Tree with 3 types of nodes
	- $\circ$  Ret: a leaf holding a value of type R
	- o Tau: an empty node that has one successor
	- Vis: a node with an **Effect** and a **Continuation**



#### **Interaction Trees**

CoInductive itree (E : Type -> Type) (R : Type) : Type :=  $Ret(r: R)$ Tau  $(t : itree E R)$ Vis  $\{A : Type\}$  (e : E A)(k : A -> itree E R).

- Tree with 3 types of nodes
	- $\circ$  Ret: a leaf holding a value of type R
	- Tau: an empty node that has one successor
	- Vis: a node with an **Effect** and a **Continuation**
- An ITree is parameterized by two types.
	- E: The type of effects this tree supports
	- R: The "return type" of the computation
- An ITree is a Colnductive type
	- Analogy: lists are Inductive, streams are CoInductive



#### **Example Interaction Trees**

CoFixpoint boring : itree IO nat  $:=$  Ret 42.

CoFixpoint spin : itree IO nat  $:=$  Tau spin.

Ex 1) A program that just returns 42 Ex 2) A program that spins forever

CoInductive itree (E : Type -> Type) (R : Type) : Type :=  $Ret(r: R)$ Tau  $(t : itree E R)$ Vis {A : Type} (e : E A)(k : A -> itree E R).

ITree definition

Inductive IO : Type -> Type := Input : IO string Output : string -> IO unit.

An input/output effect



### **Example Interaction Trees**





Ex 3) A program that takes input and prints it (forever)

CoInductive itree (E : Type -> Type)  $(R : Type)$  : Type :=  $Ret(r: R)$ Tau  $(t : itree E R)$ Vis {A : Type} (e : E A)(k : A -> itree E R).

ITree definition

Ex 4) A program that terminates upon receiving input "9"



An input/output effect



#### **Example Interaction Trees**



A program that takes input and prints it (forever)

```
CoFixpoint echo : itree IO void :=
    n \leq trigger Input;
    trigger (Output n) ;
    Tau echo.
```
The same program, using monad syntax



## **Equational Reasoning with ITrees**



#### Theorem compile correct (s : stmt) :  $[s] \approx [(complete s)]$ .

Bisimulation is a way to define when two systems "behave the same" relative to an external observer and independent of their internal structure.



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## **Simple Assembly Language → ITree**

- 1. Define the syntax of ASM
- 2. Decide what effects ASM has
- 3. Map the syntax of ASM into an Itree



## **Step 1: Define ASM**

```
Definition addr : Set := string.
Definition req : Set := nat.
Definition value: Set := nat.
Variant operand : Set :=
| Oimm ( : value)
\vert Oreg ( : reg).
Variant instr : Set :=Imov (dest : reg) (src : operand)
 Iload (dest : reg) (addr : addr)
```

```
Istore (addr : addr) (val : operand)
| Iadd (dest : reg) (src : reg) (o : operand)
```

```
Variant branch {label : Type} : Type :=
 Bimp ( : label)
 Bbrz (: reg) (yes no : label)
 Bhalt.
Inductive block {label : Type} : Type :=
 bbi ( : instr) ( : block)
 bbb (: branch label).
Record asm (A B: nat): Type :=
   internal : nat;
            : fin (internal + A) -> block (fin (internal + B))
   code
```


#### **Step 2: Determine Effects**

Variant Req : Type -> Type := GetReq  $(x : \text{req})$  : Req value SetReq  $(x : \text{req})$   $(y : \text{value})$ : Req unit.

Inductive Memory : Type -> Type := Load (a : addr) : Memory value Store (a : addr) (val : value) : Memory unit.

Definition RegAndMem : Type -> Type := Memory  $\theta$  Reg.

```
Definition addr : Set := string.
Definition reg : Set := nat.
Definition value : Set := nat.
Variant operand : Set :=
  Oimm ( : value)
 0reg ( : reg).
Variant instr : Set :=Imov (dest : reg) (src : operand)
  Iload (dest : reg) (addr : addr)
  Istore (addr : addr) (val : operand)
  Iadd (dest : reg) (src : reg) (o : operand)
Variant branch {label : Type} : Type :=
  Bjmp ( : label)
  Bbrz (: reg) (yes no : label)
  Bhalt.
 Inductive block {label : Type} : Type :=
  bbi (: instr) (: block)
  bbb ( : branch label).
Record asm (A B: nat): Type :=
    internal : nat;
            : fin (internal + A) -> block (fin (internal + B))
    code
```


#### Step 3:  $ASM \rightarrow$  ITree RegAndMem void

```
Definition denote operand (o : operand) : itree RegAndMem value :=
  match o with
    Oimm v \Rightarrow Ret vOreg v => trigger (GetReg v)
  end.
Definition denote instr (i : instr) : itree RegAndMem unit :=
  match i with
   Iload d addr \Rightarrowval \leq triqqer (Load addr) ;;
    trigger (SetReg d val)
   Istore addr v \Rightarrowval <- denote operand v;
    trigger (Store addr val)
    Imov d s \Rightarrowv <- denote operand s ;;
    trigger (SetReg d v)
    Iadd d 1 r \Rightarrowlv \leq trigger (GetReq l);
    rv <- denote operand r;
    trigger (SetReg d (lv + rv))
  \mathbf{r}
```

```
Definition denote br {B} (b : branch B) : itree RegAndMem B :=
  match b with
    Bjmp l \Rightarrow Ret lBbrz v y n \Rightarrowval <- triquer (GetReq v) ;;
    if val:nat then Ret y else Ret n
    Bhalt \Rightarrow exit
  end.
Fixpoint denote bk {B} (b : block B) : itree RegAndMem B :=
  match b with
    bbi i b \Rightarrowdenote instr i ;; denote bk b
    bbb b \Rightarrowdenote br b
  end.
```


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## **LLVM → ITree**

- 1. Define the syntax of LLVM
- 2. Decide what effects LLVM has
- 3. Map the syntax of LLVM into an Itree



## **Step 1: Define LLVM Syntax → ITree**

- Accounts for full LLVM IR
	- Straightforward, but tedious
	- o Including phi nodes, metadata, data layout, attributes, module flags,..
- Authors' provide a parser from ll files into this syntax



#### **Step 2: Determine Effects**

```
Variant GlobalE (k v:Type) : Type -> Type :=
 GlobalWrite (id: k) (dv: v): GlobalE k v unit
 GlobalRead (id: k): GlobalE k \vee v.
```

```
Variant LocalE (k v:Type) : Type -> Type :=
LocalWrite (id: k) (dv: y): LocalE k y unit
LocalRead (id: k): LocalE k \vee v.
```

```
Variant StackE (k v:Type) : Type -> Type :=
StackPush (args: list (k * v)) : StackE k v unit
StackPop : StackE k v unit.
```

```
Variant CallE : Type -> Type :=
I Call
             : forall (t:dtyp) (f:uvalue) (args:list uvalue), CallE uvalue.
```

```
Variant ExternalCallE : Type -> Type :=
ExternalCall
                     : forall (t:dtyp) (f:uvalue) (args:list dvalue), ExternalCallE dvalue.
```

```
Variant IntrinsicE : Type -> Type :=
| Intrinsic : forall (t:dtyp) (f:string) (args:list dvalue), IntrinsicE dvalue.
```


#### **Step 2: Determine Effects**

```
Variant GlobalE (k v:Type) : Type -> Type :=
GlobalWrite (id: k) (dv: v): GlobalE k v unit
GlobalRead (id: k): GlobalE k v v.
Variant LocalE (k v:Type) : Type -> Type :=
LocalWrite (id: k) (dv: y): LocalE k y unit
LocalRead (id: k): LocalE k \vee v.
Variant StackE (k v:Type) : Type -> Type :=
```

```
StackPush (args: list (k * v)) : StackE k v unit
StackPop : StackE k v unit.
```

```
Variant CallE : Type -> Type :=
Call
             : forall (t:dtyp) (f:uvalue) (args:list uvalue), CallE uvalue.
```
Variant ExternalCallE : Type -> Type := ExternalCall : forall (t:dtyp) (f:uvalue) (args:list dvalue), ExternalCallE dvalue.

```
Variant IntrinsicE : Type -> Type :=
| Intrinsic : forall (t:dtyp) (f:string) (args:list dvalue), IntrinsicE dvalue.
```

```
Variant MemoryE : Type -> Type :=
 MemPush : MemoryE unit
 MemPop : MemoryE unit
 Alloca : forall (t:dtyp),
                                                          (MemoryE dvalue)
        : forall (t:dtyp) (a:dvalue),
                                                          (MemoryE uvalue)
 Load
 Store : forall (a:dvalue) (v:dvalue),
                                                         (MemoryE unit)
         : forall (t:dtyp) (v:dvalue) (vs:list dvalue), (MemoryE dvalue)
 GEP
 ItoP
       : forall (i:dvalue),
                                                          (MemoryE dvalue)
         : forall (t:dtyp) (a:dvalue),
                                                         (MemoryE dvalue)
 PtoI
```

```
Variant PickE : Type -> Type :=
 pick (u:uvalue) (P : Prop) : PickE dvalue.
```

```
Variant UBE : Type -> Type :=
 ThrowUB : string -> UBE void.
```

```
Variant exceptE (Err : Type) : Type -> Type :=
 Throw : Err -> exceptE Err void.
```

```
Variant DebugE : Type -> Type :=
 Debug : string -> DebugE unit.
```


#### **Step 3: LLVM → ITree VellvmE V**

```
OP GetElementPtr dt1 (dt2, ptrval) idxs =>
vptr <- denote exp (Some dt2) ptrval;
vs \le map monad (fun '(dt, index) => denote exp (Some dt) index) idxs ;;
let maybe dvs := dvptr <- uvalue to dvalue vptr ;;
                 dvs < - map monad uvalue to dvalue vs ;;
                 ret (dvptr, dvs)
in
match maybe dvs with
  inr (dvptr, dvs) => fmap dvalue to uvalue (trigger (GEP dt1 dvptr dvs))
  \text{inl} \Rightarrow(* Pick to get dvalues *)
  dvptr <- concretize_or_pick vptr True ;;
  dvs <- map monad (fun v = concretize or pick v True) vs ;;
  fmap dvalue to uvalue (trigger (GEP dt1 dvptr dvs))
end
```
Mapping GetElementPrt instruction to ITree program



#### Step4: ITree E R  $\rightarrow$  Monad Transformer Stack





Fig. 5. Levels of interpretation



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## **Authors' Results**

- **Block fusion** 
	- Conditions:
		- BB1 has a direct jump to BB2
		- BB1 is the only predecessor of BB2
		- $\blacksquare$  BB1  $\neq$  BB2
	- Transformation
		- Remove BB1 branch
		- Merge BB1 and BB2
		- Update Phi nodes of BB2's successors





#### **Authors' Results**

Theorem block fusion cfg correct : forall (G : cfg dtyp),  $wf$  cfa  $G \rightarrow$  $\boxed{6}$   $\boxed{\approx}$   $\boxed{}$  block fusion cfq G  $\boxed{}$ . Proof. intros G [WF1 WF2]. unfold denote cfg. simpl bind. unfold block fusion cfg. destruct (block fusion G. (blks)) as [bks' [[src tgt] |]] eqn:EQ. - break match goal; [reflexivity |]. simpl. apply Bool.orb false elim in Hegb as [INEQ1 INEQ2]. unfold Eqv.eqv dec in \*. rewrite <- RelDec.neg rel dec correct in INEQ1. rewrite <- RelDec.neq rel dec correct in INEQ2. eapply block fusion correct some with  $(f := G.(init))$  (to :=  $G.(init))$  in EQ; auto. rewrite update provenance ineq in EQ; auto. eapply eutt clo bind; [apply EQ |].  $intros$   $[[]|?]$   $[[]|?]$   $INV;$   $try$  now  $inv$   $INV.$ subst; reflexivity. eapply wf cfg src not in phis; eauto. constructor; auto. - reflexivity. Qed.

# $\|G\|$   $\approx$   $\|fuse(G)\|$



## **Authors' Results**

- This paper and the original ITrees paper have been used in recent developments
	- VELLVM is used in the HELIX verification chain
	- HELIX is code generation and formal verification system with a focus on the intersection of high-performance and high-assurance numerical computing
- Distinguished paper POPL 2020





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### **"Group" Commentary**

- **Strengths** 
	- Elegant theory
	- Excellent proof engineering
		- Modular, reusable components
		- Abstracted over hard coinductive proofs
		- Provide great tactic library
- Weaknesses
	- Coherence
		- Memory model is not sufficient to prove certain optimizations (in progress)
		- Only sequential programs supported for now
	- While they provide a good equational theory and proof tactics, a better program logic will be needed to handle large programs. (In progress)



## **Questions?**

Monad Laws

 $\begin{array}{c} (x \leftarrow ret\ v\ ;\ ;\ k\ x) \cong (k\ v) \\ (x \leftarrow t\ ;\ ;\ ret\ x) \cong t \\ (x \leftarrow (y \leftarrow s\ ;\ ;\ t)\ ;\ ;\ u) \cong (y \leftarrow s\ ;\ ;\ x \leftarrow t\ ;\ ;\ u) \end{array}$ 

**Structural Laws** 

(Tau t)  $\approx$  t<br>
(x  $\leftarrow$  (Tau t) ;; k)  $\approx$  Tau (x  $\leftarrow$  t ;; k)<br>
(x  $\leftarrow$  (Vis e k1) ;; k2)  $\approx$ (Vis e (fun  $y \Rightarrow$  (k1 y) :: k2))

 $t1 \cong t2 \rightarrow$  Tau t1  $\cong$  Tau t2

 $k1 \approx k2 \rightarrow$  Vise  $k1 \approx V$ ise  $k2$ 

Congruences

t1  $\approx$  t2  $\land$  k1  $\approx$  k2  $\rightarrow$  bind t1 k1  $\approx$  bind t2 k2

Fig. 5. Core equational theory of ITrees.

```
Theorem block fusion cfg correct :
  forall (G : cfg dtyp),
    wf cfg G \rightarrow[ G ] \approx [ block fusion cfg G ].
Proof.
  intros G [WF1 WF2].
  unfold denote cfg.
  simpl bind.
  unfold block fusion cfg.
  destruct (block fusion G. (blks)) as [bks' [[src tgt] |]] eqn:EQ.
  - break match goal; [reflexivity |].
    simpl.
    apply Bool.orb false elim in Heqb as [INEQ1 INEQ2].
    unfold Eqv.eqv dec in *.
    rewrite <- RelDec.neg rel dec correct in INEQ1.
    rewrite <- RelDec.neg rel dec correct in INEQ2.
    eapply block fusion correct some
      with (f := G.(init)) (to := G.(init)) in EQ; auto.
    rewrite update provenance ineq in EQ; auto.
    eapply eutt clo bind; [apply EQ \vert].
    intros [[]?] [[]]'?] INV; try now INV.
    subst; reflexivity.
    eapply wf cfq src not in phis; eauto.
    constructor; auto.
  - reflexivity.
```