Design of 100-900 GHz AlGaAs/GaAs Planar Heterostructure Barrier Varactor Frequency Triplers

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***Abstract*—In this paper we offer a simple set of accurate frequency-domain design equations that can be used to calculate optimal embedding impedances and tripling efficiency. These equations can be used for a wide range of device and circuit parameters. The effects of parasitic resistance and operating temperature on device performance, and how these parameters vary with device design are explored. Comparisons to experiment are made for planar HBVs demonstrating at least 3% efficiency at 78 GHz input frequency and 50 mW of input power.**

***Index Terms*—HBV, varactor frequency tripler.**

I. INTRODUCTION

The Heterostructure Barrier Varactor (HBV) diode [1, 2] is ideally suited for frequency tripling in the millimeter wave and sub-millimeter wave regime. The symmetric capacitance-voltage characteristic of the HBV allows for tripler design without requiring second-harmonic idler circuits or DC bias. In principle, this should make HBV triplers easier to design and implement; however, the complex device structure and device physics can make the overall tripler design process more difficult. In particular, the design and fabrication of the devices are more difficult than Schottky diode structures used in similar applications. Subsequently, the output power and efficiency from Schottky diode varactor multipliers are still somewhat superior to HBV multipliers [3-5]. In this paper we describe the basic design concepts, equations, and parameters related to GaAs-AlGaAs-GaAs planar HBVs.

II. HBV MULTIPLIER ANALYSIS

A. Intrinsic device model

A generic layer structure of an HBV is shown in table i. For N epitaxially stacked barriers, the layer sequence 2-5 is repeated N times. The intrinsic part of the HBV consists of layer 2-6, where a high band-gap material (layer 4) prevents electron transport through the structure and the diode capacitance is modulated due to depletion of carriers in layers 2 and 6.

TABLE I: HBV GENERIC LAYER STRUCTURE

Layer No.		Thickness [Å]	Doping level [cm^{-3}]
7	Contact	~3000	n^{+}
6	Depletion	l ~ 3000	$N_d \sim 10^{17}$
5	Spacer	s ~ 50	Undoped
4	Barrier	b ~ 200	Undoped
3	Spacer	s ~ 50	Undoped
2	Depletion	l ~ 3000	$N_d \sim 10^{17}$
1	Buffer		n^{+}
0	Substrate		n^{+} or SI

In our analysis, we use a two element model for the intrinsic part of the HBV: a non-linear differential elastance, $S(V) = dV/dQ = 1/C(V)$, in series with a non-linear parasitic resistance, $R(V)$. Varactor mode of operation for HBVs is

preferred and therefore large conduction currents should be reduced as much as posssible for optimal performance.

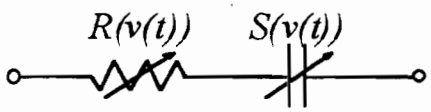

Figure 1: Intrinsic equivalent circuit of a pure varactor diode (i.e. no leakage current).

Elastance model

The minimum differential elastance of an HBV is determined by the effective separation distance between the charge on each side of the barrier. For a typical HBV structure (see table i) the minimum elastance per barrier can be estimated as

$$S'_{min} = \frac{b}{\varepsilon_b} + \frac{2s}{\varepsilon_d} + \frac{2L_D}{\varepsilon_d} [\mathrm{m^2/F}]$$
$$S_{min} = \frac{N}{A} S'_{min} \qquad (1)$$

where N is the number of barriers, A is the device area, and L_D is the Debye length:

$$L_D = \sqrt{\frac{kT\varepsilon_d}{q^2 N_D}}. \qquad (2)$$

During a pump-cycle, the differential elastance is modulated due to depletion of carriers and the overall elastance can, therefore, be expressed as the sum of the above linear term and a non-linear part as:

$$S(t) = \frac{N}{A}\left(S'_{min} + \underbrace{S'_d(t)}_{depletion} \right) [1/\mathrm{F}]$$
$$S'_d(t) \in \left[0, A\frac{S_{max} - S_{min}}{N} \right] \qquad (3)$$

where S_{min} and S_{max} are the minimum and maximum elastance during a pump cycle respectively. The maximum differential elastance is determined by the maximal extension of the depletion region, w_{max}, as:

$$S'_{max} = \frac{b}{\varepsilon_b} + \frac{2s}{\varepsilon_d} + \frac{w_{max}}{\varepsilon_d} [\mathrm{m^2/F}]. \qquad (4)$$

For an HBV, the depletion length limit is determined by at least one of three "breakdown" conditions each giving a different value for w_{max}. These are: 1) depletion layer punch-through and $w_{max}=l$, 2) large electron conduction across the barrier region at large voltage, V_{max}, or 3) large currents from avalanche breakdown at large voltage. To maintain varactor efficiency the conduction current should be minimized. For relatively large band gap materials such as GaAs-AlGaAs-GaAs conditions 1 and 2 appear to dominate. In order to calculate w_{max} used in equation 4 it is necessary to estimate the peak operating voltage. For optimal performance, $w_{max} = l$. If the punch-through voltage is greater than the voltage at the onset of large conduction current the maximum depletion width cannot be achieved. For this case, w_{max} will be reduced and its value must be estimated. This is particularly important when the device temperature is increased and conduction current across a moderate HBV barrier is increased.

It is possible to estimate w_{max} by calculating the voltage at which the conduction current through the device is nearly equal to the displacement current. For HBVs, the conduction current is approximately

$$I(E_b) = A \cdot aT^2 Sinh\left(\frac{E_b}{E_o}\right) e^{-\frac{\phi_b}{kT}} \qquad (5)$$

where a, ϕ_b, and E_o are fitting parameters and E_b is the electric field in the barrier and can be estimated as:

$$E_b = qN_d \frac{b\varepsilon_d + 2s\varepsilon_b}{\varepsilon_b^2} \cdot \left(\sqrt{1 + \frac{2\varepsilon_d \varepsilon_b^2 V_{max}}{NqN_d (b\varepsilon_d + 2s\varepsilon_b)^2}} - 1 \right) \quad (6)$$

Taking the derivative of equation (5) (device conductance) and given:

$$\left. \frac{dI(V,T)}{dV} \right|_{V=V_{max}} << \omega_p C_{max} . \quad (7)$$

For strong conduction, one can solve for V_{max} and w_{max} where conduction is dominant.

Intrinsic Series Resistance

The parasitic series resistance is the sum of the resistance of undepleted active layers, the spreading resistance, and the ohmic contact resistance. However, only the resistance of undepleted layers contributes to the intrinsic varactor model shown in figure 1. All extrinsic impedances can be regarded as a part of the embedding circuit, see figure 2. If the depletion layer, No. 2,6 in Table I, is homogeneously doped and an abrupt space charge is assumed, the resistance of undepleted layers can be expressed as a function of the length of the depleted region, w, as

$$R(t) = \frac{\rho_d}{A}(l + N(l - w(t))) \quad (8)$$
$$w(t) \in [0, l]$$

where l is the length of the depletion layer and ρ_d is the corresponding resistivity. For simplicity, the extension of the depletion region, $w(t)$, is assumed to be proportional to the elastance as

$$w(t) = \varepsilon_d S'_d(t) \quad (9)$$

which in combination with (8) gives:

$$R(t) = \frac{\rho_d}{A}\left(l + N\left(l - \varepsilon_d S'_d(t)\right)\right). \quad (10)$$

B. The frequency tripler circuit

The time-dependent voltage, $v(t)$, across the diode terminals in figure 1 can with the above proposed HBV model (3,10) be written as:

$$v(t) = \frac{\rho_d l}{A}(1+N)i(t) - \frac{N\rho_d \varepsilon_d}{A} S'_d(t)i(t) + \int S(t)i(t)dt \quad (11)$$

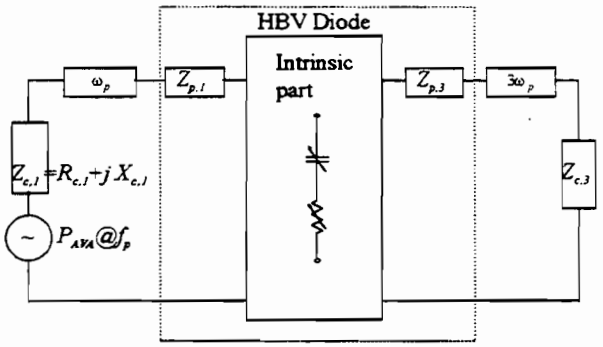

Figure 2: Schematic view of an HBV tripler circuit.

Since we are interested in the periodic steady-state solution of the above circuit equation (11), we represent the voltage-, the current- and the elastance-waveforms in the frequency domain and the time-domain equation takes the following form for the *kth* harmonic [7,11]:

$$V_k = \frac{\rho_d l}{A}(1+N)I_k + \frac{N}{A}\frac{S'_{min}}{jk\omega_p} I_k + \frac{N}{A}\left(\frac{1}{jk\omega_p} - \rho_d \varepsilon_d\right)\sum_{l=-\infty}^{\infty} I_l S'_{d,k-l} \quad (12)$$

The two first terms are linear but the last term accounts for the complex movement of the depletion edge. The current and the elastance

harmonics can be found by imposing embedding circuit conditions

$$V_k = V_k^{source} - \left(Z_{c,k} + Z_{p,k}\right) I_k \qquad (13)$$

where $Z_{c,k} = R_{c,k} + jX_{c,k}$ is the embedding circuit impedance and $Z_{p,k} = R_{p,k} + jX_{p,k}$ is the extrinsic parasitic impedance, see figure 2. Furthermore, define the complex modulation ratio as $M'_k = S'_k/(S'_{max}-S'_{min})$ and a general form of the large-signal device impedance, $Z_{d,k}$, within our varactor circuit model can be written as:

$$Z_{d,k} = \frac{\rho_d l}{A}(1+N) + \frac{N}{A}\frac{S'_{min}}{jk\omega_p} + \frac{N(S'_{max}-S'_{min})}{A} \cdot \left(\frac{1}{jk\omega_p} - \rho_d \varepsilon_d\right) \frac{1}{I_k} \sum_{l=-\infty}^{\infty} I_l M'_{d,k-l} \qquad (14)$$

Optimal embedding impedances

The summation over all current and elastance harmonics in (14) is a complex value which depends slightly on circuit conditions (13) and on physical details of the HBV itself. However, for maximum conversion efficiency when all available pump-power is absorbed and the third harmonic power delivered to the load is maximized; we assume that this complex summation is independent on external conditions and HBV layer structures. Consequently, the optimal embedding impedances, $Z_{c,n}$, close to any operating point can be expressed as

$$\begin{aligned}
R_{c,1} &\approx R_{p,1} + \frac{\rho_d l}{A}(1+N) + \frac{N}{A}(S'_{max}-S'_{min})\left(\frac{A_1}{\omega_p} - \rho_d \varepsilon_d C_1\right) \\
X_{c,1} &\approx -X_{p,1} + \frac{N}{A}\frac{S'_{min}}{\omega_p} + \frac{N}{A}(S'_{max}-S'_{min})\left(\frac{B_1}{\omega_p} - \rho_d \varepsilon_d D_1\right) \\
R_{c,3} &\approx R_{p,3} + \frac{\rho_d l}{A}(1+N) + \frac{N}{A}(S'_{max}-S'_{min})\left(\frac{A_3}{3\omega_p} - \rho_d \varepsilon_d C_3\right) \\
X_{c,3} &\approx -X_{p,3} + \frac{N}{A}\frac{S'_{min}}{3\omega_p} + \frac{N}{A}(S'_{max}-S'_{min})\left(\frac{B_3}{3\omega_p} - \rho_d \varepsilon_d D_3\right)
\end{aligned} \qquad (15)$$

where A_n, B_n, C_n, and D_n are fitting coefficients. If these parameters are extracted for realistic operating conditions and with accurate large-signal device simulator, the above optimal embedding impedances can be calculated for a wide range of device and circuit parameters.

Dynamic cut-off frequency

The dynamic cut-off frequency of a pure varactor device (i.e. no leakage current) is defined as:

$$f_c = \frac{S_{max} - S_{min}}{2\pi R_s} \cdot \qquad (16)$$

With the proposed intrinsic varactor model in Section IIa, define the series resistance as the sum of the maximal value of the intrinsic resistance (8) and the real part of the extrinsic parasitic impedance at the fundamental harmonic. If the equations for maximal and minimal elastance and the series resistance are

inserted in (16), the dynamic cut-off frequency for an HBV can finally be calculated as:

$$f_c = N\frac{w_{max} - 2L_D}{2\pi\varepsilon_d\left(AR_{p,1} + \rho_d l(1+N)\right)}. \qquad (17)$$

As shown above, it is very important to reduce the parasitic resistance as much as possible relative to the intrinsic device resistance. Also, w_{max} should be large relative to L_d to insure significant capacitance modulation and tripling. As described above, to optimize f_c the conduction current should minimized and $w_{max}=l$.

Pump power and conversion efficiency

The conversion efficiency is defined as the power delivered to the load at the third harmonic divided by the available input power and for a pure varactor multiplier, the efficiency is determined by the ratio of the pump-frequency and the dynamic cut-off frequency [6, 7]. A quick and fast estimation of the maximum conversion efficiency can be achieved from the following empirical expression

$$\eta \approx \frac{100}{1+\alpha\left(\frac{f_p}{f_c}\right)^{\beta}}\ [\%] \qquad (18)$$

where α and β are extracted from detailed large-signal simulations for a wide range of devices and circuit conditions, see table ii. For maximum possible efficiency f_c should be increased to its maximal value as described in equation 17.

Finally, it is necessary to estimate the input power needed to modulate the elastance of an HBV from S_{min} to S_{max}. The pump-power can be estimated as

$$P_{AVA} = \frac{|V_s|^2}{8R_{c,1}} = \frac{R_{c,1}}{2\left|Z_{d,1}\right|^2}|V_1|^2 \approx \gamma\frac{R_{c,1}}{2\left|Z_{c,1} - Z^*_{p,1}\right|^2}|V_{max}|^2 \qquad (19)$$

where γ is also a fitting coefficient, see table ii. Equation 19 insures that reasonable device parameters and required input powers are designed for a particular application.

III. Results and Discussion

A. Parameter extraction

All the coefficients were extracted by analyzing two four-barrier HBVs with an integrated Drift-Diffusion Harmonic Balance (DDHB) simulator [8, 9]. The pump frequency was 90 GHz and the device area 66 μm^2. All simulations were performed by assuming a homogenous temperature of T = 300 K across the active device region. A field-independent (low field) electron mobility of 4375 cm^2/Vs in the GaAs region and a calculated extrinsic parasitic series resistance of $R_{p,1}$ = 4.9 ohm were used. Intrinsic losses, e.g. ohmic losses in layers (No. 2,6), are fully taken into account by the DDHB simulator. The conversion efficiency was maximized by tuning the embedding impedances at the first and the third harmonic respectively. Finally, coefficients for the design equations (15,18,19) were extracted, see table ii. These coefficients allow the optimal embedding impedances and efficiency to be easily calculated.

TABLE II: HBV DESIGN COEFFICIENTS

Extraction conditions: f_p/f_c~0.05			
$A_1 = 0.047$	$B_1 = 0.33$	$C_1 = -0.17$	$D_1 = -2.5$
$A_3 = 0.24$	$B_3 = 0.66$	$C_3 = -1.3$	$D_3 = 4.9$
$\alpha = 200$	$\beta = 1.4$	$\gamma = 0.7$	

Comparison to experimental results

Device structure and measured performance

The epitaxial layer structure in table iii has been fabricated into a planar HBV configuration, see figure 4.

TABLE III: UVA-NRL-1174

Layer	Material	Doping [cm^{-3}]	Thickness [Å]
9	InAs	5×10^{18}	100
8	$In_{1\rightarrow0}GaAs$	5×10^{18}	400
7	GaAs	5×10^{18}	3000
6	GaAs	8×10^{16}	2500
5×4	GaAs	Undoped	35
4×4	$Al_{0,7}GaAs$	Undoped	200
3×4	GaAs	Undoped	35
2×4	GaAs	8×10^{16}	2500
1	GaAs	5×10^{18}	40000
0	GaAs	SI	-

An HBV device with an anode area of 89 μm^2 was mounted and tested in a tripler waveguide block (RAL DB2a). A flange-to-flange peak-efficiency of 3.1 % was achieved at an output frequency of 234 GHz. The maximal output power was 3.6 mW, see figure 3. The estimated loss at the input- and output circuit are approximately 1 dB and 2 dB respectively.

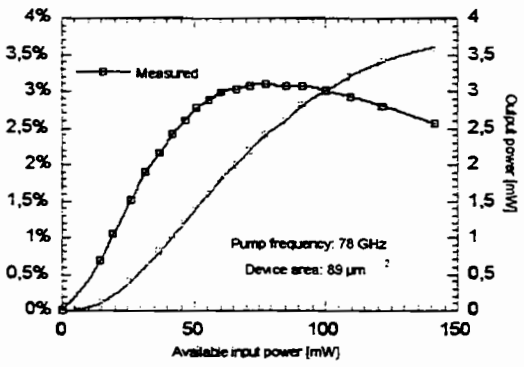

Figure 3: Measured output power and efficiency at an output frequency of 234 GHz.

Estimated thermal and parasitic resistance

In order to explain the lower than expected efficiency shown in figure 3, the effect of self-heating must be taken into account. This has been described in section IIA. For a 8 µm diameter device and by assuming a point heat-source in the middle of the active region, Jones [10] has estimated the thermal resistance through the finger and the GaAs substrate to R_t = 2 K/mW for this device geometry. Furthermore, if we assume that the thermal resistance is inversely proportional to the anode diameter and an input circuit loss of 1 dB, the device temperature can be as high as 400 K for the 10 µm (89μm^2) HBV used and an available pump power of 80 mW.

Figure 4: Planar HBVs (UVA-NRL-1174-17).

The extrinsic parasitic series resistance consists of the ohmic contact resistance and the spreading resistance in the n^{++} island that connects the two diodes. By using standard expressions for these losses, we can approximate the temperature dependent parasitic series resistance as

$$Z_{p1} = Z_{p,3} = \frac{200}{A} + \left(4 + \frac{20}{\sqrt{A}} + \frac{100}{A}\right)\frac{T}{298} \qquad (20)$$

where A is the anode area in μm^2. The first term represents the contact resistance and the second term estimates the spreading resistance in the n^{++} island.

Conversion efficiency

The negative effect of heating on the dynamic cut-off frequency (17) results from the temperature dependence of the series resistance (20) and the Debye-length (2), as well as the reduction in maximal depletion length, w_{max}, as the temperature increases.

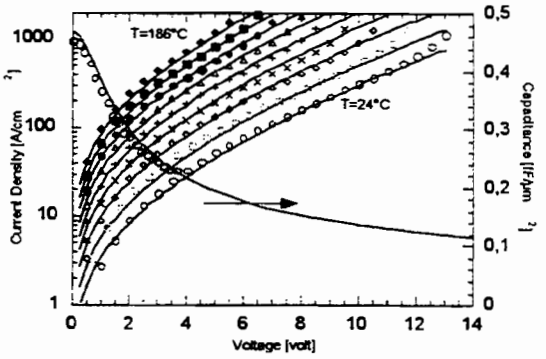

Figure 5: Measured C-V (RT) and I-V (RT-186°C) characteristics of the UVA-NRL-1174 HBV material.

The conversion efficiency increases with pump power as long as the conduction current through the barrier is negligible compared to the displacement current. The measured I-V characteristic versus temperature and C-V characteristic for the UVA-NRL-1174 device are shown in Figure 5. The parameters: $a = 170\ A/(m^2K^2)$, $E_o = 4.2\times10^6\ V/m$, and $\phi_b = 0.17\ eV$ in (5) provides an excellent fit with measured I-V characteristic at different temperatures. As a guideline, to ensure varactor mode of operation, the maximum voltage, V_{max}, can be estimated versus temperature as:

$$\left.\frac{dI(V,T)}{dV}\right|_{V=V_{max}} = \frac{1}{10}\omega_p C_{max}. \qquad (21)$$

The value of 1/10 can be adjusted significantly and only have a minor effect on the overall value of the efficiency.

Using the analysis outline in IIA w_{max} was calculated for temperatures ranging from 250-500 K. Then, the predicted efficiency over this range was calculated using equations (17,18) with the coefficients in Table II. The results are shown in Figure 6 (including 3 dB of circuit loss). The experimental results are shown. As seen, the efficiency is reduced at higher temperatures as the conduction current increases and $w_{max} < l$. Also, if the parasitic resistance is reduced the entire curve will shift up. For Figure 6 the parasitic resistance is approximately 12 ohms and calculated using equation 20.

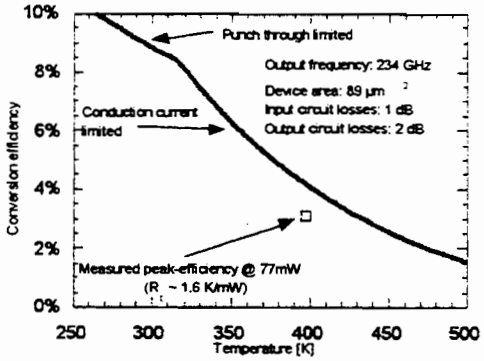

Figure 6: Maximal efficiency versus device temperature.

Finally, with the design-coefficients in table ii and equations (1-2,4,15,20) the optimal embedding impedances for a device temperature of 400 K can be estimated: $Z_{c,1} = 21 + j97$ and $Z_{c,3} = 27 + j36$.

IV. CONCLUSIONS AND SUMMARY

We have described a complete model that can be used to predict the optimal embedding impedances and efficiency for HBVs. The important effects of self heating and the need to minimize parasitic resistance have been described. Comparisons to experimental results are favorable. Based one the analysis described here a new set of HBVs have been designed and will be tested in the near future.

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