

An Integrated 435 GHz Quasi-Optical Frequency Tripler

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1 Abstract

Current saturation and reverse breakdown voltage limit the power handling capability of single Schottky diodes. This limitation can be overcome by the technique of power combining using an array of diodes. A quasi-optical design limits neither the number of diodes nor the size of the chip, on which the diodes are integrated. Based on the promising results obtained with the quasi-optical frequency doubler at 290 GHz [1], and aiming at developing an all-quasi-optical local oscillator source, a 435 GHz quasi-optical tripler device is presented. The tripler element is based on a back-to-back pair of GaAs

Schottky varactor diodes located on GaAs and integrated with a planar folded dipole antenna. A chip area of $1650 \times 1650 \mu\text{m}^2$, geared to the beam waist of the Gaussian beam, comprises thirty tripler elements. The fabrication and initial characterisation are presented. The measurement setup for the radio frequency performance evaluation of the integrated device, which is yet to be performed, is described.

2 Introduction

Waveguide based frequency multipliers have already covered the frequency band from 100 GHz to 1 THz. To date, although they have shown excellent performance as frequency multipliers, they suffer from the degradation caused by the current saturation when driven into high power levels. Instead, the maximum available power can be distributed over a number of diodes in such a way that each diode is optimally pumped. Encouraging results of an array of four planar diodes for a balanced doubler giving an output power of 5.5 mW at 320 GHz was published [4,5]. The integration of multiple diodes adds a degree of freedom in finding the optimal pumping level for each diode and can, therefore, handle more power, when distributed over the diodes.

The overwhelming majority of the frequency multipliers reported so far have utilised waveguide, stripline, or coaxial structures for tuning and filtering at the input, output, and idler frequencies [6]. This approach has proven useful for frequency multipliers at output frequencies up to 1000 GHz. But, the small dimensions of the waveguides limit the number of diodes which can be embedded. It is evident that the higher the output frequency the more difficult the mounting and realisation, especially if it is required that the multiplier be tuneable over a wide frequency range.

The open structure approach can overcome this limitation using quasi-optical elements for idler and output frequency tuning and filtering. This approach is eminently suited to local oscillators (LO) applications in millimetre and submillimetre-wave systems in which quasi-optical diplexing structures are commonly employed.

Through phase coherent pumping of multiple diodes, the maximum available power is distributed optimally over the diodes. The multiplied frequency is then coupled to the antennas and directed towards the desired direction. The principle of quasi-optical power combining is based on the constructive interference of the output signal in a given direction and can be achieved by integrating planar antennas with the tripler elements, where the spacing between the elements has to be selected accordingly [7].

3 Design of the Integrated Tripler Chip

The active element used for frequency tripling here is a pair of back-to-back Schottky varactor diodes. The symmetry, arising from the anti-serially (cathode-to-cathode) connected varactor diodes, results in an efficient odd harmonic generation forgoing idler circuits for the even harmonics. This simplifies the circuit design of these multipliers due to the significant reduction of the number of idler circuits as well as the elimination of the bias line [6].

The diode parameters were chosen according to the standard values for this application. The anode size is 3 μm , the doping level of the active n-layer is 10^{17} cm^{-3} , and the thickness is 300 nm.

The folded dipole antenna couples the fundamental frequency to the diode pair. The third harmonic generated in the diode pair is radiated by the same antenna. For maximum

power transfer, this antenna is matched to the diode pair at the fundamental frequency as well as at the tripled frequency. Additionally, this antenna functions as an idler termination for the harmonics higher than the third.

Besides the larger radiation resistance, the folded dipole antenna causes a DC short-circuit which consequently sets the operation point of the diode pair at 0 V.

It is intended to fabricate three different antenna lengths. These are 250 μm , 500 μm , and 800 μm which provide a large radiation resistance as well as an inductive load to match the diode pair at the fundamental and third harmonic.

The active area of the chip was chosen 1650 x 1650 μm^2 to match the Gaussian beam waist, focused by the first Teflon lens. This area contains 30 anti-serial diode pairs integrated with folded dipole antennas.

The DC short-circuit imposed by the folded dipole antennas makes it impossible to test the integrated anti-serial diodes using the probes. Therefore, 12 test structures are placed around the active area each consisting of a diode pair connected to two pads.

4 Device Fabrication

The wafer material consists of a 500 μm semi-insulating GaAs substrate followed by a 140 nm thick GaInP etch-stop layer, a 3 μm conductive n^+ -layer, and a 300 nm thick 10^{17}cm^{-3} doped n-layer. The active layer is passivated with a 300 nm SiO_2 layer. The wafer is wet-chemically thinned to 80 μm . This thickness caters for sufficient mechanical stability and simultaneously reduces the substrate waves.

After defining the anodes by ultraviolet contact lithography, the SiO_2 is then RIE-etched. After removing 10 to 20 nm of the active layer by anodic pulse etching [2], the Schottky contact is plated in-situ using the anodic pulse deposition technique [3]. To isolate the diodes, a photoresist circle is left on each anode pair, the exposed passivation is removed, and the active and conductive layers are wet-chemically etched leaving $3.6 \mu\text{m}$ high mesas. The GaInP etch-stop layer is then selectively etched with respect to GaAs.

The antennas and airbridge pillars are patterned on the $4 \mu\text{m}$ thick photoresist. The seed layer, consisting of 10 nm Chromium and 35 nm Gold, is then evaporated. The airbridges and antennas are transferred to a photoresist mask and electrochemically plated to a thickness of $2 \mu\text{m}$. The airbridges and antennas are completed after a lift-off process.

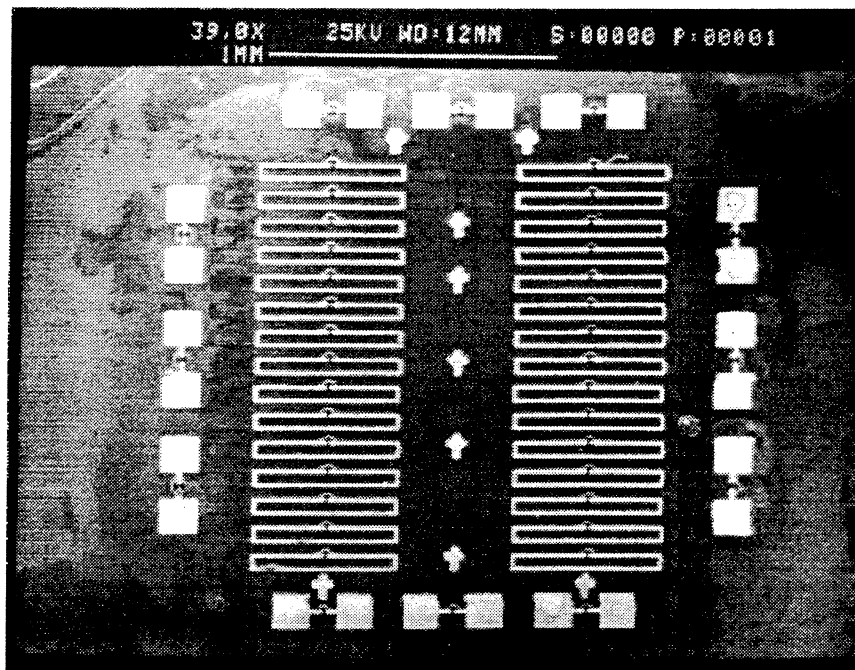


Fig. 1: Quasi-optical tripler chip with integrated folded dipole antennas and test structures

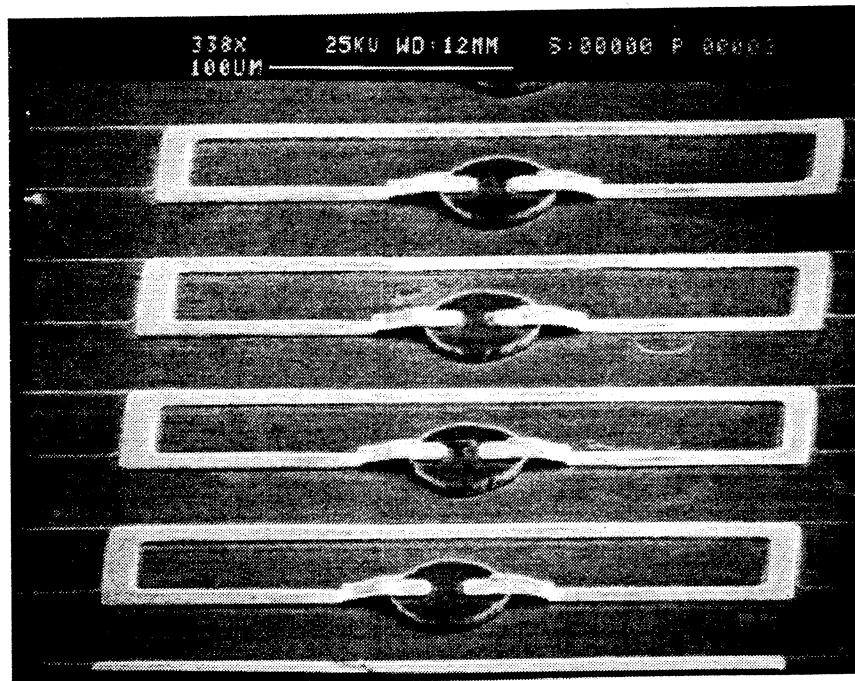


Fig. 2: SEM micrograph of four folded dipole antennas connected to the diode pairs via 4 μm high airbridges

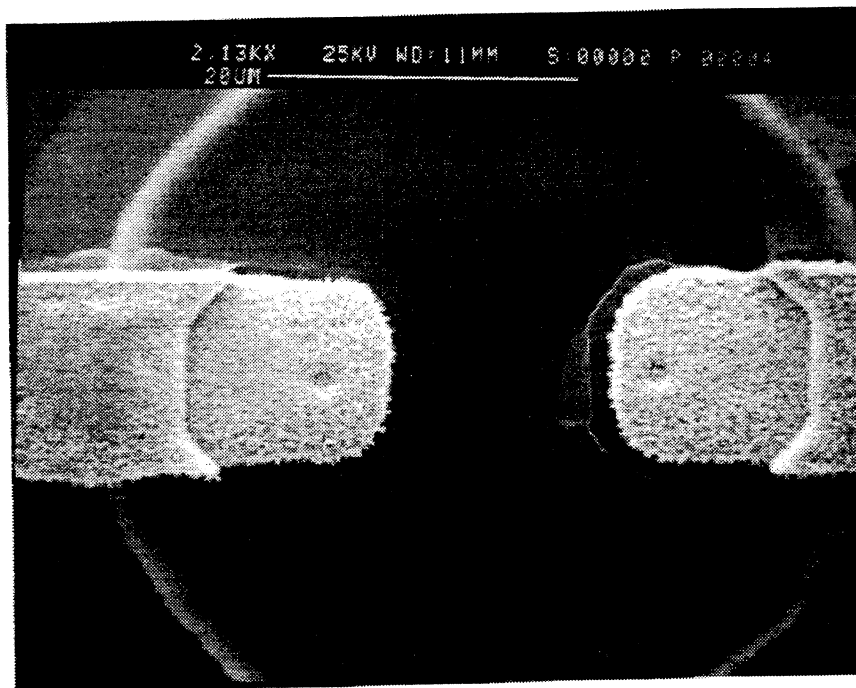


Fig. 3 Anode pair connected to the airbridges (anode diameter 3.3 μm)

Fig. 1 depicts the active area filled with 30 diode pairs integrated with folded dipole antennas. The 12 test structures are distributed on the margin of the active chip area. Fig. 2 shows four diode pairs connected to the antennas via airbridges. The airbridges are 40 μm long, 10 μm wide, and 2 μm thick. Fig. 3 shows a close-up of a 3.3 μm anode pair.

5 Characterisation

The measured current/voltage characteristics (fig. 4) demonstrate perfect anti-symmetrical behaviour. The breakdown voltage is $V_B = \pm 11.8 \text{ V}$, and the junction resistance at zero voltage is $R_{j0} = 3 \text{ G}\Omega$. The measured reverse current is less than 100 pA over a wide range which indicates the good quality of the Schottky barrier. The measured pad-to-pad capacitance versus voltage characteristics have shown the expected symmetrical behaviour. The measurements were performed at 1 MHz. The parasitic capacitance arising from the contact pads was determined by measuring a test structure with an open-circuited airbridge contact. A value of $C_p = 23 \text{ fF}$ has been obtained and subtracted from the pad-to-pad measurement. The C/V characteristics of a single diode pair is shown in fig. 5. The maximum variation of the capacitance is near zero bias, which is in agreement with theory. Also the ratio $C_{\text{max}}/C_{\text{min}}$ can be deduced from fig. 5.

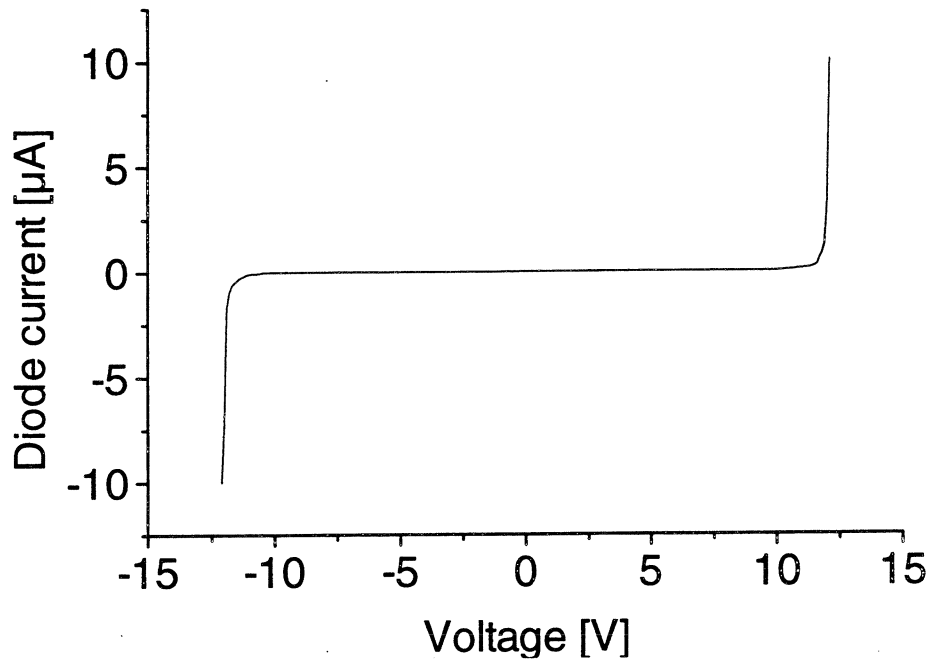


Fig. 4: Measured I/V characteristics of a anti-serial diode pair

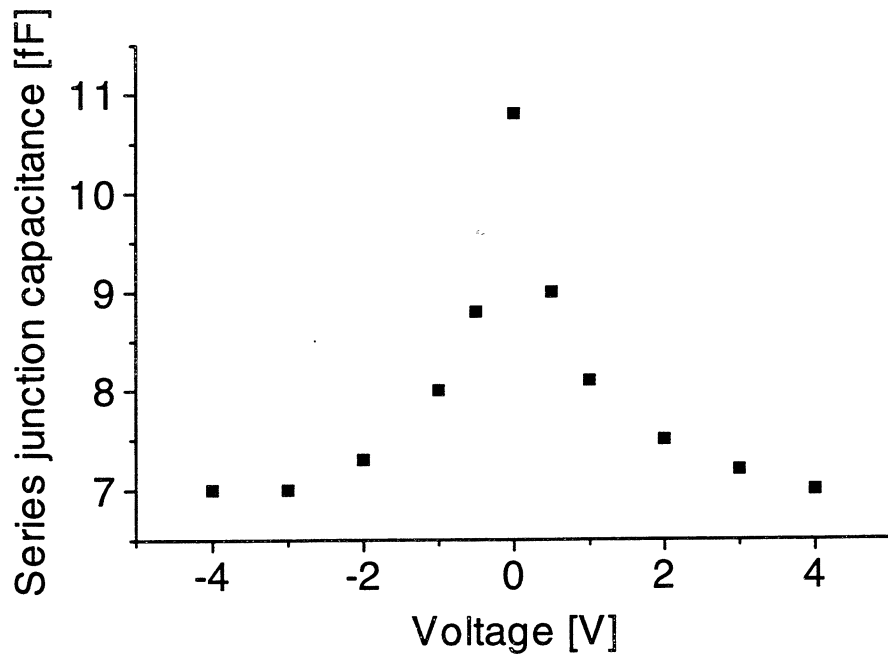


Fig. 5: Characteristics of a diode pair

6 RF Measurement Setup

In collaboration with the Universität Erlangen-Nürnberg, this tripler chip will be characterised. A 145 GHz Klystron oscillator generates an input fundamental power up to 500 mW. The beam is focused on the front side of the tripler array of 30 elements using Teflon lenses, and the output frequency is radiated from the rear side and coupled into a subharmonic mixer via a second Teflon lens [1].

An input band pass filter in the measurement setup will only pass the fundamental frequency while reflecting the output frequency. This filter can be used for output matching. An output dichroic plate prevents the input frequency from propagating to the corner-cube detector and is also used for input matching (fig. 6).

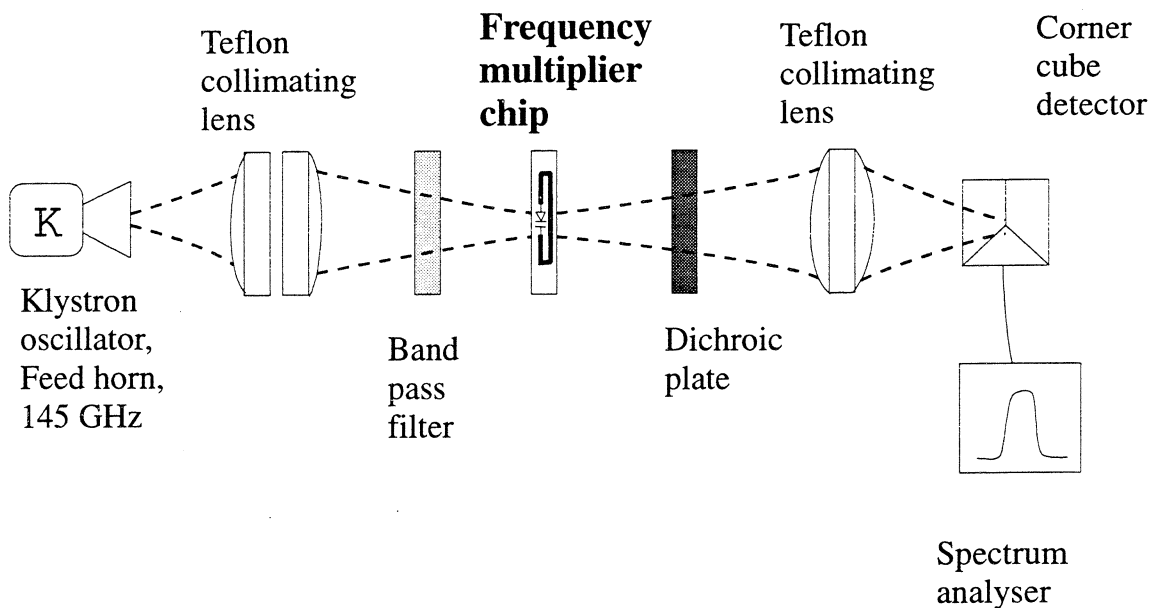


Fig. 6: Measurement setup of the integrated quasi-optical frequency tripler

7 Conclusion

A new design for a quasi-optical tripler has been presented. The fabrication process consists of standard techniques providing high reliability and yield. The novel approach is based on the folded dipole antennas which are used to enhance the coupling efficiency between the varactor diode pairs and the Gaussian beam. This open structure design reduces the formation of substrate waves by decreasing the thickness of the chip, whereas the full elimination of substrate waves can be achieved by completely removing the substrate and suspending the structure on a thick polyimide film. The tripler chips were fabricated and characterised by I/V and C/V measurements. Perfect anti-symmetrical I/V and symmetrical C/V characteristics were measured indicating the suitability of the diodes for the envisaged application. The radio frequency performance evaluation is still under way.

8 Acknowledgements

The authors would like to thank the "Deutsche Forschungsgemeinschaft" for funding this project, which aims at fabricating integrated submillimetre frequency multipliers for solid-state local oscillators.

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