# Design of Planar Varactor Frequency Multiplier Devices with Blocking Barriers *

U. Lieneweg, T. Tolmunen, M. Frerking, and J. Maserjian
Jet Propulsion Laboratory, California Institute of Technology
Pasadena, CA 91109

**Abstract**

Design principles for optimization of planar frequency triplers with symmetrical $C-V$ curves are presented. Role and limitation of various blocking barriers (oxide, Mott, heterojunction) are discussed. Devices with undoped drift regions (BIN+) have moderate efficiency but a broad range of power operation, whereas devices with doped drift regions (BNN+) have high efficiency in a narrow power window. In particular, an upper power limit of the BNN+ is caused by electron velocity saturation. Implementations in $SiO_2$/Si and AlAs/GaAs and means for increasing the power of BNN+ structures are considered.

In contrast to conventional varactor diodes with a Schottky barrier, diodes with a Mott or heterojunction barrier (B) allow one to construct devices with a symmetric capacitance-voltage ($C-V$) characteristic of high Cmax/Cmin ratio by connecting two diodes back-to-back. Each diode is constructed, top to bottom, of a Schottky metal contact, the

*This work was performed at the Jet Propulsion Laboratory, California Institute of Technology, with support from the Director's Discretionary Fund and under contract with the Army Research Office.

barrier with a thickness $d_{bar} \approx 10 \ldots 30$ nm, an $N$-type doping sheet, a drift region $d_{drift} \approx 50 \ldots 150$ nm, and an $N^+$ back contact. This construction leads naturally to a planar back-to-back configuration with no ohmic contacts. No bias is required as the sheet doping controls the operating point of the diodes. A simple planar process is desirable for construction of highly reliable integrated multiplier structures with high yield for multidiode arrays. Fig. 1 shows the device structure and its equivalent circuit. Thanks to the favorable geometry the parasitic series resistance is minimal and does not degrade due to skin effect. Isolation can be achieved by mesa etching and deposition of $SiO_2$. An optional etch stop layer allows the removal of the substrate for minimizing the parasitic capacitance and transmission line losses of the leads.

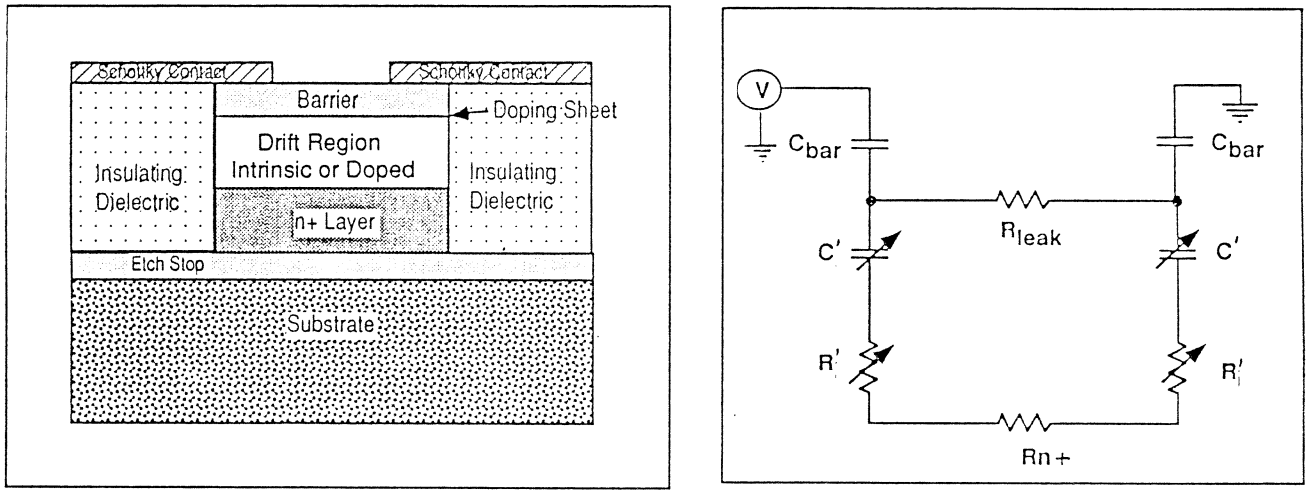


Figure 1: Planar blocking barrier varactor: cross section and equivalent circuit

If the drift region is intrinsic (I), electrons injected from the $N^+$ back contact carry a space charge limited current with a transit time limited frequency response (BIN+ diode) [1]. The $C - V$ characteristic in this case has a steep transition, $(\mathrm{d}C/\mathrm{d}V)/C = q/kT$, between $C_{min}$ and $C_{max}$ enabling to generate a frequency spectrum of high harmonic content suitable for triplers, quintuplers, etc. at low power levels. The validity of the BIN+ concept was proven earlier with a single $SiO_2$/Si diode operating as a frequency

doubler in a waveguide mount [2] and performing closely to the predictions of a large signal analysis for a stepfunction $C - V$ [3]. A similar theory for pulse-like $C - V$, as exhibited by back-to-back BIN+ diodes, was developed by the same group [4] but proved to be unrealistic. Therefore we resorted to a simulator [5], shown in Fig. 2, which optimizes the embedding impedances at input and output frequencies for an arbitrary $C(V_C)$ curve, a fixed series resistance $R$, and a given input power $P_{in}$ in order to find the maximum output power $P_{out}$.

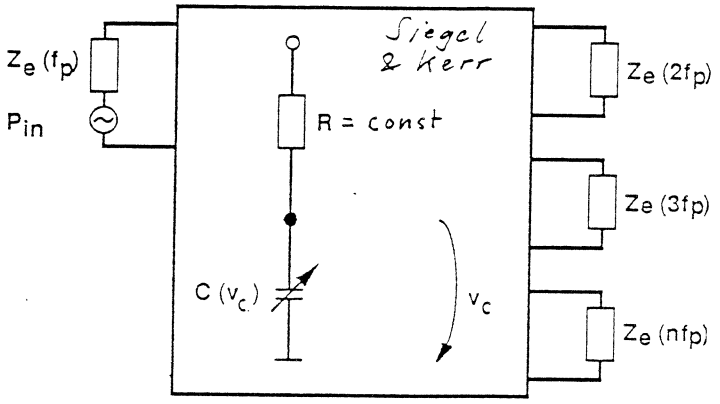


Figure 2: Varactor multiplier signal simulator with embedding impedances $Z_e$ at fundamental $f_p$ and harmonics. For tripler $\Re\{Z_e(nf_p)\} \gg R$ for $n = 2, 4, 5, 6, 7$ was chosen. Simulator maximizes output power by optimizing $Z_e(f_p) = R_1 + jX_1$ and $Z_e(3f_p) = R_3 + jX_3$.

Fig. 3 shows a schematic $C - V$ curve from a back-to-back BIN+ with its characteristic values related to physical diode properties as follows. The maximum capacitance is reached when both diodes are in accumulation, whereas at the minimum capacitance one diode is in accumulation and the other fully depleted, leading to

$$C_{max} = C_{bar}/2 \tag{1}$$

and

$$C_{min} = \frac{C'_{min} C_{bar}/2}{C'_{min} + C_{bar}/2} \tag{2}$$

with $C_{bar} = \epsilon_{bar} A/d_{bar}$ and $C'_{min} = \epsilon_{drift} A/d_{drift}$, where $A$ is the area of each single diode. The halfwidth of the $C - V$ curve is close to $2V_f$, where $V_f$ is called flatband voltage because at that voltage the field at the barrier is zero, marking the transition between accumulation and depletion of the drift region. The flatband voltage is determined from the sheet doping $N_{sheet}$ together with the barrier height at the metal interface, $\Phi_M$, the barrier height at the interface with the drift material, $\Phi_D$, and a small potential step at the border between drift and $N^+$ region $\Phi_{N+}(\approx 0.1$ V at room temperature) as

$$V_f = qN_{sheet} d_{bar}/\epsilon_{bar} + \Phi_D - \Phi_M + \Phi_{N+}. \tag{3}$$

As the capacitance changes, the series resistance changes,too, as shown in the figure. The maximum,

$$R_{max} = 2R'_{max} + R_{N+}, \tag{4}$$

is the resistance of both drift regions in accumulation plus the parasitic series resistance, whereas the minimum,

$$R_{min} = R'_{max} + R_{N+}, \tag{5}$$

is the resistance of only one accumulated diode plus parasitic because the other diode is fully depleted. As a reasonable average value we have used $R = 1.5R'_{max} + R_{N+}$ in the simulations. For the BIN+ one obtains [6]

$$R'_{max} = d^2_{drift}/2\epsilon_{drift} v_s A, \tag{6}$$

where $v_s$ is the electron saturation velocity.

Fig. 4 shows a simulated result for a tripler to 200 GHz. For a given halfwidth $2V_f$ the efficiency $\eta$ peaks at a certain input power with the peak shifting to higher powers,

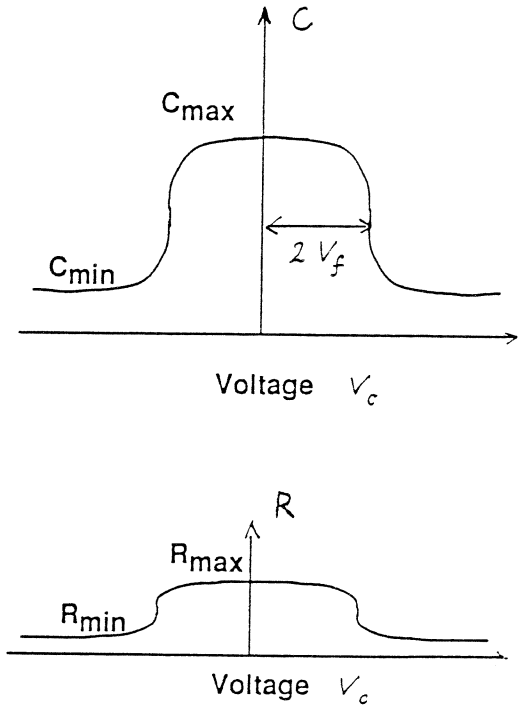


Figure 3: Capacitance and series resistance of back to back BIN+ diodes as function of voltage drop over capacitance. Halfwidth equals twice the flatband voltage of single diode.

broadening, and reaching a saturation value for larger halfwidths. Furthermore, the input power is related to the peak voltage drop over the capacitance, $\hat{V}_C$, by $P_{in} \propto \hat{V}_C^2$. The condition for maximum efficiency, obtained from many simulations, can be described by

$$2V_f = 0.6\frac{C_{min}}{C_{max}}\hat{V}_C, \tag{7}$$

where $2V_f$ should be much larger than $kT/q$ for a BIN+ structure.

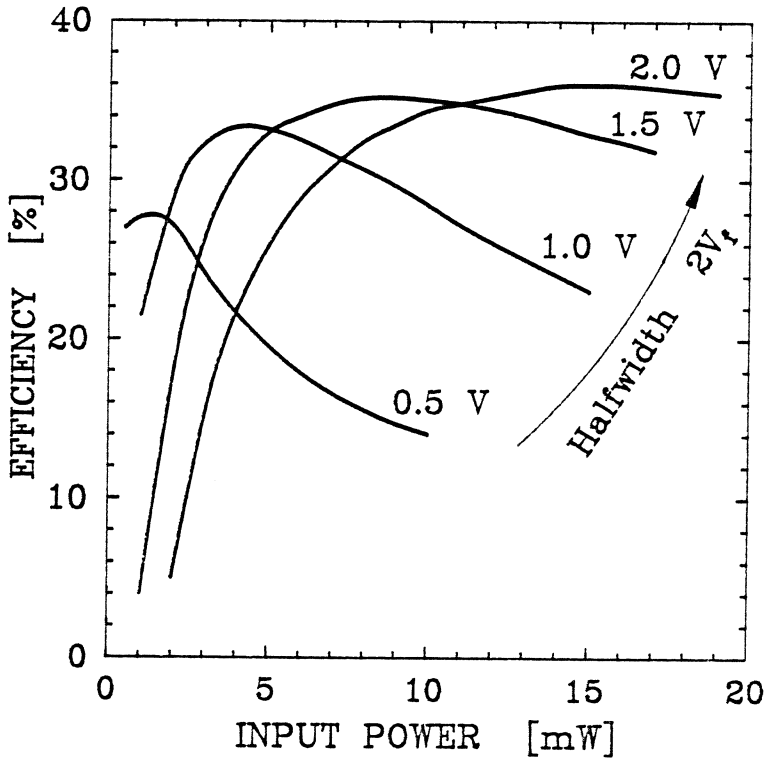


Figure 4: Simulated efficiency for BIN+ tripler to 200 GHz as function of input power with halfwidth of $C - V$ as parameter. $C_{max} = 15$ fF, $C_{min} = 5$ fF, $R = 20\ \Omega$.

The question of what limits $\hat{V}_C$ is investigated in Fig. 5. Here the conduction band edge of a back-to-back BIN+ structure with Mott barriers has been plotted from a d.c. PISCES [7] calculation. The fields are high in the reverse biased and low in the forward biased diode as long as the input frequency is much smaller than the cut-off frequency.

We define now "breakdown" by the following conditions: The forward biased barrier exhibits a leakage current of density, see, e.g., [8],

$$j_{TE} = \frac{4\pi q m_{bar} k^2 T^2}{h^3} \exp[-\frac{q\Phi_B}{kT}], \tag{8}$$

which is caused by thermionic emission (TE) over the barrier with $m_{bar}$ being its effective mass and $\Phi_B$ its effective height. The leakage current in the reverse biased barrier is dominated by Fowler-Nordheim (FN) tunneling with a density [8]

$$j_{FN} = \frac{m_0}{m_{bar}} \frac{q^3 E_{bar}^2}{8\pi h \Phi_M} \exp\{-\frac{8\pi\sqrt{2m_{bar}}q\Phi_M^{3/2}}{3hE_{bar}}\}, \tag{9}$$

which, in contrast to the thermionic current, is a strong function of the the field in the reverse biased barrier, $E_{bar} > 0$.

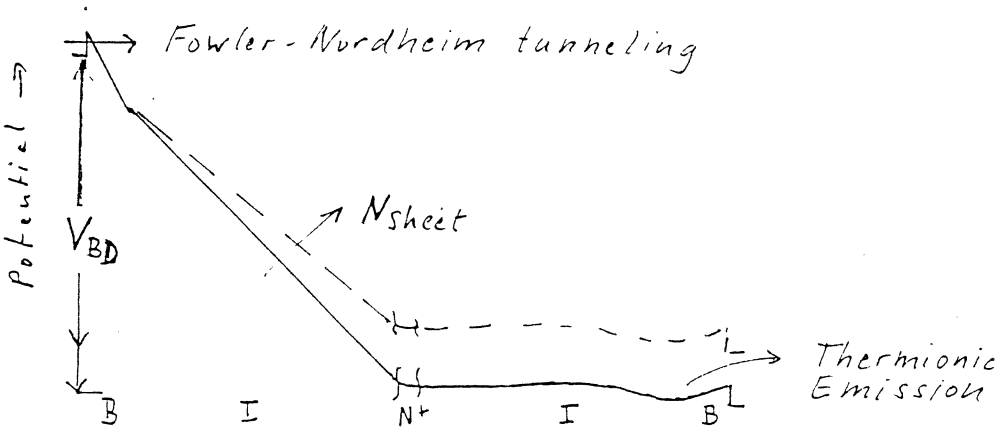


Figure 5: Potential distribution in back-to-back BIN+ at breakdown, voltage $V_{BD}$, caused by tunneling through reverse biased barrier. Increased sheet doping decreases $V_{BD}$.

Postulating that the FN current becomes nearly equal to the TE current by equating the exponents of Eqs. (8) and (9) leads to the barrier breakdown field

$$E_{bar,BD} = \frac{8\pi\sqrt{2m_{bar}q\Phi_M}}{3h} \frac{\Phi_M}{\Phi_B} \frac{kT}{q} \tag{10}$$

$$= \frac{1.7\times10^6}{\mathrm{V}^{1/2}\mathrm{cm}}\sqrt{\frac{m_{bar}}{m_0}\Phi_M}\frac{\Phi_M}{\Phi_B} \text{ at } T = 300 \text{ K}. \quad (11)$$

The above derivation of the breakdown holds not only for (triangular) Mott barriers but also for the trapezoidal heterojunction and oxide barriers as long as these barriers are not so thin that the current tunnels through the full barrier at breakdown,i.e., $\Phi_M - E_{bar,BD}d_{bar} \leq 0$ must be fulfilled.

The breakdown voltage of a single diode is related to the barrier breakdown field by

$$V_{BD,s} \approx E_{bar,BD}(\frac{\epsilon_{bar}}{\epsilon_{drift}}d_{drift}) - \frac{qN_{sheet}}{\epsilon_{drift}}d_{drift} + \Phi_D - \Phi_M. \quad (12)$$

Applying $Q = \int C\mathrm{d}V$ to the single and the back-to-back diodes, the breakdown voltage of the latter becomes

$$V_{BD} \approx \frac{C_{min,s}}{C_{min}}(V_{BD,s} - V_f) + 2V_f \quad (13)$$

with

$$\frac{C_{min,s}}{C_{min}} = \frac{d_{bar}}{d_{bar} + d_{drift}} + 1. \quad (14)$$

Note the decrease of $V_{BD}$ with increased sheet doping as illustrated in the figure.

Table 1 lists the properties of various barriers starting with the simple GaAs Mott barrier, suitable only for low power applications, and progressing to AlGaAs/GaAs with about 50% Al, AlAs/GaAs, and $SiO_2$/Si.

With these parameters and the maximum allowed voltage drop over the capacitance, $\max(\hat{V_C})$, set equal to $V_{BD}$, the results for the AlGaAs/GaAs heterojunction barrier tripler in Table 2 have been obtained. Since already $V_f \approx 1$ V, the effective height of the forward biased heterojunction barrier, $\Phi_B$, was set to $\Phi_D$. The area has been chosen to achieve matchable impedance levels.

If bulk doping $N$ is added to the drift region (BNN+ diode), the current is no longer space charge limited, and the cut-off frequency becomes intrinsically determined

Table 1: Properties of various barriers

| Barrier Type | Material | Drift Region | $\Phi_M$[V] | $\Phi_D$[V] | $m_{bar}/m_0$ |
|---|---|---|---|---|---|
| Mott | GaAs | GaAs | 0.8 | 0 | 0.07 |
| Heterojunction | AlGaAs | GaAs | 1.2 | 0.4 | 0.10 |
| Heterojunction | AlAs | GaAs | $\Gamma$: 2.0 | 1.0 | 0.15 |
| | | | X: 1.4 | 0.6 | 0.19 |
| Oxide | $SiO_2$ | Si | 3.2...4.1 | 3.2 | 1.0 |

Table 2: Simulated Performance of a AlGaAs/GaAs BIN+ Tripler to 200 GHz

| | |
|---|---|
| $d_{bar}$ [nm] | 20 |
| $d_{drift}$ [nm] | 80 |
| $N_{sheet}$ [$cm^{-2}$] | $5.5 \times 10^{12}$ |
| $A$ [$\mu m^2$] | 6 |
| $C_{max}$ [fF] | 15 |
| $C_{min}$ [fF] | 5 |
| $R$ [$\Omega$] | 20 |
| $2V_f$ [V] | 2.0 |
| $\hat{V}_C$ [V] | 11.5 |
| $P_{in}$ [mW] | 19 |
| $\eta$ [%] | 35.5 |
| $P_{out}$ [mW] | 6.7 |
| $R_1$ [$\Omega$] | 48 |
| $X_1$ [$\Omega$] | 300 |
| $R_3$ [$\Omega$] | 35 |
| $X_3$ [$\Omega$] | 50 |

by dielectric relaxation. The transition from the first mechanism to the second occurs when the Debye length $L_{Debye} = \sqrt{2\epsilon_{drift}kT/q^2N}$ becomes less than $d_{drift}$ [9]. As a side effect, the transition from high to low capacitance becomes more gradual. This should have little effect on tripling for high enough powers as long as the diodes "punch through", i.e., the maximum depletion width reaches $d_{drift}$. If punch through is reached exactly when the barrier breaks down, then

$$V_{BD,s} \approx E_{bar}(\frac{\epsilon_{bar}}{\epsilon_{drift}}\frac{d_{drift}}{2} + d_{bar}) - \frac{qN_{sheet}}{\epsilon_{drift}}\frac{d_{drift}}{2} + \Phi_D - \Phi_M, \tag{15}$$

i.e., a reduction of almost a factor 2 in comparison to the BIN+, if $N_{sheet}$ is not reduced.

Table 3 summarizes differences between BIN+ and BNN+ structures with the intrinsic cut-off frequency defined as

$$\omega_{ci} = 1/R'_{max}C'_{min}. \tag{16}$$

Table 4 gives numerical values for the intrinsic cut-off showing the superiority of GaAs BNN+ at low fields. Unfortunately the relaxation time degrades when the field in the drift region exceeds the critical field. The formulas given in Table 3 are based on a simple monotonous model for the field dependent mobility

$$\mu(E) = \frac{\mu}{1 + E_{drift}/E_{crit}} \tag{17}$$

with $E_{crit} = v_s/\mu$. Estimates of the value of the average electron velocity in 100 nm GaAs layers range from $0.6 \times 10^7$ cm/s for space averaging [10] to $3 \times 10^7$ cm/s for time averaging[11]. A simulation for transit time devices [12] gave values $1 \ldots 2 \times 10^7$ cm/s.

In our large signal simulations it was easier to monitor the total current rather than the field in the drift region. Since the current reaches 1/2 of its saturation value at the critical field , cf. $\mu(E)$, this should be the maximum current allowed to flow in the diode

Table 3: Comparison of BIN+ and BNN+ diodes

| BIN+ ($L_{Debye} \gg d_{drift}$) | BNN+ ($L_{Debye} \ll d_{drift}$) |
|---|---|
| Steep transition | Gradual transition |
| $(\mathrm{d}C/\mathrm{d}V)/C = q/kT$ | $C \propto 1/\sqrt{V}$ |
| High harmonic content | 3rd harmonic little affected |
| at low power | at high power |
| Space charge $n(x, V)$ injected | $n = N$ in undepleted drift region |
| into drift region from N+ | $n = 0$ in depleted part |
| $R'_{max} = d^2_{drift}/2\epsilon_{drift} v_s A$ | $R'_{max} = d_{drift}(1 + E_{drift}/E_{crit})/qN\mu A$ |
| Transit time limited response | Relaxation time limited response |
| $\omega_{ci} = 2v_s/d_{drift}$ | $\omega_{ci} = 1/\epsilon\rho(1 + E_{drift}/E_{crit})$ |
| for $E_{drift} > E_{crit} = v_s/\mu$ | with $1/\rho = qN\mu$ |

Table 4: Calculated intrinsic cut-off frequency for $d_{drift} = 100$ nm and $N = 10^{17}/\mathrm{cm}^3$

| | $\epsilon/\epsilon_0$ | $\mu(N)$ [$\mathrm{cm}^2$/Vs] | $v_s$ [cm/s] | $E_{crit}(N)$ [kV/cm] | $f_{ci}$(BIN+) [GHz] | $f_{ci}$(BNN+) [THz] |
|---|---|---|---|---|---|---|
| Si | 12 | 700 | $1 \times 10^7$ | 15 | 300 | 1.5 |
| GaAs | 13 | 4500 | $1 \ldots 2 \times 10^7$ | 2...4 | 300...600 | 8.6 |

without serious degradation in the frequency response. Fig. 6 shows results of a back-to-back AlGaAs/GaAs BNN+ tripler with $N = 1 \times 10^{17}$ cm$^{-3}$, $d_{bar} = 20$ nm, $d_{drift} = 100$ nm, $N_{shcet} = 4 \times 10^{12}$ cm$^{-2}$, and $A = 13$ $\mu$m$^2$. The maximum current is calculated as

$$I_{sat}/2 = qNv_sA/2 = 20 \text{ mA}. \tag{18}$$

This restricts the input and output powers to $P_{in} < 2$ mW and $P_{out} < 0.8$ mW, which is clearly below the optimum. Increasing the doping to $2.5 \times 10^{17}$ cm$^{-3}$ would increase the maximum current to 50 mA and input and output power to about 10 mW and 5.5 mW, respectively, if we use the curves in Fig. 6 for scaling. Qualitatively, the degradation of the efficiency due to the smear-out of the $C - V$ should be offset by the higher cut-off frequency due to the reduction in the intrinsic part of the series resistance. A still higher doping would cause the peak voltage exceed the breakdown limit, cf. Table 2.

As a consequence, the output power of the BNN+ is not higher than that of the BIN+ although the efficiency is. The power levels ($\propto A$) could be increased by increasing the area $A$ if lower impedance levels ($\propto 1/A$) could be matched. Another approach would be to replace each BNN+ diode by a stack of several back-to-back BNN+'s in series in order to bring the impedance up again. Actually, no metal or N+ layers would be necessary between barriers in each stack. The device approaches then the configuration of a stack of single barrier varactors [13] while preserving the planarity with Schottky contacts at the surface barriers.

We are presently implementing an AlAs/GaAs BNN+ tripler to 200 GHz with a target of 5 mW output power in a waveguide configuration with flip-mounting of a thinned chip to a quartz substrate, which carries the filter and coupling structures. We are also collaborating with Prof. N. C. Luhman and his students at UCLA on a quasioptically coupled tripler array with an integrated antenna structure using the AlAs/GaAs system. Our analysis shows, however, that the $SiO_2$/Si BIN+ system should be revisited because

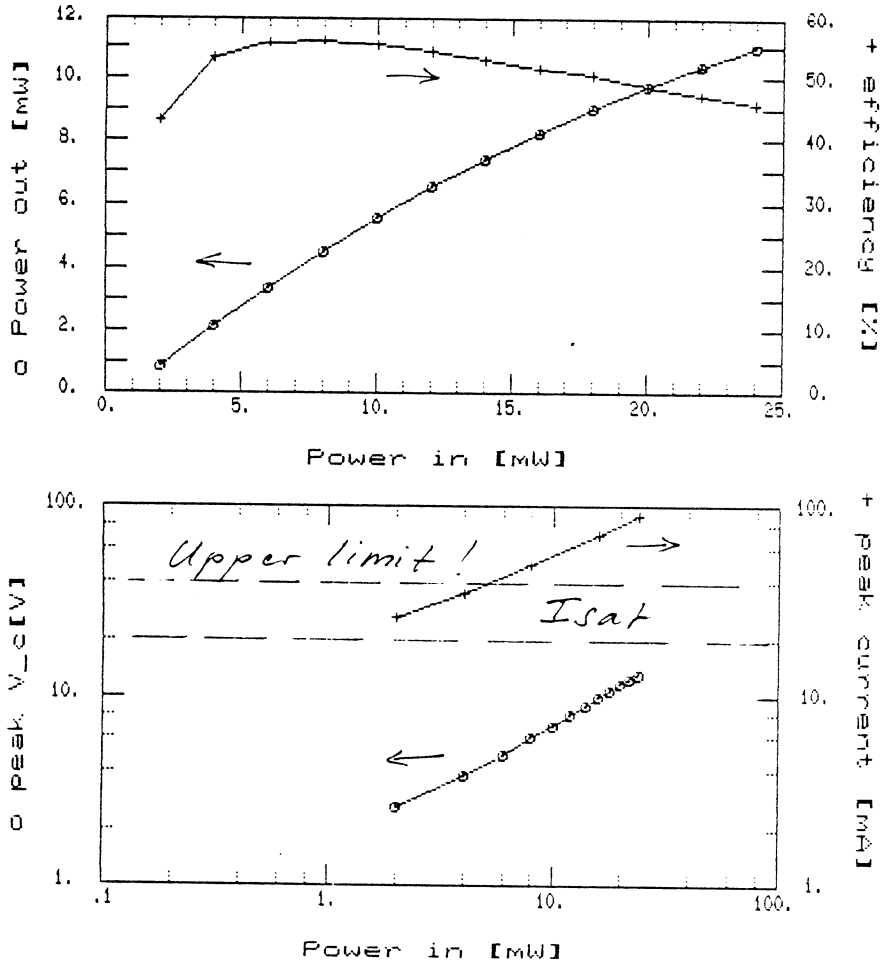


Figure 6: Simulated performance of BNN+ tripler. $C_{max} = 30$ fF, $C_{min} = 11$ fF, $R = 5\ \Omega$

of the theoretically superior breakdown resistance of the thin, grown oxide with no loss in saturation current at high fields in comparison to GaAs. Earlier experienced low yields due to oxide pinholes should be overcome due to improved cleanroom control.

## ACKNOWLEDGEMENT

The heterojunction devices are being fabricated in the Microdevices Laboratory of the Center for Space Microelectronics Technology at JPL. We thank B. Hancock, K. Delgadillo, and J. Rosenberg for their efforts.

## REFERENCES

1. U. Lieneweg and J. Maserjian, 6th Intern. Conf. IR & MM Waves, Miami, 1981

2. C. Jou, Ph.D. Thesis, Electr.Sc., UCLA (1987)

3. K. Schunemann and B. Schiek, A. E. U. (German) 22, 293 (1968)

4. B. Schiek and J. Marquard, A. E. U. (German) 24, 237 (1970)

5. P. H. Siegel, A. R. Kerr, and W. Hwang, NASA Technical Paper 2287 (1984)

6. D. P. Howson, B. Owen, and G. T. Wright, Solid St. Electron. 8, 913 (1965)

7. M. R. Pinto, C. S. Rafferty, H. R. Yeager, and R. W. Dutton, PISCES IIB, Stanford Electronics Laboratory (1985)

8. A. van der Ziel, Solid State Physical Electronics, 3rd ed., Englewood Cliffs (1976)

9. U. Lieneweg and J. C. Bean, Solid St. Electron. 27, 867 (1984)

10. D. S. Pan, UCLA, private communication

11. G. J. Iafrate, in Gallium Arsenide Technology (D. K. Ferry, Ed.), Indianapolis (1985)

12. R. O. Grondin, P. A. Blakey, and J. R. East, IEEE Trans. ED-31, 21 (1984)

13. cf. papers presented by H. X. L. King and E. Kollberg at this symposium