RECENT DEVELOPMENT OF BARRIER-INTRINSIC-N+ (BIN) DIODE FREQUENCY TRIPLER

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Abstract

Potential problems of the back-to-back GaAs Barrier-Intrinsic-N+ (BIN) diode tripler concept along with the associated device physics will be presented in this paper. The back-to-back GaAs BIN diode structure was originally proposed to have an intrinsic cut-off frequency close to 1 THz and be a highly efficient millimeter-wave frequency tripler device [1-3]. The device frequency limitations will be discussed to explain the failure of the GaAs BIN diode as a millimeter wavelength device.

Introduction

Recently, a novel metal-semiconductor homostructure, the Barrier-Intrinsic-N+ (BIN) diode structure, in which the capacitance switches rapidly between two values and behaves in a similar fashion to the punch through diode, has been proposed as a highly efficient millimeter-wave frequency tripler [1-3]. The nonlinear element of a punch through diode is a capacitor with a step-like transition in the C-V characteristics. An analytical study of the multiplication efficiency of the punch through diode was carried out and compared to that of the varactor diode [4-6]. The results show that the punch-through diode is always more efficient than the junction varactor for the same cut-off frequency. To overcome the power limitations of a single-diode multiplier, spatial power combining [7] of

the outputs of large planar arrays of nonlinear frequency multiplication devices has been implemented by the design of a diode grid [8,9]. The BIN diode concept has been adapted for the construction of diode-grid frequency tripler arrays [10,11]. Thousands of GaAs BIN diodes were integrated with a periodic grid in this approach to investigate the possibility of producing watt-level CW output power in the millimeter-wave region. This is an attractive approach to combine the power of each distributed device using monolithic integrated circuit techniques, thereby, resulting in potentially low cost fabrication and small size realization. Ideally, this approach should provide inexpensive, watt-level CW solid-state sources in the millimeter-wave region.

In the last two years, fifteen GaAs BIN diode-grid frequency tripler arrays have been fabricated with high-frequency measurements performed on each wafer. The highest tripling efficiency obtained was 8.5% at an output frequency of 100 GHz [11]. This wafer was destroyed shortly after by pumping it with too much power. Efforts have been devoted to repeat this result with additional samples. It has not been possible to reproduce the results of this measurement; in fact, no output power has been detected at the frequency of 100 GHz from any of the other wafers. Through this study, however, it was noticed that power could be obtained at the output port (W-band detector) before the detector was shielded from the input source radiation. It was further observed that once the detector was sealed all around by absorbers the detected power disappeared. At least part of the results obtained from this particular sample are believed to be due to scattered power sensed by the diode detector since no effort had been taken to shield the detector from random radiation at that time. The cut-off frequency of these GaAs BIN devices was determined to be 600 GHz assuming an average drift velocity of 3×10^7 cm/sec. A maximum tripling efficiency of 24% at an output frequency of 100 GHz was, therefore, predicted for these GaAs BIN diode-grid tripler arrays [10]. It should be pointed out that the assumed measured tripling efficiency (8.5%) was even smaller than that from an equivalent diode structure using Si

material. The major thrust of this paper is to explore the potential problems and limitations of the back-to-back BIN diode frequency tripler.

Device Concept

The Barrier-Intrinsic-N^+ (BIN) diode incorporates a thin undoped semiconductor layer (I) on a heavily doped layer (N) serving as a back contact. On top of the undoped layer, there is an ultrathin electron-blocking barrier layer (B) in contact with a metal top layer [1-3]. This blocking layer can be formed by an insulator, a semiconductor with a very wide band gap, or a Mott barrier [1-3]. With the low doping region, the action of the device depends upon the charge which is injected from the substrate into the epitaxial layer under forward bias. The device can be switched rapidly between two capacitance states which correspond to accumulation of electrons at the barrier and depletion of the intrinsic layer, respectively, by the applied bias. This results in a highly nonlinear capacitance-voltage characteristic which is needed for efficient harmonic generation. The maximum cut-off frequency of the BIN diode is determined by the time it takes electrons to transit the epitaxial layer. With a thin epilayer, intrinsic cut-off frequencies close to 1 THz have been projected in GaAs material [2,3].

The construction of a BIN diode on a III-V compound semiconductor entirely by the Molecular Beam Epitaxy (MBE) growth process (shown in Fig. 1) has been described [2,3]. A Mott-barrier is formed by a thin intrinsic layer sandwiched between the top metal contact and a charge sheet created by selective doping. This structure eliminates the problem of low fabrication yield associated with the thin MOS structure [12]. In the proposed GaAs Mott-BIN diode frequency tripler concept [2,3], it was assumed that GaAs is always superior to silicon due to the higher mobility and maximum velocity which will reduce the transit time and render negligible the parasitic resistance of the back contact. Therefore, based on the arguments above, higher intrinsic cut-off frequencies should be achieved using this structure. For example, an ideal diode with a 1000 Å epilayer thick is

predicted to have a transit time of 0.3 ps and an intrinsic cut-off frequency of 960 GHz assuming a drift velocity of $3x10^7$ cm/sec [2,3]. The validity of the possibility of achieving terahertz cut-off frequencies is investigated in the next section.

RC Time Constant

To study the properties of a BIN diode, one needs to study the large-signal series resistance of the space charge varactor in detail. The basic action of the BIN diode varactor is the movement of mobile space charge into the epilayer under forward bias conditions and out of it under reverse bias conditions. As discussed in references 1 and 4, under high field conditions, i.e., when the electron travels most of the cycle with their saturation velocity, v_d, the series resistance from the epilayer can be calculated as follows:

$$R_{epi} = V_s/(2i) = d^2_{epi}/(2\varepsilon_s v_d A)$$

The losses in the bulk are described by the spreading resistance given by

$$R_{bulk} = \rho_B(t/A + s/(lt))$$

where ρ_B is the resistivity of the bulk, t is the thickness of the back contact layer, s is the spacing between two diodes, and l is the length of the active device.

Combining these two losses, the series resistance becomes

$$R_S = R_{epi} + R_{bulk}$$
$$= d^2_{epi}/(2\varepsilon_s v_d A) + \rho_B(s/(lt))$$

The capacitance of the epilayer, on the other hand, is given by

$$C_{epi} = \varepsilon_s A/d_{epi}$$

This results in an RC time constant expressed as

$$R_{max}C_{min} = R_S C_{epi} = \varepsilon_s A(d^2_{epi}/(2\varepsilon_s v_d A) + \rho_B(s/(lt)))/d_{epi}$$
$$= (d_{epi}/(2v_d) + \rho_B\varepsilon_s As/(d_{epi}lt))$$

The dependence of the RC time constant on the device area can be neglected when the back contact layer thickness is large and/or doping is high enough. In this case, one has

$R_{max}C_{min} = R_{epi}C_{epi} = d_{epi}/(2v_d)$

The $R_{max}C_{min}$ time constant is then mainly dependent upon the epilayer thickness and saturation drift velocity. If we assume that quasi-static approximation is valid here, then the upper limit on the maximum operation frequency for the BIN diode is roughly the inverse of the RC time constant or $2v_d/d_{epi}$ (a more exact value would be $v_d/(\pi d_{epi})$). It is then clear that the maximum operating frequency of a BIN diode is strongly dependent on the epilayer thickness and saturation drift velocity. It should be pointed out that the device geometry can improve the upper limit of the maximum operating frequency only when the resistivity of the back contact layer is large and/or the thickness of this layer is small.

Due to overshoot or ballistic motion, drift velocity values much higher than those corresponding to the final steady-state conditions can possibly be achieved in semiconductors. These phenomena, occurring under non-steady state conditions, might be achieved in submicron devices [13,14]. Thus, they can be used to strongly increase the velocity of the carriers with the objective to further reduce their transit time along the active region. Based on this type of study, one can argue that the average drift velocity in the thin epilayer of the BIN diode can be much higher than the steady-state saturation velocity. This possibility is carefully investigated below.

The average transient velocity versus distance for different values of electron energy was calculated by Iafrate et. al. using Monte Carlo techniques [13,14]. The calculation makes use of the assumption that the applied electric field is constant in time, and is assumed to be turned on instantaneously [13,14]. These results were used in a feasibility study on the BIN diode frequency tripler carried out by Lieneweg et. al. [2,3]. However, this situation is not expected to occur in a real device structure. Additional numerical results obtained by using a configuration where the electric field increases proportionally to time have also been reported [14]. For this case, which may roughly simulate the electric field applied to the carriers when travelling through the active region of a common

submicron device, the average velocity remains lower than that obtained by using a simple time step for the whole region considered.

The transit velocities achievable in gallium arsenide can be quite large, however, achievement of such high velocities does not only depend upon the injection energy and the transit distance, but also is highly sensitive to the electric field [13,14]. The average drift velocity distributions for different external electric field strengths have also been calculated by Iafrate et. al. using Monte Carlo techniques. This study shows the dramatic decrease of the average drift velocity as the external electric field strength increases. The physical explanation for this velocity versus distance behavior is simple. Initially, the electrons assume the small effective mass of the central Γ valley, whereupon they are accelerated by the electric field in the forward direction. For modest injection energies and electric fields, electrons suffer little intervalley scattering. However, for injection energies approaching the L and X minima and strong electric fields, the electrons are promoted to the high effective-mass satellite X and L valleys, and the strong intervalley scattering reduces the drift velocity of carriers after a relatively short transient distance.

With suitable electric field temporal dependences, it seems possible, by using the overshoot phenomenon, to strongly increase the carrier velocity during very short times, which in the spatial scale corresponds to submicron distances. Ruch first demonstrated the velocity overshoot effect by calculating the transient response of carriers in a temporal electric field step function by the the Monte Carlo method [15-17]. In order to relate his results more pertinently to device performance, he plotted the result versus distance. The distance was obtained by integrating the ensemble velocity over time. This practice was used in many subsequent works [13,14]. However, it is somewhat misleading because most of these works were simulations of temporal velocity overshoot only but were often used as spatial overshoot.

Pan et. al. [18] clarified the significant difference between the spatial velocity overshoot and the temporal overshoot and presented the simulated spatial velocity

overshoot results for Si semiconductors. The physical condition for the temporal velocity overshoot should be a large homogeneous sample with a uniform electric field suddenly turned on. Any transient diffusional effect will be cancelled in the current because of the homogeneity of the situation. On the other hand, if a spatial step function of electric field is applied to a sample, the carrier's average velocity may show an overshoot over a short distance near the step of the electric field. In general, this spatial velocity overshoot should not be obtained from the temporal velocity overshoot by the simplified transformation. This is because transient diffusional effect should play an important role in this case. Differences between the temporal and spatial overshoot are found by Pan et. al. to be of a factor as large as three to five for Si [18].

No direct determination of the drift velocity can be achieved since the current depends not only on the carrier velocity, but also on the number of carriers injected into the active region. In addition, the presence of parasitic elements, such as series resistances, can introduce spurious effects which are difficult to fully and properly account for. In conclusion, the average drift velocity for GaAs semiconductor (3×10^7 cm/sec) used in the proposed work on the BIN diode tripler [2,3] is overly optimistic. No simulation work has been published for the spatial velocity overshoot in GaAs semiconductors. Based upon the above studies and the high electric field distribution of the GaAs BIN diode structure as will be discussed later in this paper, the average drift velocity in the GaAs BIN diode should be very close to the saturation drift velocity of the gallium arsenide material system, i.e., 6×10^6 cm/sec. This value will be used below to calculate the intrinsic cut-off frequency and series resistance of BIN diode frequency triplers. The calculated series resistance of $\approx 200\ \Omega$ has been shown to be more in agreement with the high-frequency impedance measurement results of this study.

Back-to-Back Diode Configuration

1. Capacitance-Voltage Characteristic

Due to the blocking barrier of the BIN structure, two diodes should be able to operate back-to-back generating a symmetrical capacitance-voltage curve. The sharp spike in the capacitance-voltage curve eliminates even harmonics and thus favors tripling operation [2,3]. In addition, the height and width of this capacitance-voltage curve can, in principle, be adjusted by doping control alone [2,3]. This arrangement needs no external ohmic contact, thereby making a highly efficient frequency tripler in which the efficiency does not degrade with high fundamental power. Only one metal layer is required which greatly simplifies the fabrication task [10,11]. In addition, no idler is needed in the circuit design, again, making the circuit construction much simpler [10,11]. This back-to-back configuration is considered to be a very important feature of the BIN structure. In this section, the back-to-back diode configuration will be studied and carefully discussed to illustrate the possibility of employing this concept in odd-harmonic frequency multiplication.

The C-V characteristics measured from both a single diode and from two-back-to-back connected GaAs BIN diodes are shown in Fig. 2. It can be seen from these results that the capacitance from two back-to-back connected (in series) BIN diodes can not be scaled directly from that of a single diode. Specifically, C_{max} of two back-to-back connected diodes is approximately half of that of a single diode as what one might expect. However, C_{min} of a single diode is only slightly higher than that of two back-to-back connected diodes. This is due to the symmetrical nature of the back-to-back BIN structure; when one diode is strongly reversed biased, the other diode will be strongly forward biased. Therefore, when one BIN diode is in the depletion mode, the other BIN diode is in the accumulation mode. In other words, when one diode has a capacitance value of C_{min}, the other diode has a capacitance of C_{max}. The total minimum capacitance of two back-to-back connected BIN diodes is, therefore, much higher than half of the minimum

capacitance of one single diode. The back-to-back diode configuration results in a much smaller ratio of C_{max}/C_{min} and smoother (i.e., lower gradient slope) C-V characteristic which, therefore, reduces the nonlinearity which is utilized to generate harmonics (see Fig. 2).

This can also be illustrated assuming a capacitance ratio, k ($k = C_{max}/C_{min}$), the total capacitance of a back-to-back BIN diode system when one BIN diode is under a large forward bias and the other BIN diode under a large reverse bias (i.e., when one diode is strongly forward biased, the other diode will be strongly reverse biased) is $kC_{min}/(k+1)$ as shown below:

$$C_{bb} = 1/(1/C_{max}+1/C_{min}) = 1/(1/(kC_{min})+1/C_{min}) = kC_{min}/(k+1) \approx C_{min}$$

where C_{bb} is the equivalent capacitance of two back-to-back (series) connected BIN diodes. This value is very close to C_{min} of one single diode, especially when the capacitance ratio, k, is large. Therefore, the GaAs BIN structure which has a capacitance ratio close to 4.5 in a single diode configuration, however, has a capacitance ratio of ≈ 2.3 for the back-to-back diode arrangement (as can be seen in Fig. 2).

2. Cut-Off Frequency

In the back-to-back diode configuration, when one diode is under forward bias, the other diode is always reverse biased, one may, therefore, question which series resistance should be used - the series resistance of one single diode or of two back-to-back diodes. It can be seen from Table. I that the operation of one single diode is very different from that of two back-to-back connected diodes. For example, when a single diode is strongly reverse biased, the epilayer is completely depleted, the capacitance is close to C_{min}, and the series resistance is close to zero. However, applying the same large reverse bias to the BIN diode in the back-to-back configuration will result in a much different situation. While the epilayer of one diode is completely depleted and provides the minimum capacitance, C_{min}, the other diode shows a series resistance of R_S due to the undepleted epilayer. The

back-to-back diode operation increases the effective series resistance one should use for calculating the cut-off frequency of two back-to-back connected diodes. To determine this effective series resistance, a series of high frequency impedance measurements were performed on one single diode, as well as on two back-to-back diodes. It should be mentioned that the high frequency impedance measurements were performed on approximately 25 devices per wafer. The capacitance of the diode can be deduced from the reactance values obtained from the high-frequency impedance measurements. The ratio of the RC time constant of a single diode to that of two back-to-back connected diodes can then be used to determine the effective series resistance for the back-to-back BIN diode configuration. The value of the effective series resistance is determined to be between $1.5R_S$ and $2R_S$.

Device Simulation Results

In this work, a computer program was developed to solve exactly the Poisson Equation in multilayer semiconductor devices having a step-wise doping profile [11]. The program developed in this paper allows for detailed simulation of the device and provides crucial physical insight into the key performance parameters. In this model, Poisson's equation is solved exactly by a set of coupled analytical expressions which accurately describe each region of the BIN diode. Band and carrier continuity between layers is included and properly accounted for. The final expressions derived are transcendental and require carefully structured algorithms to avoid inaccurate and unrealistic convergent difficulties. This method does not require large computer memory arrays and lengthy computer time as numerically intensive programs such as PISCES [11].

Using the device simulation model developed, the electric field of the BIN diode structure is studied in detail. The original structure proposed for the BIN diode tripler [2,3] has an aluminum metal gate in intimate contact with a layered GaAs structure consisting of a 300 Å thick undoped GaAs, a 100 Å thick $2x10^{18}$ cm^{-3} heavily doped n^+ layer, another

1500 Å thick undoped layer, and a thick heavily doped n^+ region grown on top of a semi-insulating GaAs substrate. The electric field distributions of this structure under different bias conditions are shown in Fig. 3. As can be seen from this result, the electric fields in both the barrier and epitaxial layers are fairly high. It should be pointed out that the high electric field strength in the epilayer results in low average drift velocity as discussed in the above section [13,14]. In addition, the electric field in the barrier region are very close to the breakdown field of GaAs and may actually cause the breakdown of the BIN diode structure. The results of the theoretical simulation model show good agreement with the experimental measurement of the BIN diode as shown in Fig. 2.

Summary

The intrinsic cut-off frequency of the original GaAs BIN diode is close to 50 GHz using the average drift velocity of 6×10^6 cm/sec. This result explains the low device-performance measurement from the GaAs BIN diode-grid frequency tripler arrays. The calculated series resistance also agrees well with the high-frequency impedance measurement results. Due to the large RC time constant and the reduced capacitance-voltage variation of the back-to-back BIN structure, the BIN diode frequency tripler employing a back-to-back configuration is not very efficient for high frequency generation.

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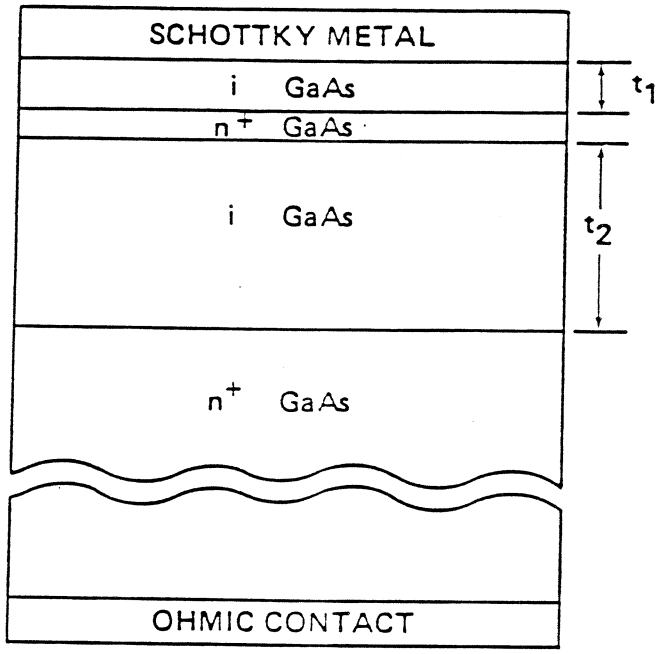

Fig. 1 The GaAs BIN diode structure.

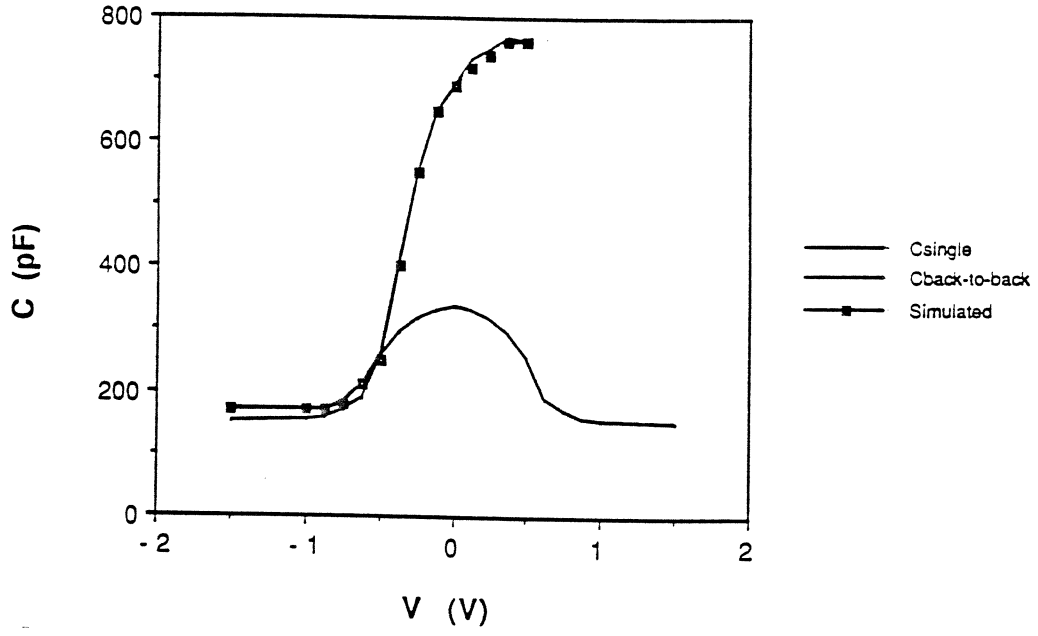

Fig. 2 The C-V characteristics measured from a single and two back-to-back connected GaAs BIN diodes.

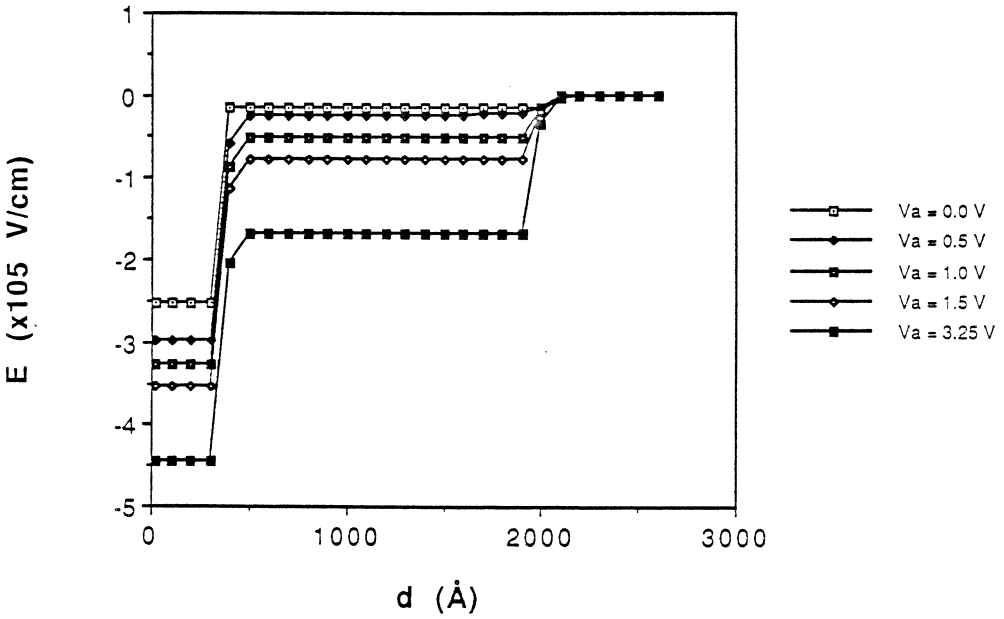

Fig. 3 The electric field distributions of the "original" GaAs BIN diode structure under different bias conditions.

Table 1.

	Large Forward Bias	Large Reverse Bias
Single BIN		
R	R_S	0
C	$C_{max,s}$	$C_{min,s}$
Back-to-Back BIN		
R	R_S	R_S
C	$C_{min,b}=C_{min,s}$	$C_{min,b}=C_{min,s}$