MORTEZA FAYAZI

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SUMMARY

Ph.D. candidate with a solid background in Electrical Engineering and Computer Science. My research aims toward solving fundamental multidisciplinary problems that span over EAD design, Machine Learning, Analog/Digital circuit design, high-level SoC design, computer architecture, Natural Language Processing, and software engineering.

RESEARCH INTERESTS

Circuit Design Automation
Analog Circuit Design
Open-source Circuit Design Tool
Machine Learning
Digital Circuit Design
SoC Design

EDUCATION

Ph.D. in Electrical Engineering and Computer Science 2017 - Present
University of Michigan, Ann Arbor, Michigan, US

M.S.E. in Electrical Engineering and Computer Science 2017 - 2020
University of Michigan, Ann Arbor, Michigan, US
GPA: 3.82/4

B.Sc. in Electrical Engineering; Major: Electronics, Minor: Computer Science 2012 - 2017
Sharif University of Technology, Tehran, Iran
GPA: 17.71/20 (3.88/4)

PUBLICATIONS (GOOGLE SCHOLAR)

FuNToM: Functional Modeling of RF Circuits Using a Neural Network Assisted Two-Port Analysis Method
Morteza Fayazi, Morteza Tavakoli Taba, Amirata Tabatabavakili, Ehsan Afshari, Ronald Dreslinski
International Conference on Computer-Aided Design (ICCAD), 2023. [PDF]

AnGeL: Fully Automated Analog Circuit Generator Using a Neural Network Assisted Semi-supervised Learning Approach
Morteza Fayazi, Morteza Tavakoli Taba, Ehsan Afshari, Ronald Dreslinski
IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications (TCAS-I), 2023. [PDF]

A Compact CMOS 363 GHz Autodyne FMCW Radar with 57 GHz Bandwidth for Dental Imaging
Morteza Tavakoli Taba, S. M. Hossein Naghavi, **Morteza Fayazi**, Ali Sadeghi, A. Cathelin, Ehsan Afshari
IEEE Custom Integrated Circuits Conference (CICC), 2023. [PDF]

A 390 GHz CMOS FMCW Radar For Dental Imaging: Theory and Implementation
Morteza Tavakoli Taba, S. M. Hossein Naghavi, **Morteza Fayazi**, Ali Sadeghi, Mohammed Aseeri, Ronald Dreslinski, Andreia Cathelin, Ehsan Afshari
To be submitted to IEEE Journal of Solid-State Circuits (JSSC), 2023.

A 507 GMACs/J 256-Core Domain Adaptive Systolic-Array-Processor for Wireless Communication and Linear-Algebra Kernels in 12nm FINFET
Kuan-Yu Chen, Chi-Sheng Yang, Yu-Hsiu Sun, Chien-Wei Tseng, **Morteza Fayazi**, Xin He, Siying Feng, Yufan Yue, Trevor Mudge, Ronald Dreslinski, Hun-Seok Kim, David Blaauw
IEEE Symposium on VLSI Technology and Circuits, 2022. [PDF]

FASCINET: A Fully Automated Single-Board Computer Generator Using Neural Networks
Morteza Fayazi, Z. Colter, Z. Benameur-El Youbi, J. Bagherzadeh, Tutu Ajayi, Ronald Dreslinski
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2022. [PDF]

Versa: A 36-Core Systolic Multiprocessor With Dynamically Reconfigurable Interconnect and Memory
Sung Kim, **Morteza Fayazi**, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor Mudge, Chaitali Chakrabarti, David Blaauw, Ronald Dreslinski, Hun-Seok Kim
IEEE Journal of Solid-State Circuits (JSSC), 2022. [PDF]

Tablext: A Combined Neural Network And Heuristic Based Table Extractor
Zachary Colter, **Morteza Fayazi**, Zineb Benameur-El, Serafina Kamp, Shuyan Yu, Ronald Dreslinski
Elsevier Array, 2022. [PDF]

Open Information Extraction: A Review of Baseline Techniques, Approaches, and Applications
Serafina Kamp*, **Morteza Fayazi***, Z. Benameur-El, S. Yu, Z. Colter, R. Dreslinski (*Equal contribution)
Submitted to Expert Systems With Applications, 2022.

Applications of Artificial Intelligence on the Modeling and Optimization for Analog and Mixed-Signal Circuits: A Review
Morteza Fayazi, Zachary Colter, Ehsan Afshari, Ronald Dreslinski
IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications (TCAS-I), 2021. [PDF]

Versa: A Dataflow-Centric Multiprocessor with 36 Systolic ARM Cortex-M4F Cores and a Reconfigurable Crossbar-Memory Hierarchy in 28nm
Sung Kim, **Morteza Fayazi**, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor Mudge, Chaitali Chakrabarti, David Blaauw, Ronald Dreslinski, Hun-Seok Kim
IEEE Symposium on VLSI Circuits, 2021. [PDF]

Fully-Autonomous SoC Synthesis using Customizable Cell-Based Analog and Mixed-signal Circuits Generation
T. Ajayi, S. Kamineni, **Morteza Fayazi**, Y. Cherivirala, K. Kwon, S. Gupta, W. Duan, J. Lee, C. Chen, M. Saligane, Dennis Sylvester, David Blaauw, Ronald Dreslinski, Benton Calhoun, David Wentzloff
IFIP/IEEE International Conference on Very Large Scale Integration-System on a Chip, 2021. [PDF]

An Open-source Framework for Autonomous SoC Design with Analog Block Generation
T. Ajayi, S. Kamineni, Y. Cherivirala, **Morteza Fayazi**, Kyumin Kwon, Mehdi Saligane, Shourya Gupta, Chien-Hen Chen, Dennis Sylvester, David Blaauw, Ronald Dreslinski, Benton Calhoun, David Wentzloff
28th International Conference on Very Large Scale Integration (VLSI-SoC), 2020. [PDF]

Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits
Ronald Dreslinski, David Wentzloff, **Morteza Fayazi**, Kyumin Kwon, David Blaauw, Dennis Sylvester, Benton Calhoun, Matteo Coltella, David Urquhart
GOMACTech Conference, 2019. [PDF]

A Simplified Approach to Two-Port Analysis in Feedback
Morteza Fayazi, Ali Fotowat, Zahra Kavehvash
To be submitted to IEEE Transaction on Education, 2015. [PDF]

POSTERS

FuNToM: Functional Modeling of RF Circuits Using a Neural Network Assisted Two-Port Analysis Method
Morteza Fayazi, Morteza Tavakoli Taba, Amirata Tabatabavakili, Ehsan Afshari, Ronald Dreslinski
Work-in-Progress at Design Automation Conference (DAC), 2023.

FASCINET: A Fully Automated Single-Board Computer Generator Using Neural Networks
Morteza Fayazi, Z. Colter, Z. Benameur-El Youbi, J. Bagherzadeh, Tutu Ajayi, Ronald Dreslinski
Work-in-Progress at Design Automation Conference (DAC), 2021.

Fully Autonomous Mixed Signal SoC Design & Layout Generation Platform
T. Ajayi, Y. Cherivirala, K. Kwon, Sumanth Kamineni, Mehdi Saligane, **Morteza Fayazi**, Shourya Gupta, Chien-Hen Chen, Dennis Sylvester, David Blaauw, Ronald Dreslinski, Benton Calhoun, David Wentzloff
IEEE Hot Chips 32 Symposium (HCS), 2020. [PDF]

RESEARCH EXPERIENCE

Functional Estimator of RF Circuits Tool 2022
- Research under the supervision of Prof. Dreslinski and Prof. Afshari, University of Michigan
- Using NNs and two-port analysis method for modeling multiple topologies using a single main dataset and multiple small datasets
- Working closely with an analog design team to add analog circuit design intuition into ML applications

Fully Automated Analog Circuit Generator Tool 2022
- Research under the supervision of Prof. Dreslinski and Prof. Afshari, University of Michigan
- Using NNs to determine the behavior of complicated topologies by combining the more simple ones and presenting a database including labeled and unlabeled data
- Using this database, we propose a tool that performs all the schematic circuit design steps from deciding the circuit topology to determining the circuit parameters

Automated Infection Control for Indoor Spaces 2021
- Internship under the supervision of Dr. Mohammad Noshad, Shyld AI
- Using image processing to detect humans and track their motions

Autonomous Single-Board Computer Generator 2020
- Research under the supervision of Prof. Ronald Dreslinski, University of Michigan
- Using NNs to design customized peripheral circuits for single-board computers given their main components
- Creating a large COTS DB of existing discrete IPs, efficiently searching through them, and selecting optimal IP options based on the user requirements

A Comprehensive Study of Applications of AI on Designing Analog Circuits 2020
- Research under the supervision of Prof. Ronald Dreslinski, University of Michigan
- Explaining the basic concepts of AI and surveying some recent studies of various AI techniques for analog circuit design
- Discussing the main approaches as well as the pros and cons of each method
- Giving meaningful insights about the current challenges and open issues, as well as recommending approaches for specific applications

Fully-Autonomous SoC Synthesis using Cell-Based Synthesizable Analog Circuits 2018
- Joint project under the supervision of Prof. Ronald Dreslinski, Prof. Blaauw, Prof. Sylvester, and Prof. Wentzloff (University of Michigan), Prof. Calhoun (University of Virginia), and ARM plc [GitHub]
- Funded by Air Force Research Laboratory (AFRL) and Defense Advanced Research Projects Agency (DARPA)

- Leveraging a differentiating technology to automatically synthesize "correct-by-construction" Verilog descriptions for both analog and digital circuits
- Presenting the world's first autonomous mixed-signal SoC framework, driven entirely by user constraints, along with a suite of automated generators for analog blocks
- Creating a large COTS DB of existing discrete IPs, efficiently searching through them, and selecting optimal IP options based on the user requirements
- Working closely with seven graduate students and integrating all works into one software platform

Automated Datasheet Scrubber 2018

- Research under the supervision of Prof. Ronald Dreslinski, University of Michigan [GitHub]
- Using ML, image processing, and text processing for realizing datasheets category and extracting relevant data within either text or table
- Discussing the main approaches as well as the pros and cons of each method
- Supervising two graduate and four undergraduate students

TEACHING EXPERIENCE

Certificate of Completion in Preparing Future Faculty *University of Michigan* 2023

Graduate Student Instructor of *"Introduction to Electronic Circuits" University of Michigan EECS 215* 2023, Instructor: Prof. Terry

Graduate Student Instructor of *"Analog Circuits" University of Michigan EECS 311* 2021
Instructor: Prof. Flynn

Graduate Student Instructor of *"Analog Circuits" University of Michigan EECS 311* 2018
Instructor: Prof. Peterson

Teaching Assistant of *"Principles of Electrical Engineering" Sharif University of Technology* 2016, 2015
Instructor: Prof. Fardmanesh

Teaching Assistant of *"Principles of Electronics" Sharif University of Technology* 2016, 2015
Instructor: Prof. Kavehvash

Teaching Assistant of *"Analog Circuits" Sharif University of Technology* 2014
Instructor: Prof. Khorasani

ACTIVITIES

- Machine Learning Engineering Intern at Shyld AI 2021
- Member of Ultra high-speed Nonlinear Integrated Circuit lab, University of Michigan 2020 - Present
- Member of Circuit and Architecture Design Research group, University of Michigan 2018 - Present

HONORS & AWARDS

- Awarded University of Michigan Rackham Graduate Student Research Grant 2023
- Outstanding undergraduate thesis award from Electrical Engineering department at Sharif University of Technology 2017
- Ranked 2^{nd} in Electronics Major among all 2012 EE entrants 2017
- Awarded University of San Diego graduate fellowship, for Ph.D. studies 2017
- Awarded University of Waterloo graduate fellowship, for M.A.Sc program 2017
- Membership of Exceptional Talents Community of Sharif University of Technology 2014-2017
- Ranked 33^{th} in the National University Entrance Examination among 60,000+ participants, Iran 2012

SELECTED COURSE PROJECTS

Designing and implementation of two ways superscalar MIPS R10K microarchitecture based out of order processor for Alpha 64 ISA
"Computer Architecture" University of Michigan EECS 470, Instructor: Prof. Dreslinski 2019

Designing and implementation of binary content addressable memory capable of in-memory compute and low power mode
"VLSI Design I" University of Michigan EECS 427, Instructor: Prof. Sylvester 2018

Designing and implementation of a CMOS wide-bandwidth transimpedance amplifier (TIA) for an optical fiber cable of operating at 5 Gbps
"Monolithic Amplifier Circuits" University of Michigan EECS 413, Instructor: Prof. Afshari 2018

Design and implementation of third order continuous time $\Delta\Sigma$ ADC with chopping and FIR feedback
"Analog to Digital Interfaces" University of Michigan EECS 511, Instructor: Prof. Flynn 2018

SELECTED COURSES FOR ELECTRICAL ENGINEERING

- **VLSI Design I** (University of Michigan EECS 427), Prof. Sylvester 2018
- **Monolith Amplifier Circuits** (University of Michigan EECS 427), Prof. Afshari 2018
- **Analog to Digital Interfaces** (University of Michigan EECS 511), Prof. Flynn 2018
- **Analog Integrated Circuits** (University of Michigan EECS 522), Prof. Wentzloff 2018
- **Power Electronics** (University of Michigan EECS 418), Prof. Avestruz 2017
- **Filter Design & Network Synthesis** (Sharif University of Technology), Prof. Sadughi 2016
- **Pulse Technique & Digital Circuits** (Sharif University of Technology), Prof. Bagheri 2015

SELECTED COURSES FOR COMPUTER SCIENCE & ENGINEERING

- **Computer Architecture** (University of Michigan EECS 470), Prof. Dreslinski 2019
- **Convex Optimization** (University of Michigan IOE 611), Prof. Epelman 2017
- **Compiler I** (Sharif University of Technology), Prof. Foroughmand-Araabi 2016
- **Automata and Language Theory** (Sharif University of Technology), Prof. Khazaei 2015
- **Linear Algebra** (Sharif University of Technology), Prof. Bahraini 2015
- **Mathematical Analysis I** (Sharif University of Technology), Prof. Bahraini 2014
- **Graph Theory and Applications** (Sharif University of Technology), Prof. Qajar 2014

MENTORSHIP & LEADERSHIP

- Mentoring two Masters and four undergraduate students, for the [FASoC project] 2018 - 2021
- Founding and leading a new student organization, Islamic Society of Ahlulbayt (ISA), on the North Campus at the University of Michigan 2018 - 2020
- Mentoring multiple undergraduate students as part of the Michigan's Lunch and Lab Mentorship Program 2017 - 2020

SKILLS & TOOLS

- **Programming Language:** Python, C, MATLAB, Ruby
- **Hardware Description Language:** Verilog
- **Scripts:** Makefile, BASH
- **HW/SW Debug tools:** Oscilloscope, Synopsys Verilog Compiler Simulator (VCS)
- **Analog Design Tool:** Virtuoso Cadence, Orcad PSpice and Schematic, HSpice, Advanced Design System (ADS)
- **Digital Design Tool:** Proteus, Quartus, Synopsys Design Compiler
- **PCB Design:** Altium Designer
- **SoC Design:** ARM Socrates