Source / drain contacts in organic polymer thin film transistors

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ABSTRACT

Organic polymer based thin-film transistors (OP-TFTs) look very promising for flexible organic electronics. In this paper, we describe devices based on a gate-planarized structure and using spin-coated organic polymer. We have analyzed the role of the device source and drain contacts and we present data indicating Schottky behavior of the contacts in OP-TFTs. In addition, we describe a quantitative evaluation of the source drain series resistances and extract the OP-TFT intrinsic electrical parameters.

1. INTRODUCTION

Organic semiconductors can be divided into three main groups: small molecules, oligomers and polymers [1]. In general, oligomers deposited by evaporation in vacuum have a highly ordered molecular structure while most of the time, organic polymers are deposited by spin coating or inkjet printing over large areas at low temperature [2]. Organic polymer thin-film transistors usually show lower electrical performances than oligomer-based devices [1] but have a considerable potential in large-area low-cost flexible electronics. Although, so far, the electrical performances of most organic polymer thin-film transistors (OP-TFTs) are often limited by the polymer low conductivity, the source and drain contacts play a predominant role in the device operation.

2. DEVICE FABRICATION

So far, many research groups have often used test structures, in which no patterning of organic and inorganic (especially gate electrode and insulator) layers is involved. We have fabricated and characterized gate planarized organic polymer thin-film transistor based on the structure shown in Figure 1 [3]. The organic semiconductor used here is solution-based F8T2 (poly-9,9-dioctylfluorene-co-bithiophene) [4,5,6]. The OP-TFTs use benzocyclobutene (BCB) as gate planarization material, amorphous silicon nitride as gate insulator and ITO as source and drain electrodes. Our typical TFT channel width and length are 50-100 and 6-100 μm, respectively.

3. RESULTS AND ANALYSIS

In this study, the OP-TFT source is always grounded, as shown in Figure 1.
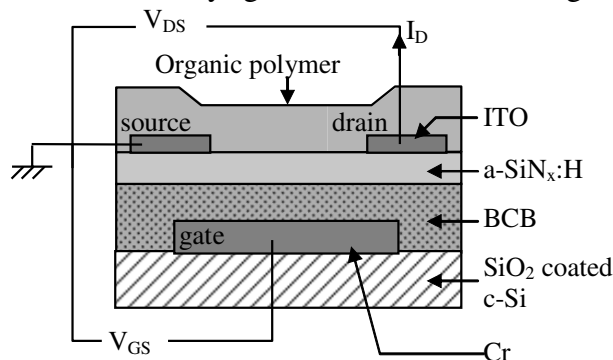

Figure 1: Cross section of our gate planarized OP-TFT structure.

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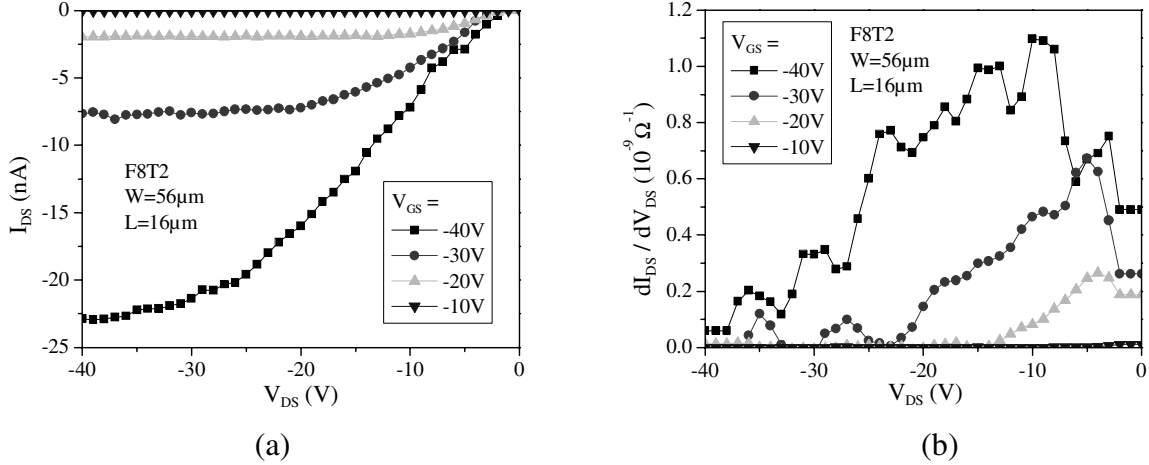
(a)

(b)

Figure 2: (a) Typical output characteristics for F8T2 based OP-TFT. (b) Derivatives of the curves in (a).

Typical OP-TFT output (drain current versus drain voltage, I_{DS}-V_{DS}) characteristics and their derivatives are plotted in Figure 2(a) and (b), respectively. Although the exact theory of OP-TFT operation is still under investigation, the MOSFET theory as modified for amorphous semiconductor based TFTs provides a good description of the device behavior. Consequently, the TFT field-effect mobility and threshold voltage in linear regime at low source-drain voltage were extracted from the following equation:

$$I_{DS} = -\mu_{FE\,lin} C_{ins} \frac{W}{L} (V_{GS} - V_{T\,lin}) V_{DS} \qquad (1)$$

In saturation regime, we used:

$$I_{DS} = -\mu_{FE\,sat} C_{ins} \frac{W}{2L} (V_{GS} - V_{T\,sat})^2 \qquad (2)$$

The OP-TFT subthreshold swing S was extracted from [7]

$$I_{DS} \propto 10^{-V_{GS}/S} \qquad (3)$$

The electrical parameters obtained for each device are summarized in Table 1. We should note that, as we have observed in most cases, the field-effect mobility extracted in saturation regime is slightly higher than the field-effect mobility extracted in linear regime.

Although the electrical performances of many organic thin-film transistors are often limited by the low conductivity of the organic semiconductor, the source and drain contacts play a predominant role in the device operation and it has clearly been found that they could have a critical effect on the device performances. In conventional inorganic TFT or MOSFETs, the S/D electrodes form ohmic contacts to a highly doped semiconductor layer. In OP-TFTs, carrier injection studies [8,9] have shown non-ohmic behavior S/D contacts: it is now believed that S/D contacts in OP-TFTs form Schottky barriers to the channel region. Indeed, in Figure 3(a), we have plotted the OP-TFT drain current versus drain voltage curves measured when the device gate is floating (gate electrode not connected), which suggests Schottky S/D contacts. In Figure 3(b), we show that the drain current of the OP-TFT in accumulation follows a power law dependence with the source-drain voltage, with an exponent β always higher than 1. For the devices measured here, the exponent β ranged between 1.2 and 2.1. These plots clearly suggest that the S/D electrodes in these OP-TFTs do not form perfectly ohmic contacts, but create Schottky barriers. The carriers can tunnel through the Schottky barriers when negative voltages are applied on the device gate and drain so that the barrier becomes narrow enough.
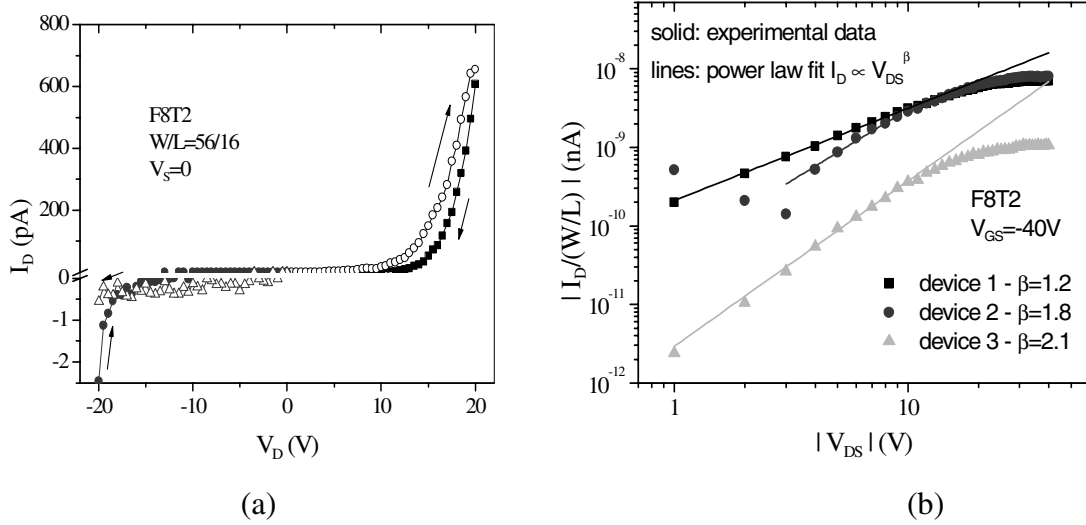
(a)

(b)

Figure 3: (a) Drain current versus drain voltage characteristics measured with the device gate floating. (b) Curves measured for different OP-TFTs in accumulation regime

The quantitative role of the source/drain (S/D) contacts can be investigated using a method developed for amorphous semiconductor thin-film transistors: the Transmission Line Method (TLM) [10,11,12]. This method models the S/D contacts and access regions by gate voltage dependent series resistances ($R_{S/D}=R_S+R_D$), as illustrated in Figure 4. In our OP-TFTs, these source/drain resistances can also be dependent on the S/D voltage. The TLM analysis is done when the TFT is in linear regime, for low values of the S/D voltage.

Based on the model shown in Figure 4, the equation describing the OP-TFT operation in linear regime at low V_{DS} becomes:

$$I_D = -\mu_{FE\,int} C_i \frac{W}{L}\left(V_{GS} - V_{T\,int}\right)\left(V_{DS} + R_{S/D}I_D\right) \tag{4}$$

where $\mu_{FE\,int}$ and $V_{T\,int}$ are the intrinsic field-effect mobility and threshold voltage, i.e. representative of the conduction channel, or ideal TFT only. In most O-TFTs, we expect significant parasitic S/D series resistances resulting from the S/D contacts resistances. In addition, we can also expect significant contributions of the resistances of the access regions between the S/D contacts and the conduction channel (access resistance) in staggered OP-TFT structures [10]. In the OP-TFTs studied here, we expect the conduction channel to be created in the same plane as the source and drain electrode, which should reduce drastically the access resistances. However, significant contact resistances can nevertheless degrade the OP-TFT performances, especially in linear regime, i.e. at low V_{DS}. To characterize the S/D series resistances using the Transmission Line Method (TLM), we measure a series of OP-TFTs with identical S/D contact characteristics and different channel lengths. The devices ON resistances (R_{ON}) are plotted as a function of the channel length, as shown in Figure 5(a). Based on equation (4), we can write:

$$WR_{ON} = \frac{V_{DS}}{I_{DS}} = WR_{S/D} + WR_{channel} \tag{5}$$

with
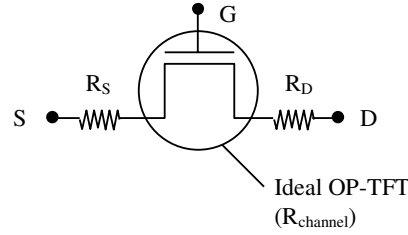$$R_{channel} = \frac{1}{\mu_{FE\,int} C_i W\left(V_{GS} - V_{T\,int}\right)} \times L \tag{6}$$

Figure 4: Equivalent model of the OP-TFT using gate voltage-dependent S/D series resistances.
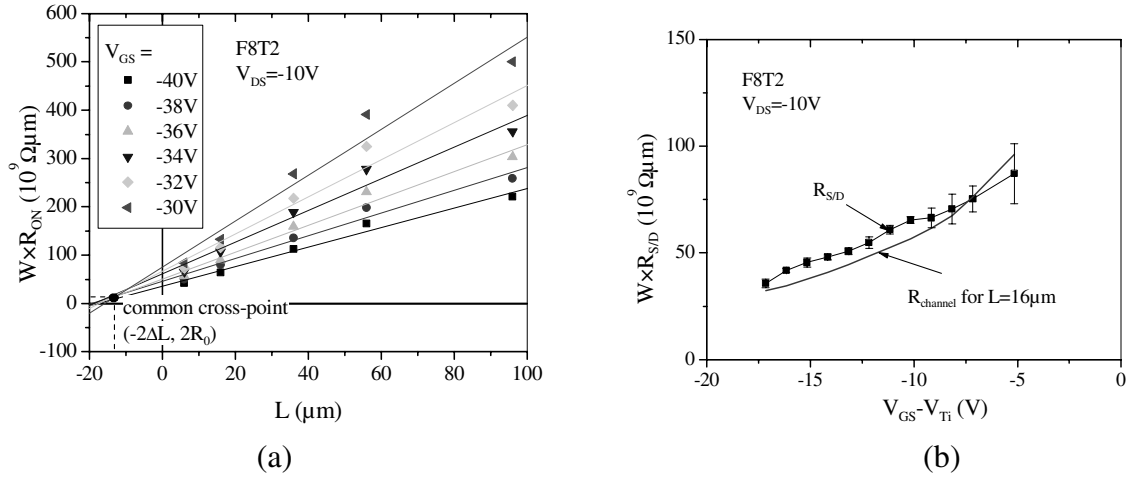

(a)

(b)

Figure 5: (a) Total ON-resistance measured on a series of OP-TFTs. (b) Variations of the OP-TFT S/D series resistances and conduction channel resistance with the applied voltage.
The total S/D series resistance $R_{S/D}$ can therefore be extracted for each gate voltage from the y-intercept of the curves and the conduction channel resistance is calculated from the slope of the curves. Figure 5(b) shows the evolution of the S/D series resistances and the corresponding values of the conduction channel resistance, for a channel length of L=16µm, extracted from the curves in Figure 5(a). We obtained values of the S/D series resistances around $5 \times 10^8 \Omega$ for V_{GT} around -10V. We can see that the channel and S/D resistances are of comparable values, clearly indicating the significant effect of the S/D contacts on the overall device electrical performances. In addition, we can calculate the device intrinsic field-effect mobility ($\mu_{FE\ int}$) and threshold voltage ($V_{T\ int}$) from the variations of the $R_{channel}$ with V_{GS}, as illustrated in Figure 6:

$$\frac{L}{W \times R_{channel}} = \mu_{FE\ int} C_i \left(V_{GS} - V_{T\ int} \right) \tag{7}$$

Equation (7) allows for the calculation of $\mu_{FE\ int}$ and $V_{T\ int}$ from the slope and x-intercept of the linear fit of the experimental data. The data shown in Figure 6 yields $\mu_{FE\ int} = 3.8 \times 10^{-3} \text{cm}^2/\text{Vs}$ and $V_{T\ int} = -23V$. As expected, the device apparent field-effect mobility is lower than the intrinsic field-effect mobility. This effect will be more significant for short-channel devices, since the channel resistance decreases with decreasing channel length while the S/D series resistances are channel length-independent. This is clear on Figure 7 where we have plotted the apparent field-effect mobility as a function of the device channel length.
The effect of the S/D series resistances can also be partially represented as an increase of the apparent channel: the total O-TFT ON-resistance is [10]

$$R_{ON} = 2R_{S/D} + \frac{L}{\mu_{FE\,i} C_i W (V_{GS} - V_{Ti})} = 2R_0 + \frac{L + 2\Delta L}{\mu_{FE\,i} C_i W (V_{GS} - V_{Ti})} \tag{8}$$

where ΔL and R_0 are independent of the gate voltage. ΔL and R_0 are extracted from the R_{ON} versus L curves: all the R_{ON} - L curves have a common cross-point located slightly away from the y-axis [10,13,14], whose coordinates are ($x = -2\Delta L, y = 2R_0$). This is quite clear in Figure 5(a), although the extraction of ΔL and R_0 may be affected by a significant uncertainty. ΔL is associated with the effective channel length, which is longer than the mask specified channel length, i.e. the current path extends beyond the source/drain contact edges. It has been shown to depend significantly on the source and drain contact resistances and R_0 represents the limit of the source and drain series resistance $R_{S/D}$ for a very high gate voltage [10]. Typical values of ΔL and R_0 obtained on our devices are summarized in Table 1.

Table 1: Typical electrical performances of our OP-TFTs.

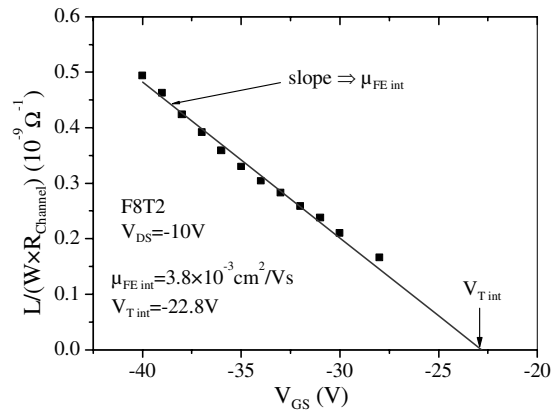|	
W/L	56/16
C_i (F/cm^2)	7.5×10^{-9}
$\mu_{FE\,lin}$ (cm^2/Vs)	2.3×10^{-3}
$\mu_{FE\,int}$ (cm^2/Vs)	3.8×10^{-3}
$R_{S/D}$ at V_G-V_{Ti}=-10V (Ω)	1.2×10^9
$R_{channel}$ at V_G-V_{Ti}=-10V (Ω)	1.0×10^9
ΔL (μm)	5-8μm
R_0 (Ω)	7×10^7-3×10^8
$V_{T\,lin}$ (V)	-21
$V_{T\,lin\,norm}$ (C/cm^2)	-2×10^{-7}
$\mu_{FE\,sat}$ (cm^2/Vs)	3.5×10^{-3}
$V_{T\,sat}$ (V)	-17
$V_{T\,sat\,norm}$ (C/cm^2)	-1.2×10^{-7}
S (V/dec)	1.5
$N_{ss}^{max} = \left(\dfrac{S \log(e)}{kT/q} - 1 \right) \dfrac{C_i}{q}$ (cm^{-2}eV^{-1})	1.2×10^{12}
ON/OFF ratio (in linear regime)	10^5

Figure 6: Curves used for the extraction of the OP-TFT intrinsic field-effect mobility and threshold voltage values.
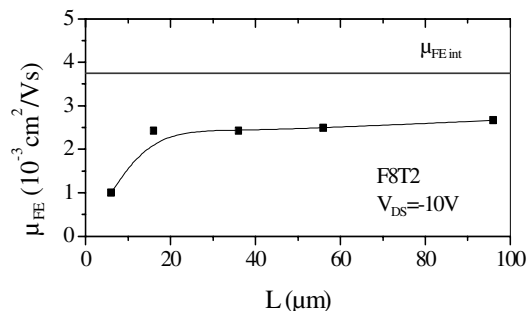
Figure 7: Apparent field effect mobility as a function of the device channel length. Constant line shows the intrinsic field-effect mobility value extracted from Figure 6.

4. CONCLUSION

We have presented OP-TFTs based on spin-coated organic polymer with field-effect mobility around $5\times10^{-3}cm^2/Vs$, ON-OFF current ratio up to 10^5 and subthreshold slope down to 1.5V/dec A detailed analysis of the devices electrical performances was presented, including a characterization of the OP-TFT source and drain contact electrical behavior suggesting the presence of Schottky barriers at the S/D electrodes. We also described a method to evaluate the device S/D series resistances and intrinsic electrical parameters.

ACKNOWLEDGEMENTS

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