Jpn. J. Appl. Phys. Vol. 42 (2003) pp. L 907–L 909
Part 2, No. 8A, 1 August 2003
©2003 The Japan Society of Applied Physics

Contact Resistance in Schottky Contact Gated-Four-Probe a-Si Thin-Film Transistor

Reiji HATTORI* and Jerzy KANICKI

Solid-State Electronics Laboratory, The University of Michigan, Ann Arbor, MI 48109-2108, U.S.A.

(Received May 6, 2003; accepted for publication June 11, 2003)

The source and drain electrode contact resistance of the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) with a Schottky-barrier source/drain contact was measured using a gated-four-probe TFT structure. Typically its variation with the gate bias is considered to be independent of the gate bias but we observed that contact resistances decrease exponentially with increasing gate bias. Our experimental data are explained by a combination of the tunneling current through the Schottky barrier and the access source/drain contact TFT resistance. [DOI: 10.1143/JJAP.42.L907]

KEYWORDS: contact resistance, Schottky-barrier, gated-four-probe, amorphous silicon, thin film transistor, five-terminal TFT structure

The gated-four-probe (GFP) technique is powerful for measuring an intrinsic performance of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs).[1] A five-terminal (FT) TFT structure has two additional narrow electrodes between source and drain electrodes. These electrodes allow us to measure the real voltage drop across a channel without any influence of source/drain contact resistances.[2,3] Therefore the intrinsic field-effect mobility and real threshold voltage can be accurately determined using this type of TFT structure.

Using the FT-TFT structure, we can measure accurately source/drain series resistances, since the voltage drop at both contacts can be measured. Their gate-bias dependence can also be determined. Typically source/drain contact resistances are considered (i) to be constant (ii) to be gate-bias independent, and (iii) to have the same value for both source and drain electrodes.

We will demonstrate in this paper that source/drain can be gate-voltage or drain-voltage dependent. This dependence can be associated with the tunneling current through the Schottky barrier (SB) and the access resistance present at source/drain contacts.

The cross-sectional view of the FT-TFT structure is shown in Fig. 1. In this paper, we used SB source/drain contacts, *e.g.*, the heavily doped a-Si:H layer was omitted at the metal/a-Si:H interface. As expected, the source/drain contact resistance in this structure is much larger than that in a conventional TFT. This type of TFT allows us a better understanding of the nature of source/drain contact resistances. The fabrication process of this structure has been described previously.[3] The TFT channel length was varied from 40 to 120 μm. The spacing between source (drain) and probe A (B) was kept constant at 10 μm for each FT-TFT structure. The measurements were carried out with an HP4156A semiconductor parameter analyzer at room temperature.

The intrinsic field-effect mobility (μ_{FE}) can be determined in the FT-TFT structure using:[2]

$$(X_B - X_A) = C_i \mu_{FE} W[V_G - V_T - (V_B + V_A)/2]/I_D, \quad (1)$$

where C_i is the geometrical capacitance of the gate insulator, V_G the applied gate voltage, V_T the threshold voltage, I_D the drain current, and V_A and V_B the potentials at X_A and X_A, respectively. Note that this equation is valid only for $(V_B - V_A) \ll V_G$. Because the source/drain series TFT resistance is high in our device, we use $V_D = 5$ V. Even under this condition, we can still use eq. (1) if the value of $V_B - V_A$ is small. In our case, we have confirmed that this value is less than 0.1 V. The field-effect mobility of 0.2 cm^2/V·s was obtained for all GFP TFT structures without any degradation for short-channel devices.

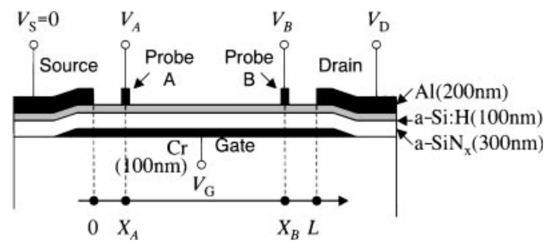

Fig. 1. Structure of gated-four-probe Schottky contact a-Si TFT.

Figure 2 shows a typical output characteristic of the Schottky contact (SC) a-Si:H TFT. This characteristic is different from the one typically observed for a conventional a-Si:H TFT. First the drain current increases with increasing drain voltage and saturates in the voltage region below 5 V. Then the drain current increases again and saturates above 15 V. Similar characteristics have been obtained for TFTs with different channel-lengths. The I_D saturated value in our devices is much smaller than that in a conventional TFT.[1)]

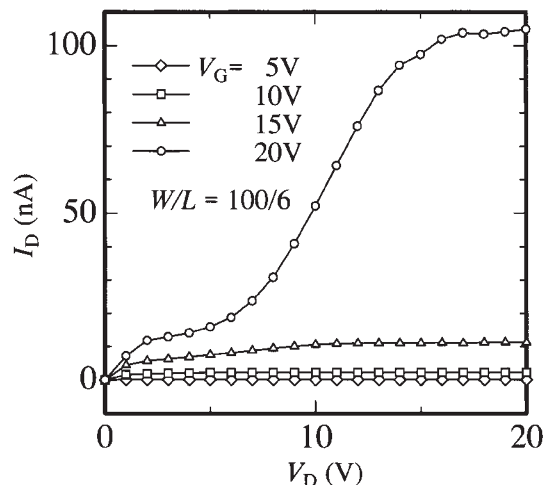

Fig. 2. Typical output characteristic as in text of the Schottky contact TFT.

*Current address: VLSI Design and Education Center, The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan.

This degradation in I_D is due to large source/drain contact series resistances. We should note that a constant source/drain series resistance cannot explain our experimental data. If the series resistance is constantly, the high drain current should show a simple saturation behavior at a very small value.

Using the GFP TFT structure, we can evaluate correctly the a-Si:H TFT series resistance. The advantage of this GPF method in comparison with the conventional transverse line (TL) method is that it can evaluate the series resistances at both the source (R_S) and drain (R_D) contacts, and their dependence on gate voltage. To evaluate R_S and R_D, we can use

$$R_S = \left(\frac{V_B X_A - V_A X_B}{X_A - X_B}\right)\frac{1}{I_D}, \quad (2)$$

$$R_D = \left[V_D - \frac{L(V_A - V_B) + V_B X_A - V_A X_B}{X_A - X_B}\right]\frac{1}{I_D}, \quad (3)$$

where we assume a constant electric field along the a-Si:H TFT channel. Thus the potential varies linearly between source and drain contacts. This assumption is correct for $(V_B - V_A) \ll V_G$.

Figure 3 shows the variations of R_S and R_D with the TFT channel length. Both of the applied drain and gate voltages are 20 V. This figure shows that, as expected the source and drain contact resistance is TFT channel-length independent at the same time. R_S is larger, by about one order of magnitude, than R_D because of the SB formation at the Al/a-Si interface. The SB at the source and drain contacts is reversed and forward biased, respectively.

Figure 4 shows the gate-bias dependences of R_S and R_D. It is apparent from this figure that R_S and R_D decrease exponentially by more than three orders of magnitude with increasing V_G. Only gate voltages above V_T were measured, because V_A and V_B are not related to the current flow below V_T. Also because electrons flow is induced by the reverse gate bias of the SB at the source contact, R_S should be larger than R_D except in the gate bias region near V_T. This exponential behavior can be explained by the tunneling current through the SB at the source contact. The voltage

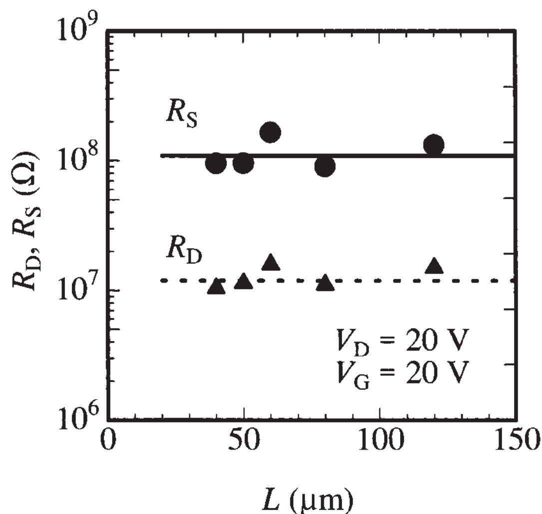

Fig. 3. Variations of the Schottky contact TFT R_S and R_D with the channel length.

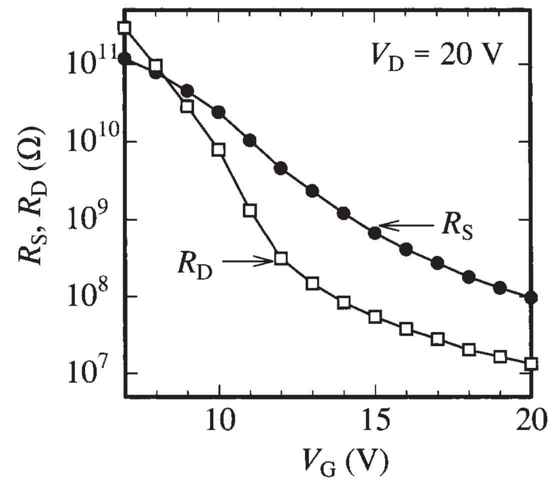

Fig. 4. Variations of R_S and R_D with the gate bias for the Schottky contact FT-TFT.

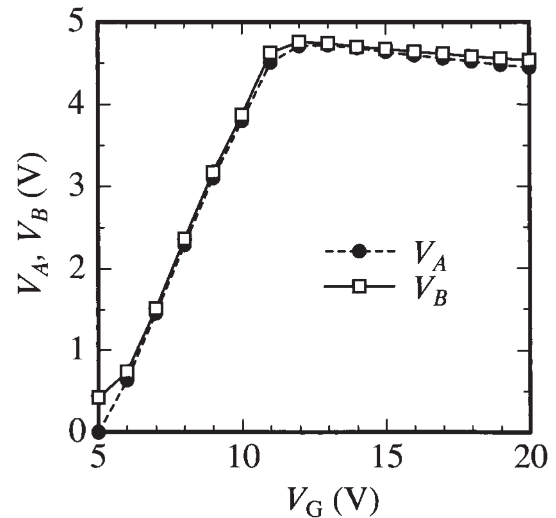

Fig. 5. Variations of the Schottky contact TFT V_A and V_B with the gate bias.

applied at the source electrode, which is almost equal to V_A, increases with increasing V_G as shown in Fig. 5. Therefore the tunneling current induced by V_G increases, and R_S decreases exponentially with V_G. However the increase in V_A saturates at $V_G > 12$ V and V_A even decreases slightly at larger V_G; although in this gate bias region, R_S decreases exponentially with V_G. This behavior can be explained by the SB modulation induced by gate voltage shown in Fig. 6, which shows the potential distributions of the on and off states schematically in the TFT channel where the deep channel region is neglected. The field induced by gate voltage is vertically crossing the field composed of SB in a conventional TFT structure. When the gate voltage V_G is applied (on state), the vertical field $E = -\partial\phi/\partial x$ to the gate is enhanced and $\partial^2\phi/\partial x^2$ must have a positive value to satisfy the continuity of the electric field near the gate insulator. According to Poisson's equation $\partial^2\phi/\partial x^2 + \partial^2\phi/\partial y^2 = \rho/\varepsilon$, the value of $\partial^2\phi/\partial y^2$ becomes negative on the contrary and the field along the y-direction near the source is enhanced. As a result, SB narrowing occurs by applying the gate voltage and tunneling current flows from

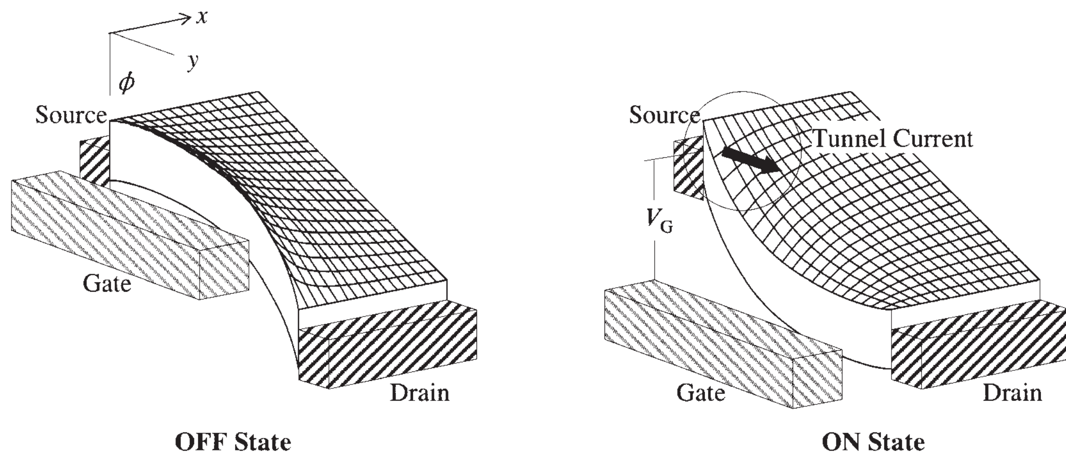

Fig. 6. The explanation of SB narrowing by gate voltage.

the source electrode to the channel, leading to a reduction R_S. This SB behavior is in agreement with the TFT two-dimensional simulation result published previously.[4)]

On the other hand, the SB at the drain contact is forward biased. In this case the current flow is mainly due to the forward current of the SC, and the contact resistance can be defined from the SB current equation: $I \cong I_0 \exp(nqV/kT)$. Apparently R_D will decrease with increasing SB forward bias at the drain electrode.

The source/drain electrode access resistance can also explain the exponential behavior of the TFT series resistance.[5)] However in our case, the source/drain contact resistances are much larger than the access resistance (the access resistance is in the order of $10^5\ \Omega$, while R_S is in the order of at least $10^7\ \Omega$), and the TFT access resistance can be neglected in our devices.

In summary, we have described the behaviors of the source/drain contact resistances in the SC FT-TFT structure. We have shown that both R_S and R_D decrease exponentially with increasing gate bias. This decrease can be associated with the tunneling current through the SB at source/drain a-Si:H contacts.

This work was carried out in the University of Michigan and was supported by the Center for Display Technology and Manufacturing and JSPS postdoctoral fellowship for research abroad.

1) C. S. Chiang and J. Kanicki: IEEE Electron Device Lett. **18** (1997) 340.
2) C. S. Chiang, C. Y. Chen, J. Kanicki and K. Takechi: App. Phys. Lett. **72** (1998) 2874.
3) C. S. Chiang, C. Y. Chen and J. Kanicki: IEEE Electron Device Lett. **19** (1998) 382.
4) R. Hattori and J. Shirafuji: Jpn. J. Appl. Phys. **33** (1994) 612.
5) S. Martine, A. Rolland, S. Mottet, N. Szydlo and H. Lebrun: Thin Solid Films **296** (1997) 129.