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4.2 Organic Polymer Field Effect Transistors

Jerzy Kanicki and Sandrine Martin

4.2.1 Introduction

Conjugated organic polymers are a novel class of semiconductors that combine the optical and electronic properties of semiconductors with the advantages of low-cost processing, large-area scalability, compatibility with flexible substrates, and mechanical properties of polymers. Important examples of polymers within this class include poly(p-phenylene vinylene), poly(p-phenylene), polythiophenes, polyfluorene derivatives, and others. In general, the conducting polymers contain extended π-conjugated systems composed of single and double bonds alternating along the polymer chain (for an explanation of π-conjugation, *see* Chapter 2). The strong relation between electronic structure and backbone conformations is a fundamental feature of π-conjugated polymers. The extent of the π-conjugation is the essential structure parameter that controls the physical properties of conducting polymers. Within conducting polymers, carriers can be created by adding impurities. These impurities act as electron donors or acceptors, where the *carrier concentration* depends on the doping level (*i.e.*, amount of impurities present). For example, the introduction of acceptors into a polymer creates holes (positive charge carriers), resulting in structural defects in the alternation of the double and single bonds. These defects can travel along the polymer chain without changing its shape and represent localized solitary waves; they are responsible for localization of the electron states along the polymer chain. The defects can also be called *polarons* if single-charged and *bipolarons* if double-charged. A polaron is a *quasiparticle* that repulses adjacent electrons while attracting the nuclei of neighboring atoms. This results in the polarization of the lattice in its closest vicinity. This accompanying cloud of polarization causes an increased effective mass of the particle, decreasing the mobility of those quasiparticles. Those quasiparticles can be identified by additional energy levels, which appear within the semiconductor bandgap. Polarons in conjugated systems affect not merely the polarization in their vicinity but they can also change the nature of bonds from σ to π and vice versa via excitation and while traveling. The strong electron-lattice coupling is responsible for the existence of polarons in conjugated systems.[1]

In general, the conductivity in polymers is one-dimensional on the molecular scale. Therefore, the polymers can be represented as a one-dimensional disordered system, in which electron states are localized due to defects along the chain. The physical reason for localization is interference of forward- and backward-scattered electron wave functions, forming

standing waves. The situation changes if electrons can be transferred between the chains. If the electrons can move off the chain before they scatter backwards, they become effectively delocalized. Let the inter-chain exchange rate be I_{RE} and the mean free time of an electron moving along chain τ. Then the condition of delocalization is expressed by

$$I_{RE} > \frac{1}{2}\tau \tag{4.2.1}$$

There exists a threshold value of I_{RE}

$$I_{RE}^{C} \approx \frac{1}{\tau} \tag{4.2.2}$$

above which electron states become three-dimensional, and below which they are localized on a single chain. Therefore, three-dimensional conductivity will occur when the interchain transfer rate is high enough.[2] However, even if the conductivity in polymers is one-dimensional on the molecular scale, the bulk samples (and device structures) have a three-dimensional conductivity because macromolecules are assembled into three-dimensional structures, and their conductivity will be highly dependent on the thin film morphology. In conducting polymers, one can distinguish *intra-chain* and *inter-chain* transport mechanisms. Intra-chain transport depends on intrinsic properties of macromolecules and the doping level. Inter-chain transport is a function of the polymer morphology and the packing density.

Bulk electronic conduction that is observed in device structures described in this chapter is a result of these processes. If the polymer chain packing is not perfect, inter-chain disorder will reduce the inter-chain transfer rate, and hence decrease the conductivity. It can be argued that polymer chains are packed into a bundle and are well ordered within the bundle, and that the electronic behavior of particular films is controlled by the dimensions and ordering of the bundles. The conductivity in randomly oriented polymers used in OFETs depends on the pathways that are available for carriers to organize a macroscopic electronic current between two contacts. It is expected that the structural order (that can be influenced by solvent polarity, solid content in the solution, thermal treatment and film deposition method) in an intrinsically conducting polymer will have a pronounced influence on its charge transport and device electrical characteristics. For instance, it is expected that the inter-chain transport will

be favorable for high-density crystalline packing of macromolecules because of the relatively small value of the energetic barriers. Therefore, film conductivity will increase with the thermal annealing of samples, leading to an increase in the degree of crystallinity.

In summary, order is one of the key properties of conducting polymers that can have a major effect on electrical performance of devices such as field-effect transistors. The organic materials used in device structures described in this chapter are as-deposited disordered organic polymers.

4.2.2 Device Structures

Since in most of the published papers, the electrical properties of organic thin-film transistors (OFETs) are analyzed using models and carrier transport equations developed for inorganic thin-film transistors (TFTs),[3,4] it is important first to summarize the physics of the TFTs before describing the electrical properties of OFETs. Inorganic TFT operation is based on the crystalline silicon (c-Si) metal-oxide-semiconductor field-effect transistor.

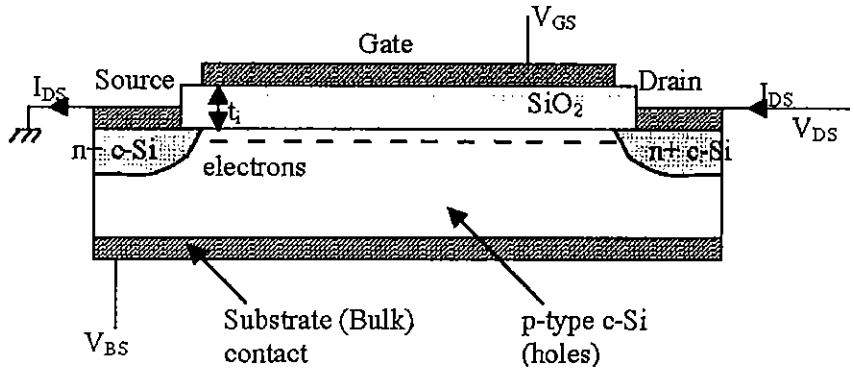

Figure 4.2.1. Typical MOSFET device structure.

The structure of a typical metal-oxide-semiconductor field-effect transistor (MOSFET) is shown in Figure 4.2.1. This cross-section shows an *n*-channel enhancement mode inorganic device built on a *p*-type single crystal silicon (c-Si) substrate, designated as *B* (bulk). The source and drain electrodes are heavily doped *n*-type (*n*+) c-Si regions covered with metal. (An *n*-type material contains impurities, such as phosphorous, which create a

material containing an excess of electrons. Increasing the concentration of dopants generally increases the electrical conductivity of the material.) The heavily doped region creates improved electrical contact between the source and drain electrodes and the metal interconnects used to connect the device to other circuit elements. The gate electrode is separated from the *p*-type c-Si by a gate insulator film (SiO_2) formed by thermal oxidation of the c-Si surface. (A *p*-type material is similar to an *n*-type material, except the dopants create a material with an excess of holes, which are essentially "missing" electrons. Since this missing electron behaves like a positively charged particle, for convenience it is usually treated as such.) Thermal oxidation is a process where a material is heated to a very high temperature (800 to 1200 °C), while being subjected to an oxidizing substance (such as oxygen gas or water vapor). The MOSFET is characterized by its channel length (L), which is the gap between the electrically conductive source and drain electrodes, its channel width (W) (the length of this gap), and the thickness of the gate insulator (t_i). When a positive voltage bias (V_{GS}) is applied to the gate electrode, a conducting channel is formed by accumulation of electrons at the semiconductor/gate insulator interface. This reduces the effective resistance of the path between source (S) and drain (D), allowing the MOSFET drain current (I_{DS}) to flow between the source and drain electrodes if there is a source-drain bias (V_{DS}) applied between them. To collect electrons at the source and drain contacts, *n*+ c-Si regions are needed. The MOSFET is usually a symmetric device in which there is no difference between source and drain; for an *n*-channel device in which the channel carriers are electrons, the source is usually grounded and the substrate-channel junction must be reverse-biased for normal device operation (Figure 4.2.1). This device operates in inversion mode, *e.g.*, electrons are accumulated within a *p*-type semiconductor. Polarities are reversed for a *p*-channel device in which the majority carriers are holes, the substrate is *n*-type c-Si and the source/drain regions are heavily doped *p*-type c-Si (*p*+ c-Si). More details about MOSFETs can be found in Reference 5.

The structure of a typical *n*-channel inorganic thin-film transistor (TFT) is shown in Figure 4.2.2. Many other TFT structures are possible and have been discussed by the authors in Reference 6. In most inorganic TFTs, the active layer is often either hydrogenated amorphous silicon (a-Si:H) or polycrystalline silicon (poly-Si) and is typically 50 to 150 nm thick. Amorphous silicon has virtually no crystal structure, where silicon atoms are randomly arranged. Polycrystalline silicon represents a state between amorphous and crystalline silicon, where some short-range order is present in small crystals that are randomly oriented throughout the material. Since these devices are not fabricated using the more highly-ordered crystalline silicon, both a-Si:H and poly-Si contain defects that introduce electronic

states (trap states) within the semiconductor bandgap. In other words, the defects in the disordered structure create electrical impediments to the flow of electrons and holes. In a-Si:H, these defects are distributed uniformly within the bulk of the film, while in poly-Si they are mostly localized at grain boundaries. In both cases, the Fermi level in the undoped material is typically near midgap level. The Fermi level is a mathematical indicator of the type and concentration of overall doping (natural or due to added impurities) in a material. When it is at midgap, essentially an equal number of electrons and holes are present in the material. A material in an "undoped" state is referred to as an "intrinsic" material. Therefore, doping of a-Si:H and poly-Si is possible and both *n*- and *p*-type materials can be produced. When *n*-type material is used for the channel material, the source and drain contacts use heavily doped *n*-type (*n*+) a-Si:H regions while *p*+ a-Si:H source and drain contacts are used for *p*-channel TFTs. This device arrangement is the opposite of what is used in MOSFETs. The gate insulator of most TFTs is amorphous silicon oxide (a-SiO_x:H, essentially glass) or amorphous silicon nitride (a-SiN_x:H, a common insulating material in microelectronics) deposited by plasma-enhanced chemical vapor deposition (PECVD). PECVD is a deposition process that uses radio-frequency (RF) discharge and gas mixtures. The excited species flow over the substrate and form a thin film on the top of the substrate. In *n*-channel TFTs, electrons accumulate near the gate insulator/semiconductor interface when a positive voltage bias is applied on the gate electrode, see Figure 4.2.2. In TFTs, there is no creation of an inversion layer but rather an accumulation layer, composed of majority carriers, is formed at the semiconductor/gate insulator interface. In other words, in an *n*-channel device, the conductive layer at the semiconductor/ gate interface is composed of a large number of electrons; in a *p*-channel device, this layer consists of holes.

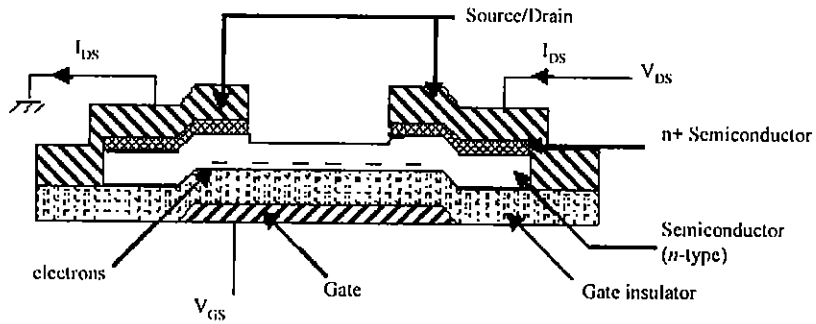

Figure 4.2.2. Typical TFT device structure.

In organic thin-film transistors (OFETs), the semiconductor active layer is a thin organic film (having a thickness t_{SC}), which can be fabricated by vacuum deposition, printing, or from solution (by spin-coating for instance).[7] The OFET structure is often very similar to the one of the inorganic amorphous or polycrystalline semiconductor TFTs, Figure 4.2.3. OFET device structures can be divided into two categories: coplanar and staggered structures. In coplanar OFETs, the gate, source and drain electrodes are all located on the same side of the organic semiconductor film. In staggered devices, the gate electrode is on the opposite side of the organic semiconductor film from the source and drain electrodes. Staggered OFETs are further subdivided into top- or bottom-gate OFETs, depending on the position of the gate electrode, on the top or bottom side of the organic semiconductor film, respectively. Examples of OFET cross-sections are shown in Figure 4.2.3. Independently of the OFET device structures shown in Figure 4.2.3, there are different possible source-drain electrode arrangements. Figure 4.2.4 shows top views of standard, Corbino, and interdigitated device structures. In all these devices, the source and drain electrodes (traditionally often Au or ITO) are usually directly in contact with the organic semiconductor, *i.e.*, without the use of a heavily doped interfacial layer, as it is common in inorganic devices. Like inorganic devices, the OFET is also characterized by the channel length (L) between source and drain electrodes and the channel width (W). The gate insulator can again be composed of traditional microelectronics materials, such as thermal silicon dioxide (SiO_2), amorphous silicon oxide, amorphous silicon nitride, aluminum oxide, or others (see Section 4.2.6.4). Patterned gate electrodes can be made of metals such as chromium, aluminum, or transparent conducting oxides such as indium tin oxide (ITO). When a non-defined gate electrode is used (this is typical practice when new organic semiconducting materials are being evaluated), highly doped (n+) c-Si is often used as the gate electrode and thermal SiO_2 is often used as gate insulator. It should also be noted that most organic semiconductors are naturally p-type, and therefore most OFETs are p-channel devices operating in accumulation enhancement mode. As described before, this means that holes are the majority carriers, which accumulate and create a conductive path at the gate insulator/organic semiconductor interface. Attempts to dope organic semiconductors have often led to ambiguous results. Typically, the preferred route to n-channel devices is to use a naturally n-type material. So far, major problems with n-type organic semiconductors are attributed to material instability with respect to oxygen. However, n-type organic semiconductors for OFETs have recently been produced.[8]

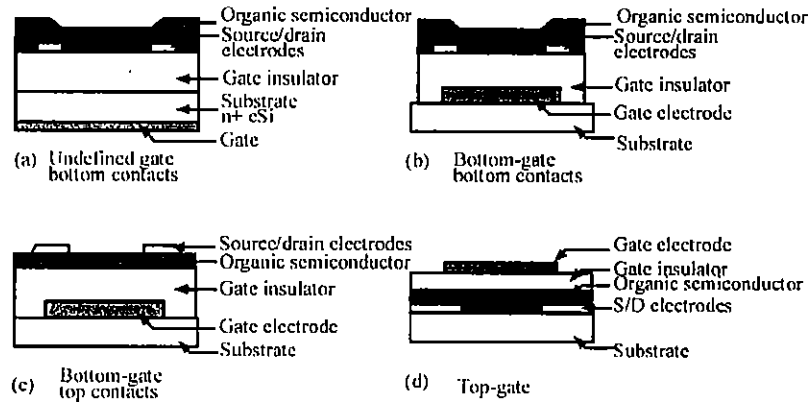

Figure 4.2.3. Examples of OFET device structures. (*a*) Coplanar OFET with non-defined gate electrode. (*b*) Coplanar OFET with defined gate electrode. (*c*) Staggered bottom-gate OFET. (*d*) Staggered top-gate OFET.

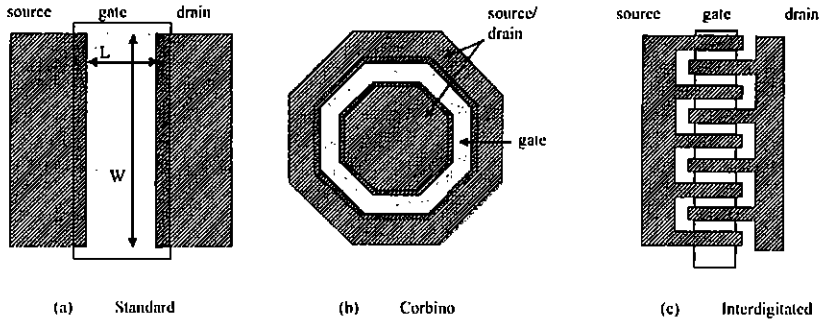

Figure 4.2.4. Top-views of OFET device structures. (*a*) Standard OFET. (*b*) Corbino OFET. (*c*) Interdigitated OFET.

4.2.3 Device Operation Principles

4.2.3.1 c-Si MOSFET Operation

The theory of operation of a MOSFET is well known and will not be discussed in detail here. However, some of the basic principles that are most

useful for OFET analysis will be described. Note that the following section is intended to describe transistor operation in detail in order to give the reader a detailed, quantitative understanding of FET operation. The reader is walked through the derivation of the most important equations used to describe the transistor operation. Full understanding of this material may require at least some background in semiconductor device physics, due to the large amount of terminology and detail in this section. A conceptual description of transistor operation can be found in Section 4.2.2.

For an *n*-channel MOSFET under a positive gate voltage bias (V_{GS}), thermally generated free electrons are capacitively induced (*i.e.*, appear on the opposite end of the gate insulator when a voltage is applied to the gate) at the semiconductor/gate insulator interface. These minority carriers (holes outnumber electrons) create an inversion channel or space charge (in other words, a conductive path) in the *p*-type bulk c-Si, the MOSFET is therefore said to operate in inversion mode. The charge in the semiconductor is composed of the depletion charge, associated with the depletion (*i.e.*, removal) of majority carriers (holes) and the inversion charge, associated with the accumulated electrons at the semiconductor/gate insulator interface (channel). When the concentration of electrons in the channel region becomes higher than the hole concentration in the bulk of the semiconductor, the device is in the strong inversion regime, as shown in Figure 4.2.5.

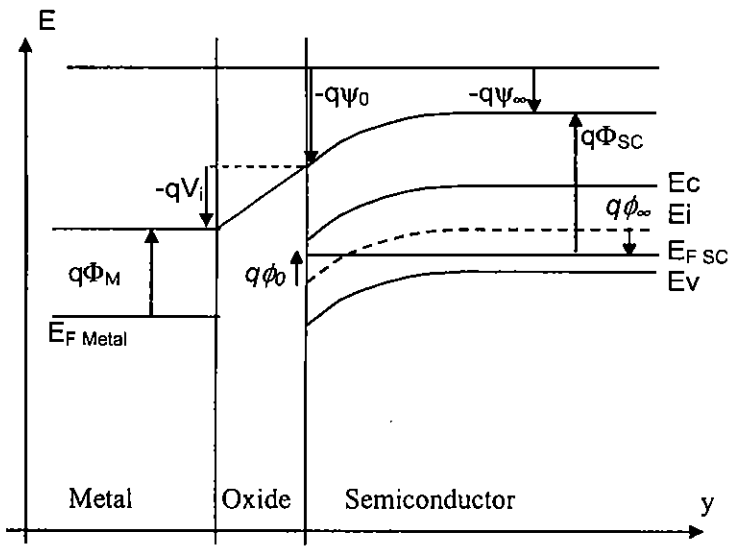

Figure 4.2.5. Typical electronic band structure of an *n*-channel MOSFET in inversion regime.

Here it is assumed that the band bending does not significantly change with further increase of the gate voltage and, based on the balance of charges in the structure, the conduction channel (or inversion) charge can be expressed as

$$Q_{cond} = -C_i(V_G - V_{SC}) + C_i(\Phi_M - \Phi_{SC}) - Q_{depl} - 2C_i\phi_\infty \quad (4.2.3)$$

where Q_{cond} is the conduction charge, C_i is the gate insulator capacitance per unit area, V_G is the voltage applied on the gate, V_{SC} is the voltage applied on the semiconductor, Φ_M is the metal work function, Φ_{SC} is the semiconductor work function, Q_{depl} is the depletion charge and φ_r is the potential difference between the Fermi level and the intrinsic level in the bulk of the semiconductor. For a *p*-type semiconductor,

$$\phi_\infty = -\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) < 0 \quad (4.2.4)$$

where N_A is the density of acceptor dopants (*p*-type semiconductor) and n_i is the intrinsic carrier density. If the variations of Q_{depl} with the gate voltage and along the conduction channel are neglected, the resolution of Poisson equation gives

$$Q_{depl} = -\sqrt{-4qN_A\varepsilon_{SC}\varepsilon_0\phi_\infty} \quad (4.2.5)$$

where ε_{SC} is the semiconductor dielectric constant and ε_0 is the vacuum permittivity (also known as the *permittivity of free space*). The device threshold voltage, also supposed to be independent of the gate voltage and the position along the conduction channel, can be defined as

$$V_T = (\Phi_M - \Phi_{SC}) + \frac{\sqrt{-4qN_A\varepsilon_{SC}\varepsilon_0\phi_\infty}}{C_i} - 2\phi_\infty \quad (4.2.6)$$

The expression of the conduction charge then becomes

$$Q_{cond} = -C_i(V_G - V_{SC} - V_T) \quad (4.2.7)$$

If a source-drain voltage is applied between the source and drain electrodes and if it is assumed that the Fermi potential gradient is mostly along the *x*-axis (gradual channel approximation), the current density is, for an *n*-channel device

$$J_n(x) = -q\mu_n n \frac{d\varphi_n}{dx} \tag{4.2.8}$$

where $d\varphi_n/dx$ is the gradient of the Fermi potential in the semiconductor channel. Consequently, the drain current $I_{DS} = I_D = -I_S$ is obtained

$$I_{DS}(x) = -\iint J_n dydz = -\mu_n \frac{d\varphi_n}{dx} W Q_{cond}(x) \tag{4.2.9}$$

where it has been assumed that the current I_{DS} is positive when flowing from drain to source, *i.e.*, in the negative x-axis direction. Combining Equations 4.2.7 and 4.2.9, the following equation is obtained

$$I_{DS}(x) = \mu_n W C_i \frac{d\varphi_n}{dx}\left[(V_G - V_{SC}(x)) - V_T\right] \tag{4.2.10}$$

Because the current flowing through the channel is constant, the following relationship is made

$$I_{DS} = \frac{1}{L}\int_0^L I_{DS}(x)dx \tag{4.2.11}$$

which results in, assuming that the field-effect mobility, μ_n, does not depend on x

$$I_{DS} = \mu_n \frac{W}{L} C_i \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{4.2.12}$$

where μ_n is the field-effect mobility of the electrons, W and L are the channel width and length, respectively, C_i is the gate insulator capacitance per unit area and V_T is the MOSFET threshold voltage as defined by Equation 4.2.6. This model assumes that the source-drain voltage is sufficiently low so that the entire conduction channel (from source to drain) is in strong inversion. It also assumes that the depletion charge and, consequently, the threshold voltage, depend mostly on the gate voltage, and that their dependence on the position in the conduction channel can be neglected. These assumptions correspond to the so-called *MOSFET gradual channel approximation*.

Equation 4.2.12 is valid as long as the whole channel remains in accumulation, *i.e.*, there is no channel pinch off. This assumption is true for

$$V_{DS} \le V_{GS} - V_T \tag{4.2.13}$$

For larger values of the source-drain voltage, the current saturates and is given by

$$I_{DS} = \mu_n \frac{W}{2L} C_i (V_{GS} - V_T)^2 \tag{4.2.14}$$

Ideally, the values of μ_n and V_T used in both equations (linear and saturation regimes) should be the same. However, these two different operation regimes of the MOSFET are not affected equally by second-order effects and this can result in slight discrepancies between the linear and saturation parameters.

Before the MOSFET reaches strong inversion, it is said to be in the subthreshold regime. In this case, the band bending in the semiconductor still depends significantly on the gate voltage. Solving the Poisson equation (*see* Equation 4.2.23) yields the following expression of the conduction channel charge

$$Q_{cond} \approx -kT\sqrt{\frac{N_A \varepsilon_{SC}\varepsilon_0}{2q(\phi_0 - \phi_\infty)}} \cdot e^{\frac{q(\phi_0 + \phi_\infty)}{kT}} \tag{4.2.15}$$

where φ_0 is the potential difference between the Fermi level and the intrinsic level at the semiconductor/gate insulator interface. This equation becomes, after assuming that the device is close to the onset of strong inversion and making a few approximations

$$Q_{cond} \approx -kT\sqrt{\frac{-N_A \varepsilon_{SC}\varepsilon_0}{4q\phi_\infty}} \cdot e^{\frac{q(V_G - V_{SC}(x) - V_T)}{nkT}} \tag{4.2.16}$$

The expression of the MOSFET current is then

$$I_{DS}^{subthreshold} = \mu_n \frac{W}{L} kT\sqrt{\frac{-N_A \varepsilon_{SC}\varepsilon_0}{4q\phi_\infty}}\left(\frac{nkT}{q}\right) e^{\frac{q(V_{GS} - V_T)}{nkT}}\left[1 - e^{-\frac{qV_{DS}}{nkT}}\right] \tag{4.2.17}$$

where an additional parameter has been introduced

$$n = 1 + \frac{1}{2C_i}\sqrt{-\frac{qN_A\varepsilon_{SC}\varepsilon_0}{\phi_\infty}} \qquad (4.2.18)$$

From the MOSFET drain current expression, the subthreshold swing, S, is defined by

$$S = \left(\frac{d\log I_{DS}^{subthreshold}}{dV_{GS}}\right)^{-1} \qquad (4.2.19)$$

which yields

$$S = \frac{nkT}{q\log(e)} = \frac{kT}{q\log(e)}\left(1 + \frac{1}{2C_i}\sqrt{-\frac{qN_A\varepsilon_{SC}\varepsilon_0}{\phi_\infty}}\right) \qquad (4.2.20)$$

Consequently, in an ideal MOSFET, the subthreshold swing is associated with the density of acceptors in the bulk of the semiconductor.

4.2.3.2 Inorganic TFT Operation

Inorganic TFTs operate differently than the c-Si MOSFET. In these TFTs, there is no depletion region and current can flow between source and drain even when there is no bias voltage on the gate electrode. In this case, the level of this source-drain *leakage current* depends on the film thickness and electronic quality, as indicated by the following equation

$$I_{leakage} \approx \frac{\sigma_d dWV_{DS}}{L} \qquad (4.2.21)$$

where σ_d is the semiconductor dark conductivity, and d its thickness. In general, low off-currents can be obtained in TFTs because of the characteristically low electrical conductivity of the inorganic amorphous or polycrystalline semiconductors. Since the TFT operates in accumulation mode, which is different from most MOSFETs, which operate in inversion mode, care has to be taken when using equations derived for MOSFETs to describe the TFT operation.

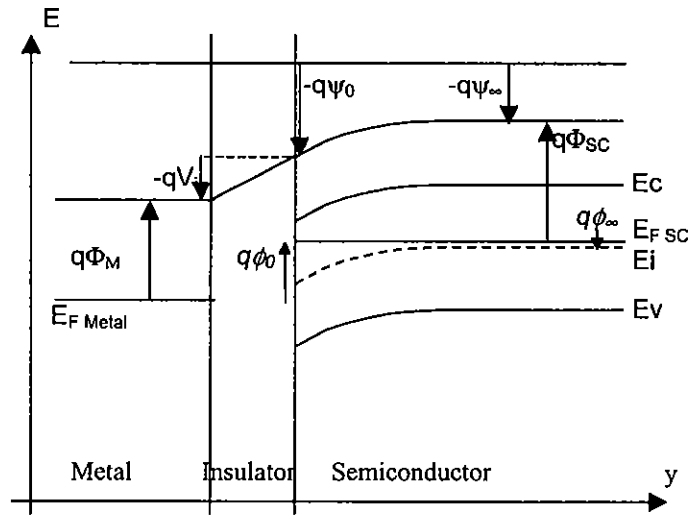

Figure 4.2.6. Typical electronic band structure of an *n*-channel TFT in accumulation regime.

The main difference between the c-Si MOSFET and the a-Si:H TFT is the expression of the charge in the semiconductor, which does not involve a depletion charge (as the semiconductor is usually not doped), but includes contributions from carriers trapped at states present in the inorganic semiconductor bandgap. Figure 4.2.6 shows the electronic band diagram of an *n*-channel TFT in the accumulation regime. The equations describing the TFT operation in the accumulation and subthreshold regimes are established in a similar way to what has been done for the MOSFET, by taking into consideration the balance of charges in the device structure

$$V_G - V_{SC} = (\Phi_M - \Phi_{SC}) - \frac{Q_{SC}}{C_i} + (\phi_0 - \phi_\infty) \qquad (4.2.22)$$

and the Poisson equation

$$\frac{d^2\phi}{dy^2} = -\frac{\rho(y)}{\varepsilon_{SC}\varepsilon_0} \qquad (4.2.23)$$

Often, different non-idealities of the device structure and materials have to be included when establishing the equations above. First, the contributions of the fixed charges within the insulator layer or at the semiconductor/gate insulator interface (Q_i) may have to be included

$$V_G - V_{SC} = (\Phi_M - \Phi_{SC}) - \frac{Q_{SC}}{C_i} + (\phi_0 - \phi_\infty) - \frac{Q_i}{C_i} \qquad (4.2.24)$$

In addition, the density of defect states at the semiconductor/gate insulator interface (N_{ss}) may also need to be considered. Assuming that these density of states distributions are constant within the semiconductor bandgap and that the states are donor-type below midgap and acceptor-type above midgap, their contribution to the device charge is

$$Q_{ss} = -q^2 N_{ss}(\phi_0 - \phi_\infty) \qquad (4.2.25)$$

Finally, defect states (N_T) are also present in the bulk of the semiconductor and need to be taken into account in the balance of charges and for the solution of Poisson equation. Assuming that there is a constant distribution of defect states within the semiconductor bandgap, donor-type below midgap and acceptor-type above midgap, their contributions to the semiconductor density of charge is

$$\rho_T(y) = -q^2 N_T \phi(y) \qquad (4.2.26)$$

Because of the complex expression of these non-idealities, solving Poisson and balance of charge equations is not as simple as for c-Si MOSFETs, even in the accumulation regime.[6,9,10,11] However, after a few approximations, it is usually possible to obtain equations describing the *n*-channel TFT operation in the accumulation regime, in the linear, and the saturation regime, respectively, that are similar to the ones developed for c-Si MOSFETs

$$I_{DS}^{lin} = \mu_{FE} C_i \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (4.2.27)$$

and

$$I_{DS}^{sat} = \mu_{FE} C_i \frac{W}{2L}(V_{GS} - V_T)^2 \qquad (4.2.28)$$

In this case, the mobility μ_{FE} is the device field-effect mobility, which is usually lower than the free carrier band mobility because of the presence of gap states. The threshold voltage V_T is not directly associated with the characteristics of the materials, as in the case of the c-Si MOSFET (Equation 4.2.6), but is defined by the gate voltage for which the TFT conduction charge equals zero. Charges present in the insulator film or at the gate insulator/ semiconductor interface only result in a voltage shift of the TFT characteristics, *i.e.*, shift of V_T without a change in Equations 4.2.27 and 4.2.28. On the other hand, defect states in the semiconductor or at the gate insulator/semiconductor interface would affect the device characteristics and response. In addition, if defect states having an exponential energy dependence (such as band tails) in the amorphous or polycrystalline semiconductor bulk are taken into account, the expression of the charge localized on the defect states is more complex and the expressions of the TFT current (Equations 4.2.27 and 4.2.28) need to be modified. More details on this subject are provided in References 6-11.

When the TFT is in the weak accumulation regime, the calculation is similar to that used for the MOSFET, but taking into account the contribution of defect states to the semiconductor charge is critical. Assuming that there is a constant density of states N_T in the bulk of the semiconductor and a density of surface states N_{ss} at the semiconductor/gate insulator interface, an expression similar to Equation 4.2.17 can be obtained

$$I_{DS}^{subthreshold} = I_0 \exp\left(\frac{qV_{GS}}{nkT}\right)\left(1 - \exp\left(\frac{qV_{DS}}{nkT}\right)\right) \qquad (4.2.29)$$

with n now defined as follows

$$n = 1 + \frac{\sqrt{q^2 N_T \varepsilon_{SC} \varepsilon_0}}{C_i} + q^2 \frac{N_{ss}}{C_i} \qquad (4.2.30)$$

Using the same definition as for the MOSFET (Equation 4.2.20), the following expression of the subthreshold swing is obtained

$$S = \frac{kT}{q\log(e)}\left[1 + \frac{\sqrt{q^2 N_T \varepsilon_{SC} \varepsilon_0}}{C_i} + q^2 \frac{N_{ss}}{C_i}\right] \qquad (4.2.31)$$

The subthreshold swing S increases with increasing density of defect states. From this equation, is can be concluded that the separation of the

individual contributions of N_T and N_{ss} to S is not possible from the analysis of S alone. Other experimental methods should be used to determinate N_T and N_{ss} independently from each other. For example, electron spin resonance method can be used to measure N_T and capacitance–voltage technique can be used to find N_{ss}.

It is noted that, if the density of defect states in the amorphous semiconductor is constant within the semiconductor bandgap, the *Debye screening length* (L_D) can be defined. It represents the distance over which the electrical field penetrates into the semiconductor film. The Debye screening length is given by the following equation

$$L_D = \sqrt{\frac{\varepsilon_{SC}\varepsilon_0}{q^2 N_T}} \tag{4.2.32}$$

In general, if the bulk density of defect states N_T is not constant over the gap, the Debye screening length is still expected to be correlated to the distance over which the electrical field penetrates into the semiconductor film. Typical values for inorganic semiconductors are 250 nm for a-Si:H ($N_T \sim 10^{16}$ cm^{-3}·eV^{-1}) and 50 nm for poly-Si ($N_T \sim 3 \times 10^{17}$ cm^{-3}·eV^{-1}). It should be noted that small values of the screening length or a high density of defects would make the semiconductor unattractive for TFT applications. To obtain low TFT OFF-current, the undepleted region of the TFT should be maximized, *i.e.*, a large Debye screening length is desired.

The TFT equations for *p*-channel devices would be very similar to the equations developed above for *n*-channel TFTs, with only a change of sign resulting from the majority carriers being holes instead of the electrons that are present in *n*-channel TFTs.

4.2.3.3 OFET Operation

It is now well established that the physics of the carrier transport is, in many respects, different from that of inorganic thin-film amorphous semiconductors. Nevertheless, OFETs exhibit electrical characteristics that are very similar in many respects to those of thin-film inorganic semiconductors.[12]

An important and general feature of organic polymers is that they are not well-ordered materials, where any crystalline phases present are always made of small, imperfectly ordered crystallites. Hence, the disorder present in organic polymers has an important electronic consequence, which is localization (*i.e.*, trapping) of charge carriers. Furthermore, the conformation of the chain within the microcrystalline polymers has static

fluctuations along its length, with the inter-chain interactions fluctuating as well. The potential fluctuations due to these effects are spread over some distance and usually are not very deep (so-called *weak disorder*). On the other hand, chemical defects, such as non-conjugated carbon atoms inserted within the chain or other impurities, may result in strong local potential variations (so-called *strong disorder*). Both types of disorder are important in limiting the conjugation length and in affecting the carrier transport within OFETs. The effect of disorder in organic polymers and its impact on OFET operation principle is a complicated problem and will not be addressed in this chapter. It is argued that weak disorder may be the main source of localization and the limitation of conjugation length. However, simultaneous trapping of a charge by deep gap states located at well-defined energies can generate a "localized" (*i.e.*, trapped) polaron, which can have a very long lifetime: of seconds or more. Organic polymers seem therefore to be different from amorphous silicon, in which localized state energies form continuous distributions (so called *band tail states*), extending deep into the gap. However, in amorphous inorganic semiconductors, localized deep-gap sates in addition to band tails are present. Generally, traps are expected to yield field-effect mobilities, which are both much lower than microscopic ones and vary with physical or electronic properties of the materials.

In general, organic field-effect transistors exhibit so-called *p*-channel behavior (where the majority carriers are holes) within a *p*-type organic semiconductor. Thus, when the gate electrode is biased positively with respect to the grounded source electrode, the channel region is depleted of carriers. This results in a high channel resistance (which is referred to as the '*off' state*). When the gate electrode is biased negatively, OFETs operate in the *accumulation mode*. In this state, a large concentration of holes is accumulated within the device channel, resulting in a low channel resistance (which is referred to as the '*on' state*). The accumulation layer is believed to be limited to the first few monolayers at the organic semiconductor/gate insulator interface. It has been shown that an organic semiconductor layer with a thickness equivalent to only few such monolayers is sufficient for proper OFETs operation, with additional thickness not substantially increasing the device 'on'-current.[8] The magnitudes of these 'on'- and 'off'-currents and the time required to switch between these two states determine the utility of a transistor in a organic circuits. The OFETs must produce enough 'on'-current to activate or switch another part of a circuit, but it must not generate off-currents that are large enough to cause unwanted switching.

To describe the OFET operation, the simplest model can be based on a *p*-channel thin-film transistor as developed for inorganic TFTs. In the accumulation regime, the drain current is given by the following equations, characterizing the linear and the saturation regimes, respectively

$$I_{DS}^{lin} = -\mu_{FE} C_i \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (4.2.33)$$

$$I_{DS}^{sat} = -\mu_{FE} C_i \frac{W}{2L}(V_{GS} - V_T)^2 \quad (4.2.34)$$

In the subthreshold regime, the drain current is expressed as

$$I_{DS}^{subthreshold} = I_0 e^{-\frac{qV_{GS}}{nkT}}\left(1 - e^{-\frac{qV_{DS}}{nkT}}\right) \quad (4.2.35)$$

In this model, it is assumed that the field-effect mobility is independent of the gate bias, and that the source/drain contacts are ohmic in nature. Experiments done at different laboratories have indicated that these assumptions are nor necessarily valid. Further details regarding the role of the source and drain contacts are provided in Section 4.2.6.1. A more detailed description of the device field-effect mobility and carrier transport mechanisms is given in Section 4.2.6.2.

4.2.4 Measurement of Device Electrical Characteristics

Unless otherwise specified, all experimental data shown in this chapter has been obtained on gate-planarized OFETs based on solutions of the semiconducting polymer poly(9,9-dioctylfluorene-co-bithiophene) (F8T2), which is described in greater detail in References 13, 14, 15, and 16.

Typical OFET output characteristics (I_{DS} vs. V_{DS}) are plotted in Figure 4.2.7 (top). As is generally expected for field effect devices, the linear regime can be identified for low drain voltages, and the saturation regime for higher drain voltages. The derivatives of the I_{DS} vs. V_{DS} curves are used to identify any possible current crowding near the origin. Figure 4.2.7 (bottom) shows almost monotonic curves, which are associated with the absence of significant current crowding. This suggests that the drain current of this OFET is not limited by the carrier injection between the organic materials and the source and drain contacts. This might not be the case for devices based on high-mobility organic materials. Typical transfer curves (I_{DS} vs. V_{GS}) in the linear regime and $\sqrt{|I_{DS}|}$ vs. V_{GS} curves in the saturation regime for the same device are plotted in Figure 4.2.8 (top). Transfer characteristics are used to show the effect of an input to a device on its response. For TFTs, the input is the voltage on the gate, and the output is the resulting current

through the channel. Since the field-effect mobility (μ_{FE}) in the saturation regime can be directly extracted from a curve fit of the $\sqrt{|I_{DS}|}$ vs. V_{GS} plot, it is common practice to include such a plot with OFET data. Transfer plots are generated using one or more drain voltages (V_{DS}), held constant for each curve shown. These transfer curves exhibit behaviors that are consistent with the MOSFET theory described in Section 4.2.3.1. A semilogarithmic plot of the OFET transfer characteristics for a drain voltage $V_{DS} = -10$ V is shown in Figure 4.2.8 (bottom), in which the off-, subthrehsold- and on-regimes can be observed.

4.2.4.1 Standardized Measurement Procedure

One of the most critical issues during OFET measurements is the establishment of the *device permanent regime*. In other words, it is critical to ensure that the device is electrically stable so that measurements performed at two different times will closely resemble each other. Other critical factors that need to be considered are acceptable measurement reproducibility and minimal device aging.

It is usually assumed that, during OFET electrical characterization, the device is in a steady-state regime (*i.e.*, its electrical behavior is stable over time) and that any transient phenomena (short-lived electrical effects) do not affect the measured values. This is to ensure that the measured TFT drain current is meaningful. Transient phenomena can be associated with carrier thermalization,[17] which can be defined as a process related to the trapping of carriers in deep-gap defect states and the emission of carriers from these states. Thermalization occurs on a very small time frame in the 'on' state because of large concentration of accumulated carriers.

Since in OFETs the organic materials have large bandgaps, the concentration of accumulated carriers in the device 'off' state is low and the carrier thermalization is much slower. It is therefore recommended to usually start the transfer characteristic measurement (I_{DS} vs. V_{GS}) in the 'on' state, and then sweep the gate voltage towards the 'off' state. This technique ensures that the OFET is in steady-state regime throughout most of the transfer characteristic measurement.

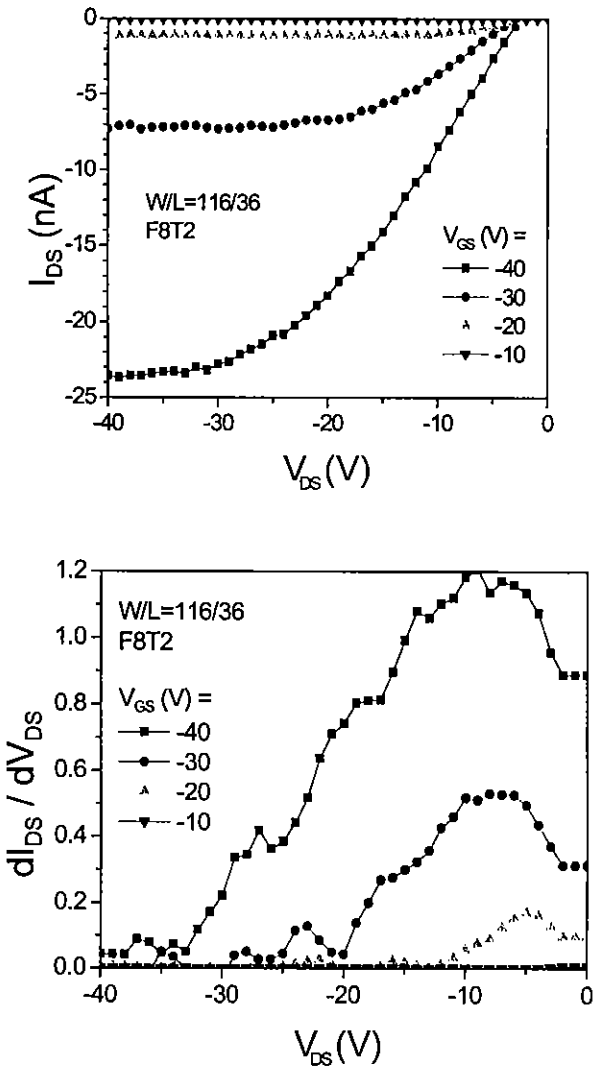

Figure 4.2.7. (top) Typical output characteristics (I_{DS} vs. V_{DS}) of organic polymer TFTs. *(bottom)* Derivatives of the curves shown around the origin.

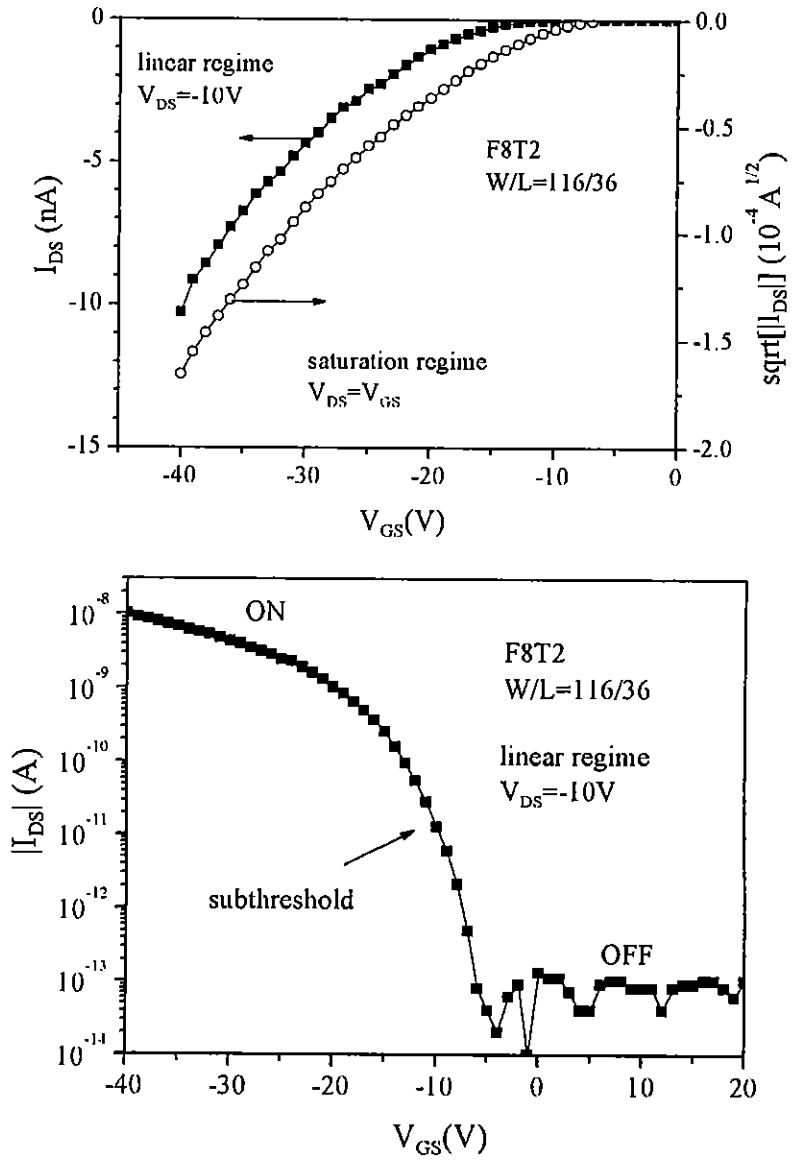

Figure 4.2.8. (top) Linear plots of typical transfer characteristics of OFETs in linear and saturation regimes ($V_{DS} = -10$ V and $V_{DS} = V_{GS}$, respectively). The I_{DS} vs. V_{GS} curves are plotted in linear regime and $\sqrt{|I_{DS}|}$ vs. V_{GS} in the saturation regime. *(bottom)* Semilog plot of typical transfer characteristics of OFETs in the linear regime.

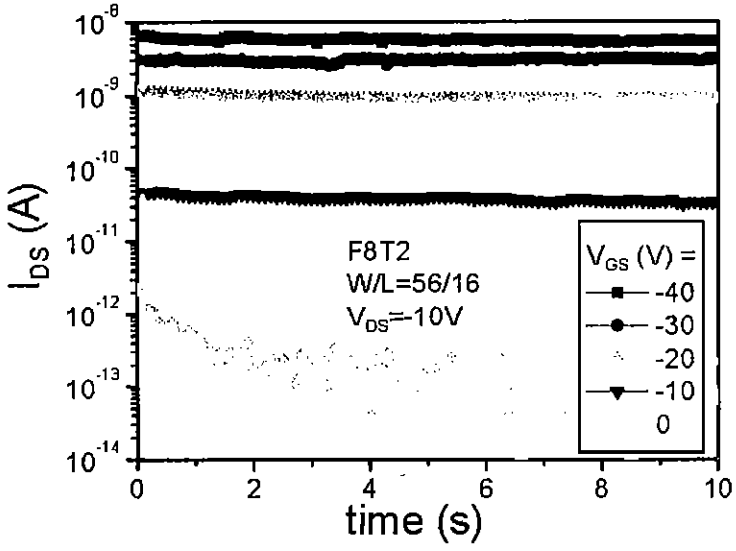

Figure 4.2.9. Short-term time evolution of the OFET drain current, for different gate voltages.

It should be noted that, in most measurements at room temperature and in the dark, the OFET is not in steady-state when the off-current is measured. Performing measurements in the dark is usually important for OFETs, as light can induce electrical effects and therefore significantly alter the measured electrical response of the device. Because of the thermalization process, a significant time dependence of the OFET electrical characteristics is observed. It can be seen in Figure 4.2.9 that a significant time, typically a few seconds, is needed before the OFET drain current stabilizes, *i.e.*, before the OFET reaches the steady-state regime. Carrier thermalization is achieved faster for larger negative gate voltages. The time dependence of the OFET drain current is also significant for long time scales, but the decrease in the OFET current in this case results from a shift of the current-voltage characteristic, associated with device aging.

During the output characteristic (I_{DS} vs. V_{DS}) measurements, the gate voltage is constant and the OFET accumulation state does not change: the device is usually in accumulation during all the output characteristics measurements. Carrier thermalization is therefore not expected to be an issue, regardless of the conditions used.

4.2.4.1.1 Measurement Methods

The electrical characteristics of organic thin-film transistors are usually measured by applying a series of gate and drain voltages and measuring the resulting currents. The gate and/or drain voltages are swept over a specific range, and the corresponding OFET drain current is measured. Due to a variety of transient (short-lived) effects, the gate voltage is typically set to its initial value and is held for a pre-selected time (referred to as the *hold time*) before the voltage sweep begins. Each voltage step is also sometimes followed by a *delay time* before the appropriate current is measured.

The OFET output characteristic (also known as the *I vs. V output* or simply *I vs. V curves*) is measured by sweeping the drain voltage (V_{DS}) while keeping the gate voltage (V_{GS}) constant. Often, a series of curves is generated, each using a different value for the gate voltage, with the series of curves shown in a single plot. Transfer characteristics are usually measured by sweeping the gate voltage (V_{GS}) and keeping the drain voltage (V_{DS}) constant. However, transfer characteristics in the saturation regime are often measured by sweeping together both gate and drain voltages (*i.e.*, $V_{DS} = V_{GS}$). Transfer characteristics are often more sensitive to measurement conditions than output characteristics, because the OFET accumulation state changes throughout the measurement.

4.2.4.1.2 Measurement Parameters

Because of the time needed for the drain current stabilization, the hold time and delay time parameters used in the OFET characterization studies can affect the measured curve. Consequently, this affects the accuracy of the OFET electrical parameters extracted from these measurements, such as field-effect mobility, threshold voltage and subthreshold swing. Following the reasoning described above, the effect of the hold and delay times is related to both the establishment of the steady-state regime (which has already been described as necessary to obtain meaningful results) and device aging (which should be reduced as much as possible). The hold time has only an effect immediately before the characteristic measurement, and since the gate voltage is swept from negative to positive values, the applied voltage during the hold time is typically selected as –40V (in the case of the devices characterized by the authors). Often for this voltage, the OFET is in the strong accumulation regime, and the steady-state regime is reached almost immediately. As seen in Figure 4.2.10, the main effect of the hold time is therefore device aging, which is not desirable and should be minimized. Consequently, the hold time should be kept to a minimum for

accurate measurement. On the other hand, the delay time affects the measured OFET drain current during the entire measurement. Very long values of the delay time lengthen the measurement duration and can result in significant device aging, as shown in Figure 4.2.11. However, when the OFET is no longer in the strong accumulation regime (at relatively low gate voltages), the delay time is sometimes needed to obtain stable current values. A compromise must therefore be reached.

In addition, when large gate voltages are used, sweeping the gate voltage from the 'on' to the 'off' state could result in an apparent shift of the OFET characteristic towards more negative voltages, as seen in Figure 4.2.12. The curves shown in Figure 4.2.12 have been measured by sweeping the gate voltage from the OFET 'off' state ($V_{GS} = 0$ V) to the 'on' state ($V_{GS} = V_{GS\ max}$), then back to 'off' state ($V_{GS} = 0$ V). A very large shift, or hysteresis, is observed between transfer characteristics measured using successive forward and reverse sweeps. It is the opinion of the authors that this observed hysteresis, also reported by others,[18,19] could be associated with trapped charges present near the gate insulator/organic semiconductor interface. The density of charges can be estimated by using

$$Q_{hyst} = C_{ins} \times \Delta V_{GS} \tag{4.2.36}$$

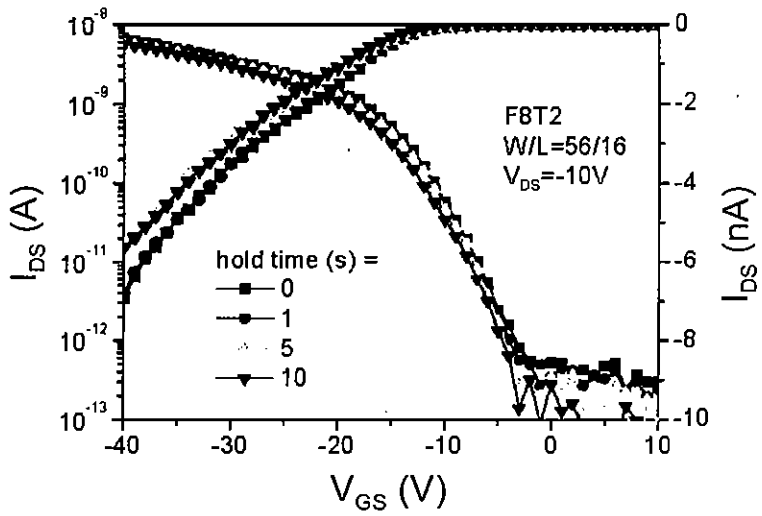

Figure 4.2.10. OFET transfer characteristics for different values of the hold time.

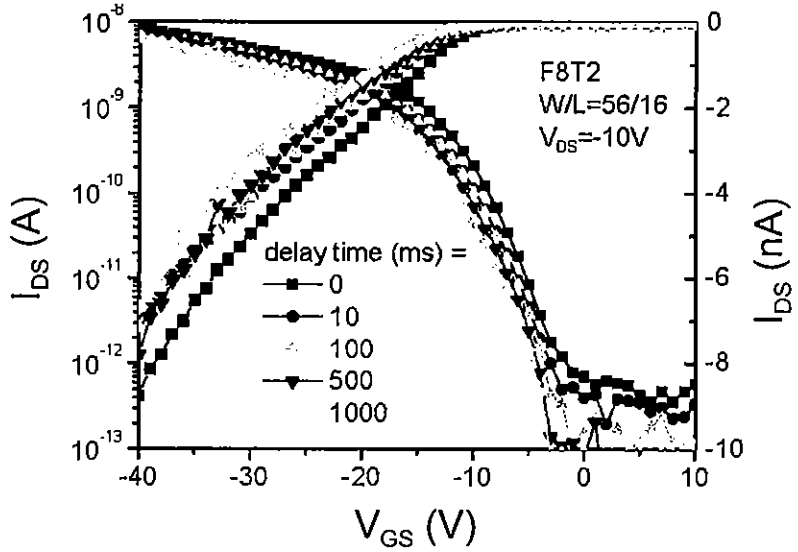

Figure 4.2.11. OFET transfer characteristics for different values of the delay time.

where ΔV_{GS} is the hysteresis width for a value of I_{DS} of approximately –7 nA. As seen in the inset of Figure 4.2.12, Q_{hyst} significantly depends on the maximum value of the gate voltage used during the measurement $V_{GS\ max}$, indicating that the charge trapping might be triggered by the accumulation of carriers (holes) under the effect of the gate voltage. When the gate voltage is swept from the 'on' to the 'off' state, the trapping of charges and the resulting shift of the transfer characteristic occur immediately at the beginning of the transfer characteristic measurement. When the gate voltage is swept from the 'off' to the 'on' state, the trapping of charges and the resulting shift of the transfer characteristic occur progressively as the magnitude of the gate voltage increases. This will result in a deformation of the transfer characteristic for large V_{GS}, as seen in Figure 4.2.12. The authors have therefore decided, in order to avoid any deformation of the measured transfer characteristics, to select gate voltage sweep from the 'on' to the 'off' state (in other words, from negative to positive voltages). To prevent any significant shift of the transfer characteristic, the magnitude of V_{GS} is limited to about –40 V. It is important to reduce this voltage to the lowest (negative) possible value.

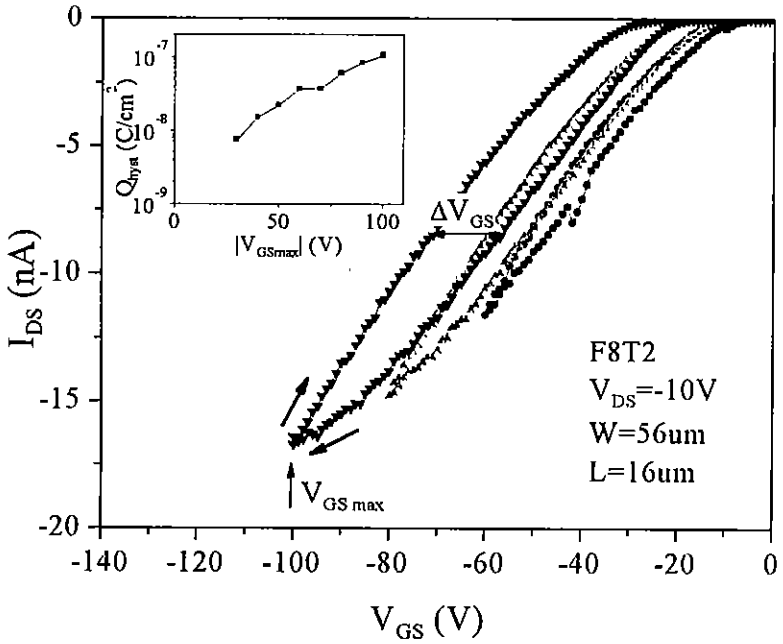

Figure 4.2.12. OFET transfer characteristics exhibiting a significant hysteresis phenomenon. The inset shows the estimated corresponding trapped charge as a function of the maximum gate voltage used in the OFET characteristic measurement.

There is no perfect measurement procedure for characterizing OFETs, but it is critical that the effect of measurement conditions is recognized and that consistent and repeatable procedures are used. The methods selected to obtain the OFET transfer characteristics presented in this chapter are summarized in Table 4.2.1. The authors believe that this choice provides a reasonable compromise in terms of measurement accuracy and device aging for the present suite of organic electronics technologies. When the OFET output characteristics are measured, the band bending and density of accumulated carriers in the channel do not change significantly during the drain voltage sweep. The measurement conditions are therefore less critical than for the acquisition of transfer characteristics. However, it is the belief of the authors that it is preferable to always use the same procedure for consistency. The parameters used for these measurements are also summarized in Table 4.2.1.

Table 4.2.1. Selected parameters for the measurement of the gate-planarized OFET transfer and output characteristics.

Transfer characteristics (linear regime)	Gate voltage	- *Initial value*	–40 V
		- *Final value*	+20 V
		- *Step*	+1 V
	Hold time		0 s
	Delay time		100 ms
	Source-Drain voltage (*kept constant during each characteristic measurement*)		–10 V, –5 V
Transfer characteristics (saturation regime)	Gate voltage	- *Initial value*	–40 V
		- *Final value*	0 V
		- *Step*	+1 V
	Hold time		0 s
	Delay time		100 ms
	Source-Drain voltage		= V_{GS}
Output characteristic	Drain voltage	- *Initial value*	0 V
		- *Final value*	–40 V
		- *Step*	–1 V
	Hold time		0 s
	Delay time		100 ms
	Gate voltage (*kept constant during each characteristic measurement*)		–40 V, –30 V, –20 V, –10 V

4.2.4.2 Normalization of Device Electrical Characteristics

In general, OFET transfer characteristics need to be normalized to accurately compare samples with different geometric parameters, different gate insulator characteristics, or measured under different conditions.[20] First, in order to take into account the geometrical dependence of the OFET characteristics and the effect of the source-drain voltage in linear regime, the

normalized OFET conductance, G, (in Siemens, S or Ω^{-1}) is used instead of the OFET drain current

$$G = \frac{I_{DS}}{V_{DS}} \cdot \frac{L}{W} \tag{4.2.37}$$

where V_{DS} is the source-drain voltage, and W and L are the TFT channel width and length, respectively.

Instead of the gate voltage, the electrical charge induced by the gate voltage at the organic semiconductor/gate insulator interface (in C/cm^2) is used

$$Q_{ind} = V_{GS} \times C_i \tag{4.2.38}$$

where C_i is the insulator capacitance per unit area. A linear plot of a typical normalized transfer characteristic $G - Q_{ind}$ is shown in Figure 4.2.13 (top). Alternatively, a plot of $G / C_i - V_{GS}$ can be used to investigate the OFET 'on' state in the linear regime, as is shown in Figure 4.2.13 (bottom). A normalized semilog plot of a typical normalized transfer characteristic $G - Q_{ind}$ is shown in Figure 4.2.14. These curves correspond to the non-normalized characteristics shown in Figure 4.2.8.

In the saturation regime, the normalized OFET current should be used, which is expressed by

$$I_{DS\,norm} = \frac{I_{DS}}{C_i W / 2L} \tag{4.2.39}$$

A typical normalized transfer curve $I_{DS\,norm} - V_{GS}$ in the saturation regime is shown in Figure 4.2.15. This corresponds to the non-normalized curve shown in Figure 4.2.8(top). A similar normalization procedure can be used for all devices shown in Figure 4.2.3 and Figure 4.2.4.

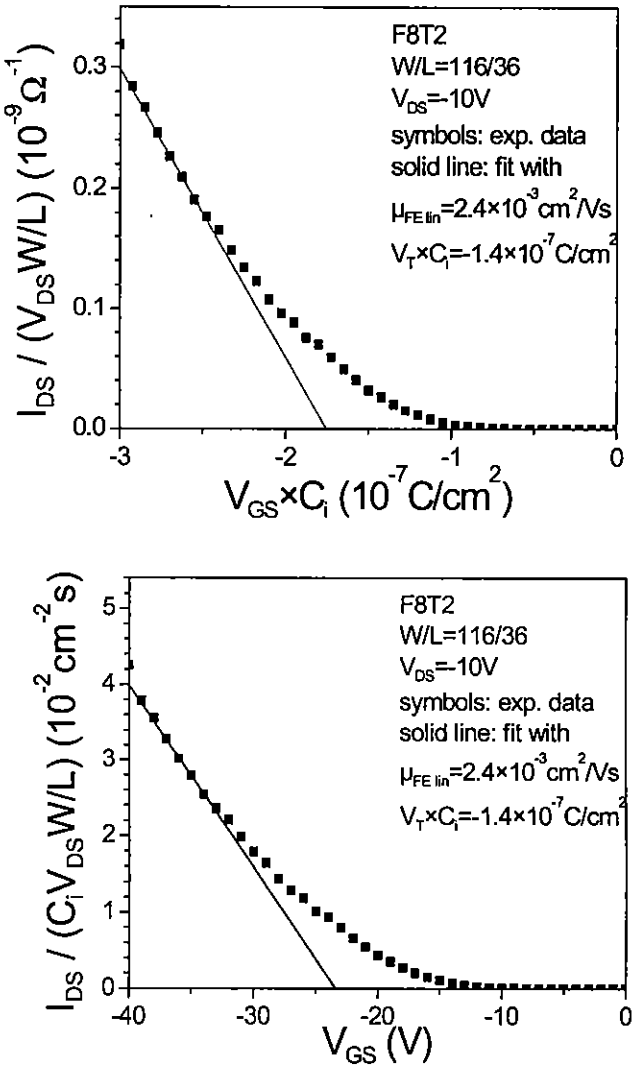

Figure 4.2.13. (*top*) Linear plots of typical OFET normalized transfer characteristics ($G - Q_{ind}$) in linear regime. (*bottom*) Alternative normalized transfer characteristics ($G / C_i - V_G$) in linear regime.

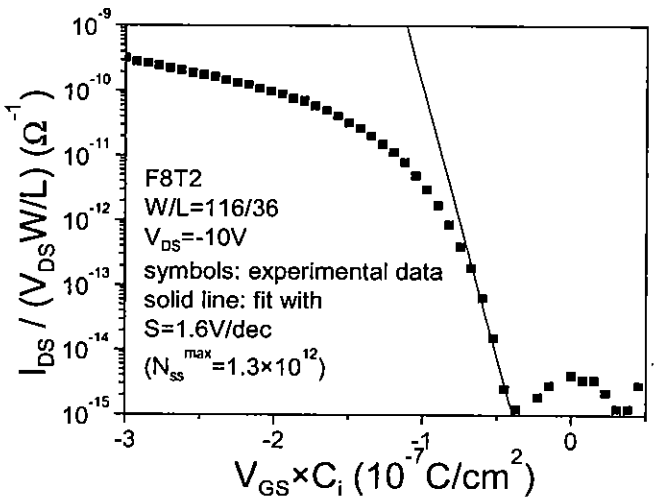

Figure 4.2.14. Semilog plot of typical OFET normalized transfer characteristics in linear regime.

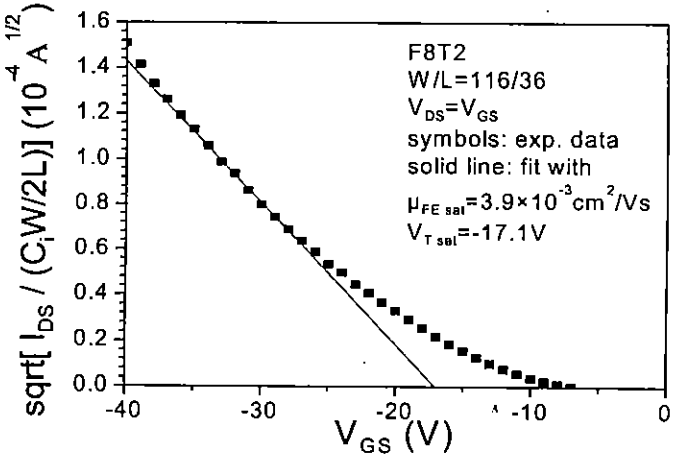

Figure 4.2.15. Typical OFET normalized transfer characteristic in saturation regime.

4.2.5 Extraction of Basic Device Electrical Parameters

4.2.5.1 Extraction Methods

4.2.5.1.1 Fitting Equations

In the linear regime, the OFET apparent field-effect mobility, $\mu_{FE\ lin}$, and threshold voltage, $V_{T\ lin}$, can be extracted using the following equation (for *p*-channel OFETs), from Equation 4.2.27[21]

$$I_{DS}^{lin} = -\mu_{FE\ lin} C_i \frac{W}{L}\left[\left(V_{GS} - V_{T\ lin}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (4.2.40)$$

where V_{DS} is the source-drain voltage, W and L are the OFET channel width and length, respectively, and C_i is the gate insulator capacitance per unit area. A linear plot of a typical transfer curve in the linear regime and the corresponding fit used to extract the field-effect mobility and threshold voltage is shown in Figure 4.2.13 (top).

For low source-drain voltages, *i.e.*, $V_{DS} \ll V_{GS} - V_T$, a simplified equation can be also used

$$I_{DS}^{lin} = -\mu_{FE\ lin} C_i \frac{W}{L}\left(V_{GS} - V_{T\ lin}\right)V_{DS} \qquad (4.2.41)$$

In the saturation regime, *i.e.*, typically for $V_{DS} = V_{GS}$, the OFET apparent field-effect mobility, $\mu_{FE\ sat}$, and threshold voltage, $V_{T\ sat}$, have been extracted using the following equation (for *p*-channel OFETs), from Equation 4.2.28[16]

$$I_{DS}^{sat} = -\mu_{FE\ sat} C_i \frac{W}{2L}\left(V_{GS} - V_{T\ sat}\right)^2 \qquad (4.2.42)$$

An example of an OFET transfer characteristic in the saturation regime and the corresponding fit used to extract the field-effect mobility and threshold voltage is shown in Figure 4.2.15.

The subthreshold swing, *S*, is extracted in the linear regime by fitting the experimental data to (*see* Equation 4.2.31)

$$I_{DS}^{subthreshold} \propto 10^{-\frac{V_{GS}}{S}} \quad (4.2.43)$$

A semilog plot of a typical OFET transfer curve in the linear regime and the corresponding fit used to extract the subthreshold swing is shown in Figure 4.2.14.

4.2.5.1.2 Fitting Range Selection

The most basic OFET characterization involves the extraction of the field-effect mobility, threshold voltage and subthreshold swing. To obtain meaningful and reproducible extracted electrical parameters, the range used for the curve fitting of the experimental curves must be selected carefully: it should ensure that devices with different geometries, gate insulator characteristics, or measurement conditions, are in comparable operating states. This does not necessarily occur for comparable gate voltage ranges.

In the linear regime, the OFET apparent field-effect mobility μ_{FE} and threshold voltage V_T are deduced from the fit of the experimental data to Equation 4.2.40 around a fixed value of the normalized drain current

$$I_{DS,norm}^{lin} = \frac{I_{DS}}{V_{DS} C_i W / L} \quad (4.2.44)$$

For the fits shown in Figure 4.2.13, the following value was used

$$I_{DS,norm}^{lin} = 0.03 \pm 50\% \quad (4.2.45)$$

In the saturation regime (typically for $V_{DS} = V_{GS}$), the OFET field-effect mobility and threshold voltage are calculated from the fit of the experimental data to Equation 4.2.42 around a fixed value of the normalized drain current

$$I_{DS,norm}^{sat} = \frac{I_{DS}}{C_i W / 2L} \quad (4.2.46)$$

For the fit shown in Figure 4.2.15, the following value was used

$$I_{DS,norm}^{sat} = 1 \pm 50\% \quad (4.2.47)$$

The subthreshold swing (S) is usually extracted from the OFET transfer characteristic in the subthreshold regime, by fitting the experimental data to Equation 4.2.43 around a fixed value of the normalized TFT drain current

$$I_{DS,norm}^{subthreshold} = \frac{I_{DS}}{V_{DS} W / L} \quad (4.2.48)$$

For the fit shown in Figure 4.2.14, the following value was used

$$I_{DS,norm}^{subthreshold} = 10^{-14} \pm 1/4 decade. \quad (4.2.49)$$

All extracted parameters for the authors' devices are summarized in Table 4.2.2.

Table 4.2.2. Electrical parameters extracted from transfer characteristics plotted in Figures 4.2.13-4.2.15

W / L	116 / 36
C_i (F/cm^2)	7.5×10^{-9}
$\mu_{FE\,lin}$ (cm^2/V·s)	2.4×10^{-3}
$V_{T\,lin}$ (V)	−18.7
$V_{T\,lin\,norm}$ (C/cm^2)	-1.4×10^{-7}
$\mu_{FE\,sat}$ (cm^2/V·s)	3.8×10^{-3}
$V_{T\,int}$ (V)	−22.8
$V_{T\,int\,norm}$ (C/cm^2)	-1.7×10^{-7}
$W \times R_{SD}$ at $V_{GS} - V_T = -10$ V (Ω·µm)	6.5×10^{10}
$\mu_{FE\,sat}$ (cm^2/V·s)	3.9×10^{-3}
$V_{T\,sat}$ (V)	−17
$V_{T\,sat\,norm}$ (C/cm^2)	-1.2×10^{-7}
S (V/dec)	1.6
N_{SS}^{max} (cm^{-2}·eV^{-1})	1.3×10^{12}
on/off current ratio (in linear regime)	10^5

4.2.5.2 Normalization of Device Electrical Parameters

To compare devices for which the gate insulators, geometrical dimensions, and/or measurement conditions are different, the OFET characteristics must be normalized. For the same reasons, some of the extracted electrical parameters also need to be normalized. Comparisons between different devices should be done using the normalized threshold voltages or equivalent charges

$$V_{T\,norm} = V_T \times C_i \tag{4.2.50}$$

in both the linear and saturation regimes. Additionally, the normalized subthreshold slope

$$S_{norm} = S \times C_i \tag{4.2.51}$$

should be used. Furthermore, the equivalent maximum density-of-states that can be present at the organic semiconductor/gate insulator interface[21,22] can be calculated from the S-value, based on Equation 4.2.31

$$N_{ss}^{\max} = \left(\frac{S \log(e)}{kT/q} - 1 \right) \frac{C_i}{q} \tag{4.2.52}$$

where q is the electron charge, k is the Boltzmann constant, and T is the temperature. All normalized electrical parameters extracted for our devices from Figures 4.2.13 to 4.2.15 are summarized in Table 4.2.2.

4.2.6 Advanced Device Electrical Characterization

4.2.6.1 Source/Drain Contacts

Although the electrical performances of many organic thin-film transistors are often limited by the low conductivity of the organic semiconductor, the source and drain (S/D) contacts play a predominant role in the device operation. It has clearly been found that these contacts could have a critical effect on device performance. In conventional inorganic TFTs or MOSFETs, the S/D electrodes form contacts to a highly doped semiconductor layer that ensures ohmic behavior and which do not limit carrier injection (*i.e.*, current flow into the device). Ideally in OFETs, the source and drain contacts should also behave as ohmic contacts for the majority carrier, *e.g.*, holes for *p*-type organic polymers. Such contacts will facilitate the injection or extraction of carriers from the contact electrodes. Most of the work done to date has employed either indium tin oxide (ITO) or gold (Au) as the source and drain contacts (ITO and Au have work functions of about 4.8 and 5.0 eV, respectively, against vacuum). The ionization potential of F8T2, which has been employed by the authors as an exemplary organic polymer semiconductor for the results shown in this chapter, is about 5.45 eV, with respect to vacuum.

In OFETs, recent carrier injection studies[23,24] have shown S/D contacts with non-ohmic behavior: it is now believed that the S/D contacts in OFETs form Schottky barriers to the channel region. Indeed, in Figure 4.2.16(top), the OFET drain current versus drain voltage curves measured when the device gate is floating (gate electrode not connected) are plotted, which clearly suggests Schottky S/D contacts. In Figure 4.2.16(bottom), the drain current of the OFET in accumulation follows a power-law dependence with the source-drain voltage, with an exponent always greater than 1. For the devices measured here, the exponent ranged between 1.2 and 2.1. These plots indicate that the S/D electrodes in these OFETs do not form perfectly ohmic contacts, but create Schottky barriers. However, the carriers (holes) can tunnel through the Schottky barrier present at the source when negative voltages are applied on both the device gate and drain, so that the depletion width becomes sufficiently narrow. This process is called *hole injection* into the polymer layer (and is equivalent to *electron extraction*) from the source electrode. At the same time, *hole extraction* is expected from the device channel (or *electron injection*) taking place at the drain electrode. To maximize hole extraction at the drain electrode, it is important that the drain metal work function be very close to that of the ionization potential of the polymer.

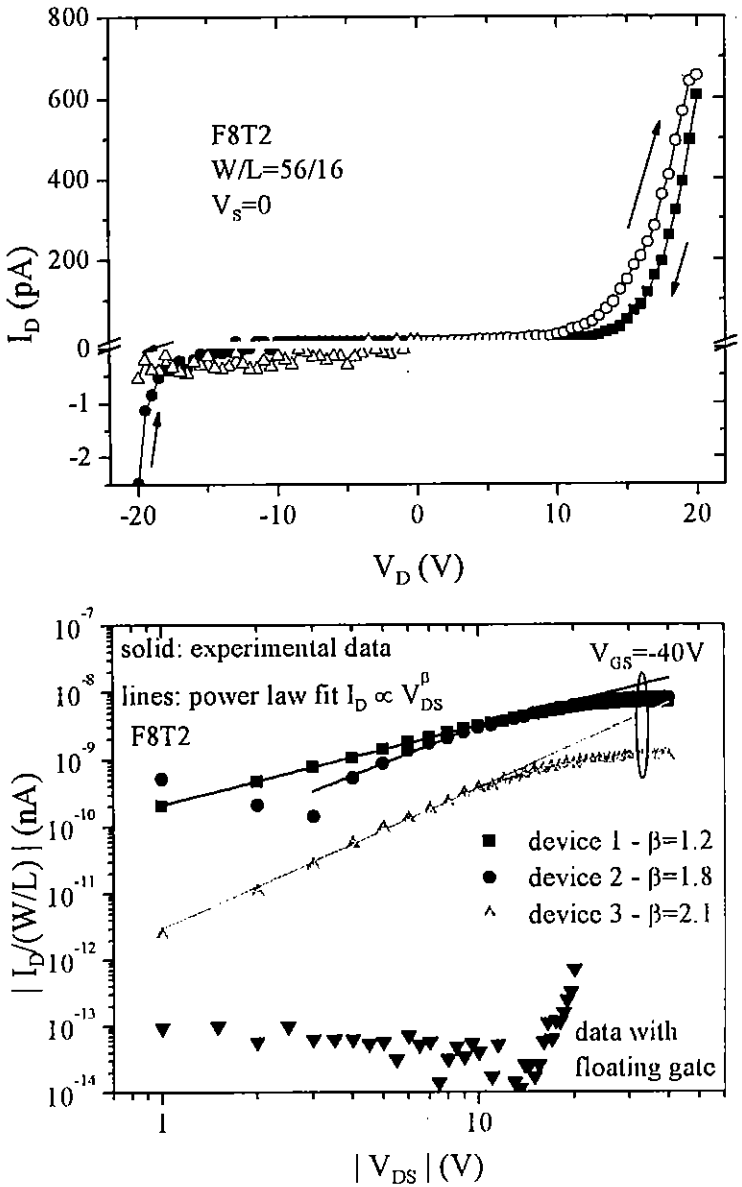

Figure 4.2.16. (*top*) Drain current versus drain voltage characteristics measured with the device gate floating. (*bottom*) Curves measured for different OFETs in accumulation regime.

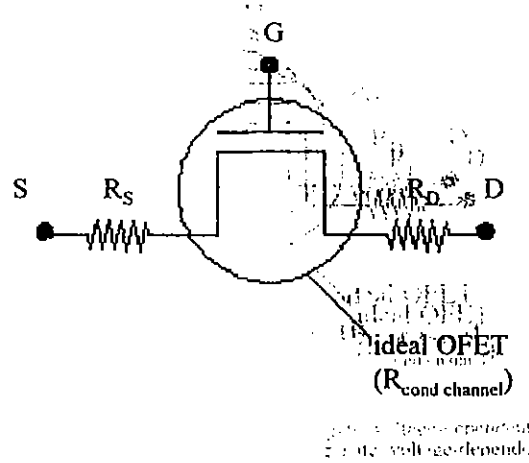

Figure 4.2.17: Equivalent model of the OFET using gate voltage-dependent S/D series resistances.

The quantitative role of the source/drain (S/D) contacts can be approximated using a method developed for amorphous semiconductor thin-film transistors with ohmic contacts: the *transverse line method* (TLM).[25,26,27] This method models the S/D contact and access regions by gate voltage-dependent series resistances

$$R_{S/D} = R_S + R_D \tag{4.2.53}$$

as illustrated in Figure 4.2.17. In OFETs with non-ohmic contacts, the values obtained for these source/drain resistances will also be dependent on the S/D voltage. The TLM analysis is done when the TFT is in the linear regime. In most OFETs, significant parasitic S/D series resistances are expected, resulting from the S/D contact resistances. In addition, significant contributions of the access region resistances between the S/D contacts and the conduction channel (*access resistance*) are expected in staggered OFET structures.[25] In the OFETs studied here, it is expected that the conduction channel is created in the same plane as the source and drain electrode. This should drastically reduce the access region resistances. However, significant contact resistances can nevertheless degrade OFET performance, especially in the linear regime.

A series of OFETs with different channel lengths was measured and the on-resistances (R_{ON}) are plotted as a function of the channel length in the

linear regime, as shown in Figure 4.2.18. The total S/D series resistance $R_{S/D}$ is extracted for each gate voltage from the y-intercept of the curves, as indicated by the following equation[25]

$$WR_{ON} = \frac{W_{DS}}{I_{DS}} = WR_{S/D} + \frac{1}{\mu_{FE\,\mathrm{int}} C_i \left(V_{GS} - V_{T\,\mathrm{int}}\right)} \times L \qquad (4.2.54)$$

where $\mu_{FE\ int}$ and $V_{T\ int}$ are the intrinsic field-effect mobility and threshold voltage, i.e. representative of the conduction channel, or ideal OFET only. The total S/D series resistance $R_{S/D}$ is gate voltage dependent, as can be seen in Figure 4.2.18 (bottom). The data show a total S/D series resistance value of about 0.5 GΩ for $(V_{GS} - V_T)$ around −10 V. The equivalent conduction channel resistance for a channel length of 16 μm is also shown in Figure 4.2.18 (bottom). This resistance was derived from the following equation

$$W \times R_{cond\ channel} = \frac{L}{\mu_{FE\,\mathrm{int}} C_i \left(V_{GS} - V_{T\,\mathrm{int}}\right)} \qquad (4.2.55)$$

It is observed that, under most gate voltage conditions, the S/D series resistances are comparable to the conduction channel resistance and should consequently have a significant effect on the device electrical performances. In addition, from the slope of the $W \times R_{ON} - L$ curves at different values of V_{GS}, the device intrinsic field-effect mobility ($\mu_{FE\ int}$) and threshold voltage ($V_{T\ int}$) can be calculated

$$\frac{1}{slope} = \mu_{FE\,\mathrm{int}} C_i \left(V_{GS} - V_{T\,\mathrm{int}}\right) \qquad (4.2.56)$$

The variations of 1/*slope* with the applied gate voltage are shown in Figure 4.2.19, together with a linear fit. This allows for the calculation of $\mu_{FE\ int}$ and $V_{T\ int}$ from the slope and x-intercept of the linear fit. The data shown in Figure 4.2.19 yield $\mu_{FE\ int} = 3.8 \times 10^{-3}\mathrm{cm}^2/\mathrm{V{\cdot}s}$ and $V_{T\ int} = -23$ V. F8T2 OFETs tend to be normally off with a negative threshold voltage. This can reflect the density of charge carriers trapped in the F8T2 organic semiconductor that needs to be filled before an accumulation layer can be formed.

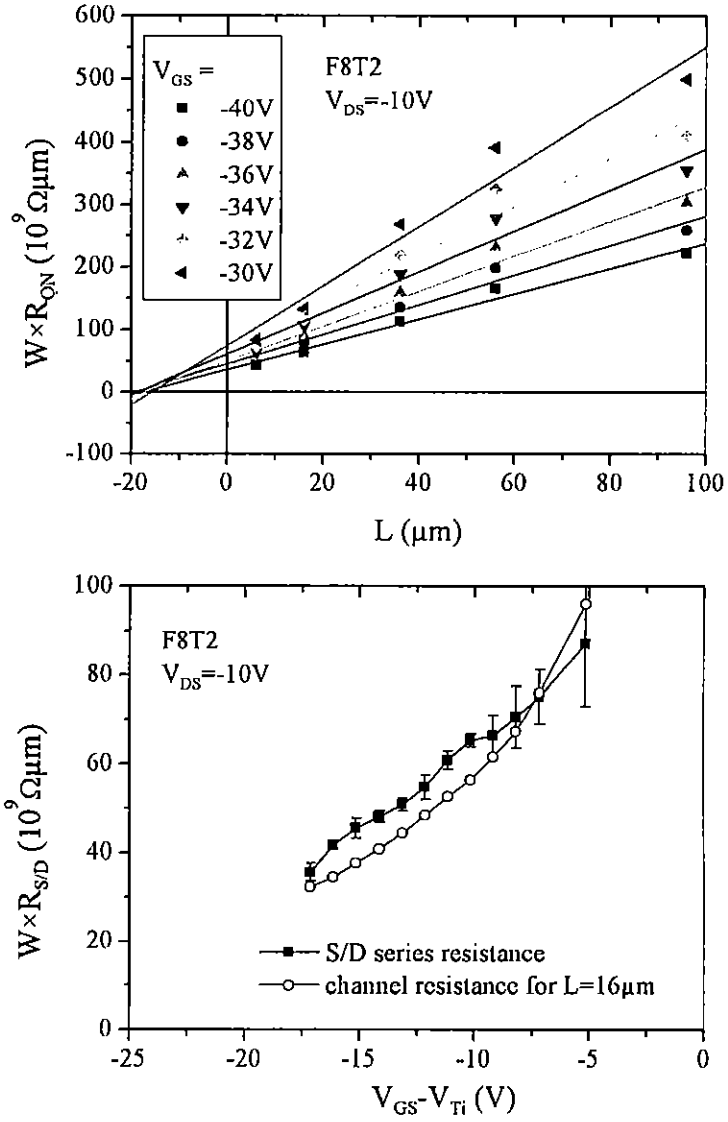

Figure 4.2.18. (top) Total on-resistance measured on a series of OFETs. *(bottom)* Variations of the extracted S/D series resistance with the gate voltage above threshold.

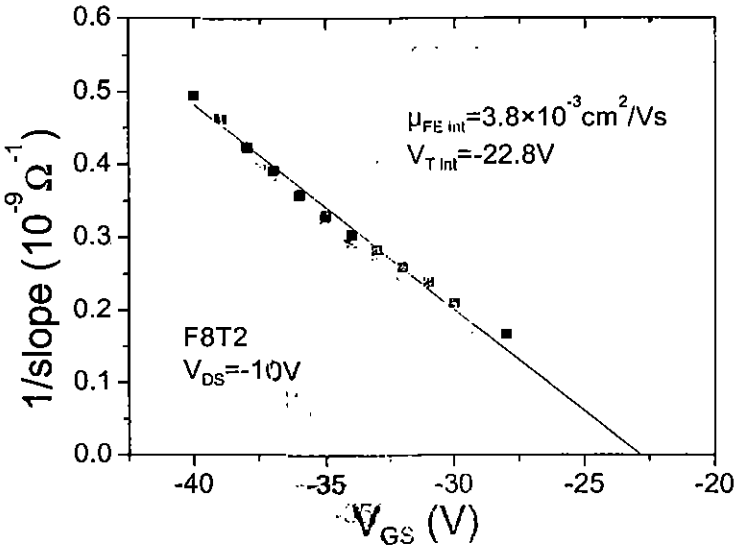

Figure 4.2.19. Curves used for the extraction of the OFET intrinsic field-effect mobility and threshold voltage values.

It can be observed from Table 4.2.2 that the device apparent field-effect mobility is lower than the intrinsic field-effect mobility. This effect is more significant for short-channel devices, since the channel resistance decreases with decreasing channel length, but the S/D series resistances are channel length-independent. This can be seen in Figure 4.2.20 where the apparent field-effect mobility as a function of the device channel length has been plotted. Therefore, to evaluate the device intrinsic electrical properties, an OFET with the largest possible channel length should be used.

The effect of the series resistances can also be partially represented as an increase of the apparent channel: the total OFET on-resistance is[25]

$$R_{ON} = \frac{V_{DS}}{I_{DS}} = 2R_{S/D} + \frac{L}{\mu_{FE}C_i W(V_{GS} - V_{Ti})} = 2R_0 + \frac{L + 2\Delta L}{\mu_{FE}C_i W(V_{GS} - V_{Ti})} \quad (4.2.57)$$

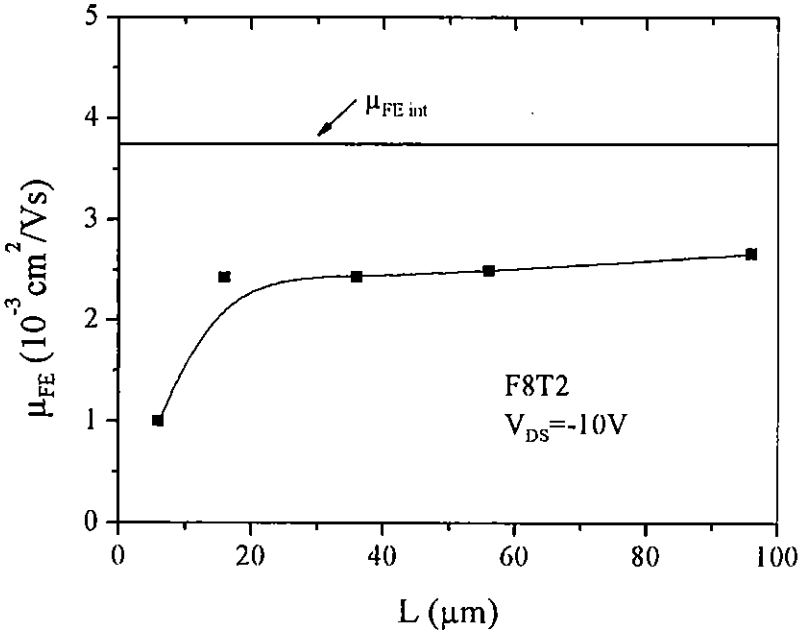

Figure 4.2.20. Extracted device (apparent) field effect mobility as a function of the device channel length. Also shown on the figure is the intrinsic field-effect mobility extracted from Figure 4.2.19.

where ΔL and R_0 are independent of the gate voltage. The values of ΔL and R_0 are extracted from the R_{ON} versus L curves: all the $R_{ON} \sim L$ curves have a common cross-point located slightly away from the y-axis,[20,25,28] whose coordinates are ($x = -2\Delta L$, $y = 2R_0$). This can be seen in Figure 4.2.18, although the extraction of ΔL and R_0 may be affected by a significant uncertainty. From Figure 4.2.18, the values $\Delta L \sim 5 - 8$ μm and $R_0 \sim 7 \times 10^7 - 3 \times 10^8$ Ω are obtained. ΔL is associated with the effective channel length, which is longer than the physical channel length. In other words, the current path extends beyond the source/drain contact edges. ΔL depends significantly on the source and drain contact resistances, and $2R_0$ represents the limit of the source and drain series resistance, $R_{S/D}$, for a very high gate voltage.[25]

4.2.6.2 Channel Material and Device Field-Effect Mobility

It has often been observed that the OFET transfer characteristic at low drain voltage does not always exhibit perfectly linear behavior, as shown in Figure 4.2.21 and as reported by other groups.[18,29] This deviation from the ideal c-Si MOSFET behavior has also been observed in a-Si:H TFTs,[9,10,30,31] where it has been associated with dispersive transport in a-Si:H.[31,32] In general, in amorphous and other low-mobility solids (including organic polymers), the movement of an injected pulse of charges in a steady electrical field produces completely smeared-out drift of the pulse. This is due to very heavy trapping of charges and their very slow release under thermal excitation. In such a case, it is very difficult to define a transit time of any particular charge. Instead, the time dependence of the current is of the power law type

$$I(t) \propto t^{-s}, \quad (0 < s < 2) \tag{4.2.58}$$

and this type of behavior is know as dispersive transport.

To accommodate this type of carrier transport, the device model was modified to include an additional parameter, γ, representative of the non-linearity of the device transfer characteristic at low V_{DS}

$$I_{DS}^{lin} = -\mu_{FElin0} C_i \frac{W}{L} (V_{GS} - V_T)^{\gamma} V_{DS} \tag{4.2.59}$$

where μ_{FElin0} is a fitting parameter associated with the device field-effect mobility in linear regime. It is noted that the unit of μ_{FElin0} is not $cm^2/V \cdot s$ but $cm^2/V^{\gamma} \cdot s$.

The physical significance of γ in a-Si:H has often been expressed by

$$\gamma = 2\frac{T_0}{T} - 1 \tag{4.2.60}$$

where T_0 is the characteristic temperature of the inorganic semiconductor density-of-states distribution around the position of the Fermi level.[18,30] The equation is valid for $T < T_0$. In a-Si:H TFTs (n-channel devices), T_0 is the characteristic temperature (slope) of the conduction band tail. The non-ideal situation of $\gamma > 1$ is associated with a high density of conduction band tail states, which can usually be attributed to variations of the Si–Si bond angles

and distances in the amorphous semiconductor. It has been previously demonstrated for a-Si:H TFTs[33] that γ can be significantly under-estimated in cases of non-negligible source and drain series resistances. Indeed, $\gamma = 1$ can be observed for a TFT with both a high density of conduction band tail states and high source/drain series resistances.

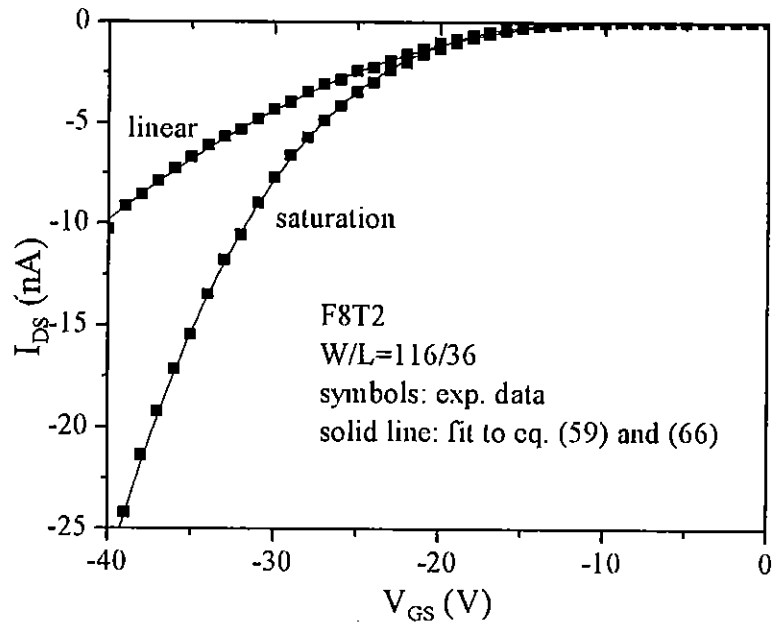

Figure 4.2.21. OFET transfer characteristics. Symbols represent experimental data; solid lines show fit to Equations 4.2.59 and 4.2.66 (*see text*).

Equation 4.2.59 can also be used to fit the OFET experimental data in the linear regime over a wide gate voltage range. In Figure 4.2.21 the OFET drain current in the linear regime and the fit to Equation 4.2.59 using the parameters summarized in Table 4.2.3 are plotted. The physical significance of γ-values larger than one in organic devices has not yet been fully explained. However, the authors believe that, following amorphous semiconductor theory, it can also be associated with an energy-dependent high density of states around the Fermi level position caused by residual disorder in the locally self-organized polymer film. As the carrier

concentration increases, localized defects states are filled and the Fermi level approaches a region of the density of states of more extended electronic states with higher mobilities. It should be noted that, when the OFET parameter extraction is performed using Equation 4.2.59, the unit of μ_{FElin0} is not $cm^2/V{\cdot}s$ but $cm^2/V^{\gamma}{\cdot}s$. Equation 4.2.59 is therefore used only to extract γ. The values of field-effect mobility and threshold voltage presented elsewhere in this chapter have been extracted using Equation 4.2.40), *i.e.*, assuming $\gamma = 1$.

Table 4.2.3. Fitting parameters used for the transfer characteristics shown in Figure 4.2.21.

	Linear regime	*Saturation regime*
W/L	116/36	116/36
C_i (F/cm^2)	7.5×10^{-9}	7.5×10^{-9}
μ_{FElin0} and μ_{FEsat0} ($A/V^{\gamma+1}$)	7×10^{-12}	1×10^{-13}
μ_{FElin} and μ_{FEsat} ($cm^2/V{\cdot}s$) for $V_{GS}-V_T=-25$ V	1×10^{-3}	2×10^{-3}
γ	2.1	2.5
T_0 (K)	465	525
V_{Tlin} and V_{Tsat} (V)	−9	−6

Alternatively, it is also possible to rewrite Equation 4.2.59 as

$$I_{DS}^{lin} = -\mu_{FElin0}(V_{GS}-V_T)^{\gamma-1} C_i \frac{W}{L}(V_{GS}-V_T)V_{DS} \qquad (4.2.61)$$

which becomes

$$I_{DS}^{lin} = -\mu_{FElin}(V_{GS}) C_i \frac{W}{L}(V_{GS}-V_T)V_{DS} \qquad (4.2.62)$$

with:

$$\mu_{FElin}(V_{GS}) = \mu_{FElin0}(V_{GS}-V_T)^{\gamma-1} \qquad (4.2.63)$$

The gate voltage dependence of the OFET field-effect mobility has been connected to the characteristic temperature of the semiconductor density-of-states distribution around the position of the Fermi level.[18,34] Equation 4.2.62 is very similar to the standard MOSFET equation in the linear regime but contains the gate voltage dependence of the field-effect mobility. It is therefore incorrect to extract μ_{FElin} as it is done for the MOSFET because of the gate voltage dependence of the device field-effect mobility. Indeed, as it has been pointed out previously,[35] doing so would overestimate the device field-effect mobility by a factor γ, as indicated by the equations below. Using the standard MOSFET Equation 4.2.41, the field-effect mobility is sometimes extracted using the following equation

$$\mu_{calc}^{lin} = \frac{1}{V_{DS} C_i W/L}\frac{dI_{DS}^{lin}}{dV_{GS}} \qquad (4.2.64)$$

However, if the field-effect mobility is gate voltage dependent, Equation 4.2.41 has to be replaced by Equation 4.2.59 or 4.2.62. In such a case, the field-effect mobility expression becomes

$$\begin{aligned}\mu_{calc}^{lin} &= \gamma\mu_{FElin0}(V_{GS}-V_T)^{\gamma-1} \\ &= \gamma\mu_{FElin}(V_{GS})\end{aligned} \qquad (4.2.65)$$

This equation clearly indicates that the OFET field-effect mobility can be overestimated by a factor γ if the parameter extraction is not done properly. These observations are illustrated by Figure 4.2.22 (top), where the device field-effect mobility has been plotted in the linear regime and extracted by the different methods below:

- Curve 1: Conventional value extracted from experimental data using the standard MOSFET Equation 4.2.41;
- Curve 2: Values calculated using Equation 4.2.63 and fitting parameters from Table 4.2.3;
- Curve 3: Values extracted from experimental data using Equation 4.2.64, *i.e.*, μ_{calc}^{lin}

- Curve 4: Values extracted from experimental data using Equation 4.2.64 and taking into account γ, *i.e.*, μ_{calc}^{lin}/γ.

It can be seen that Curves 1 and 3 show significantly overestimated values of the field-effect mobility, especially at moderate gate voltages. On the other hand, Curves 2 and 4 are very similar. It is therefore critical to keep this in mind when the conventional extraction is applied to OFETs. It can also be concluded that the methods used to extract Curves 2 and 4 are the most appropriate for OFETs.

In the saturation regime, the MOSFET equation and corresponding extraction method should be modified as follows

$$I_{DS}^{sat} = -\mu_{FEsat0} C_i \frac{W}{(\gamma+1)L}(V_{GS} - V_{Tsat})^{\gamma+1} \quad (4.2.66)$$

Figure 4.2.21 also shows the OFET drain current in saturation regime and the fit to Equation 4.2.66 using the parameters summarized in Table 4.2.3.

Following the same method as in the linear regime, it is also possible to rewrite Equation 4.2.66 as

$$I_{DS}^{sat} = -\mu_{FEsat0}(V_{GS} - V_{Tsat})^{\gamma-1} C_i \frac{W}{(\gamma+1)L}(V_{GS} - V_{T\,sat})^2 \quad (4.2.67)$$

or

$$I_{DS}^{sat} = -\mu_{FEsat}(V_{GS}) C_i \frac{W}{(\gamma+1)L}(V_{GS} - V_{T\,sat})^2 \quad (4.2.68)$$

with

$$\mu_{FEsat}(V_{GS}) = \mu_{FEsat0}(V_{GS} - V_{Tsat})^{\gamma-1} \quad (4.2.69)$$

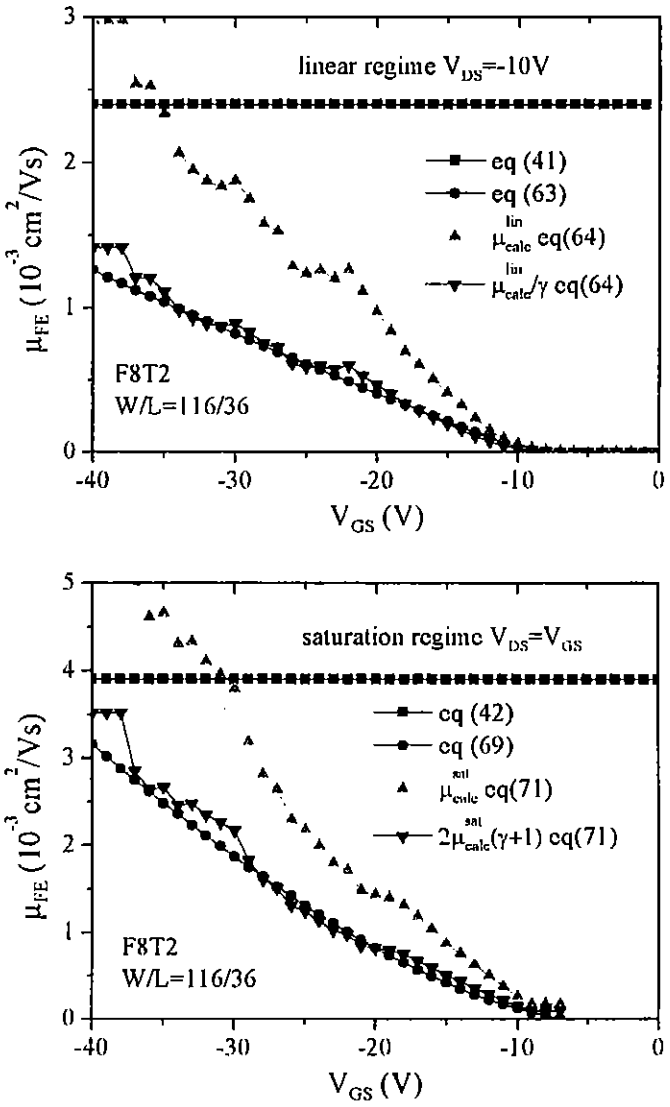

Figure 4.2.22. (top) OFET field-effect mobility of the same device as used in Figure 4.2.21, in linear regime. *(bottom)* OFET field-effect mobility of the same device as used in Figure 4.2.21, in saturation regime. The extractions methods are described in more details in the text.

Equation 4.2.69 is very similar to the standard MOSFET equation in the saturation regime but contains the gate voltage dependence of the field-effect mobility. It is therefore incorrect to extract μ_{FEsat} as it is done for the MOSFET because of the gate voltage dependence of the device field-effect mobility. Indeed, doing so would overestimate the device field-effect mobility by a factor $(\gamma + 1)/2$, as indicated by the equations below. It is possible to write the standard MOSFET Equation 4.2.42 as follows

$$\sqrt{\left|I_{DS}^{sat}\right|} = \sqrt{\mu_{FE\,sat} C_i \frac{W}{2L}} \left(V_{GS} - V_{T\,sat}\right) \tag{4.2.70}$$

Consequently, the field-effect mobility is sometimes extracted using the following equation

$$\mu_{calc}^{sat} = \frac{1}{C_i W/2L} \left(\frac{d\sqrt{\left|I_{DS}^{sat}\right|}}{dV_{GS}} \right)^2 \tag{4.2.71}$$

However, if the field-effect mobility is gate voltage dependent, Equation 4.2.42 has to be replaced by Equation 4.2.66 or 4.2.69. In such a case, the field-effect mobility expression becomes

$$\begin{aligned} \mu_{calc}^{sat} &= \left(\frac{\gamma+1}{2}\right) \mu_{FEsat0} \left(V_{GS} - V_T\right)^{\gamma-1} \\ &= \left(\frac{\gamma+1}{2}\right) \mu_{FEsat} \left(V_{GS}\right) \end{aligned} \tag{4.2.72}$$

In Figure 4.2.22 (bottom), the values of the extracted device field-effect mobility in saturation regime are shown using the following methods:

- Curve 1: Conventional value extracted from experimental data using the standard MOSFET Equation 4.2.42;
- Curve 2: Values calculated using Equation 4.2.69 and fitting parameters from Table 4.2.3;

- Curve 3: Values extracted from experimental data using Equation 4.2.71, *i.e.*, μ_{calc}^{sat};
- Curve 4: Values extracted from experimental data using Equation 4.2.71 and taking into account γ, *i.e.*, $(2/\gamma+1)\mu_{calc}^{sat}$.

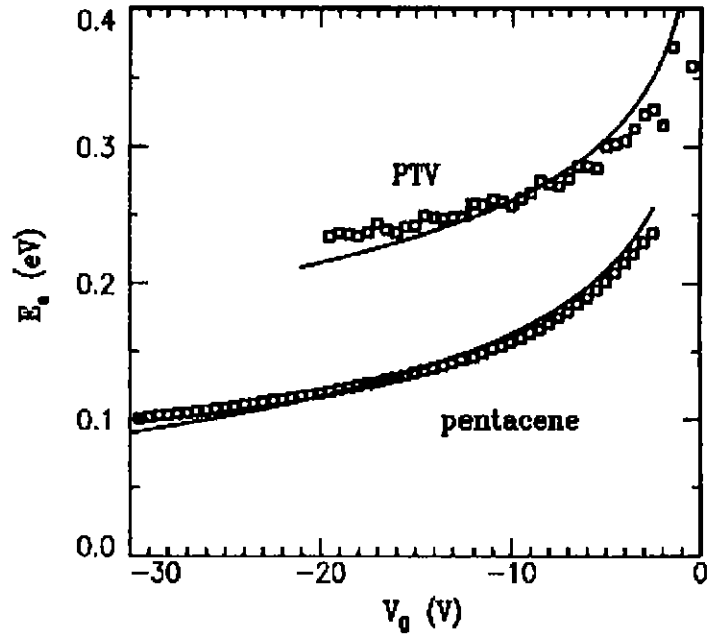

Figure 4.2.23. Gate voltage dependence of the OFET field-effect mobility activation energy. (From Reference 34, copyright © 1998 by the American Physical Society).

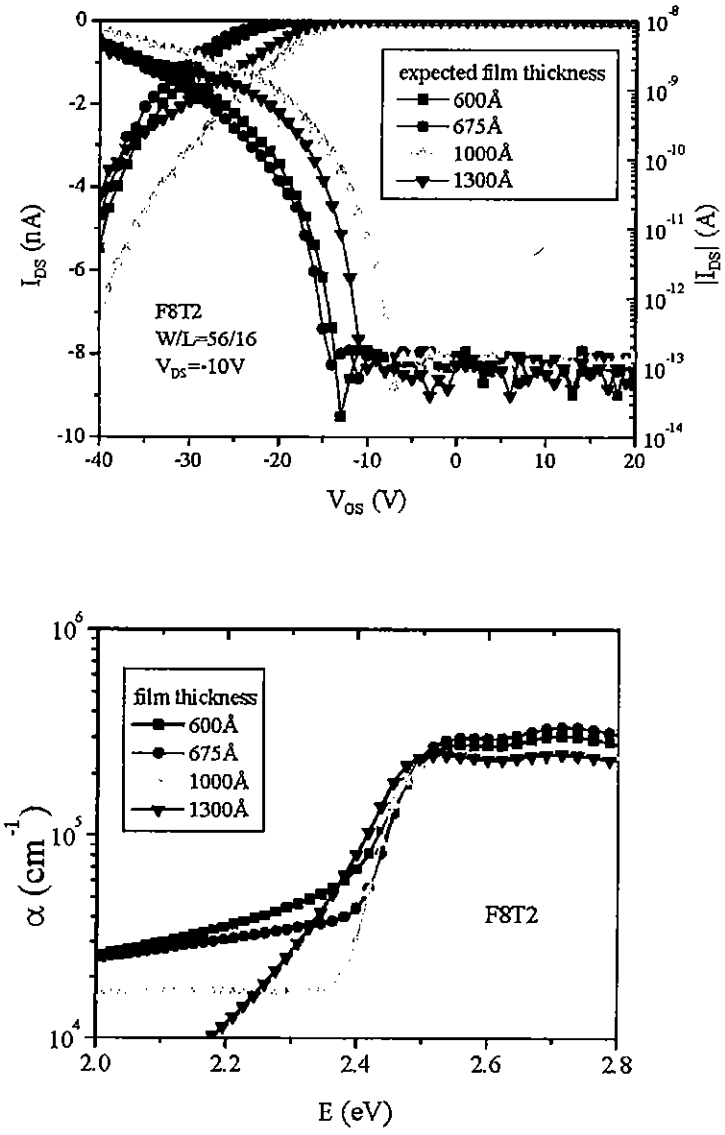

Figure 4.2.24. (top) OFET transfer characteristics for devices with different organic polymer film thicknesses. *(bottom)* Optical transmission curves for film with the same thicknesses as *(top)*.

It can be seen in Figure 4.2.22 (bottom) that Curves 1 and 3 show significantly overestimated values of the field-effect mobility in the saturation regime, especially at moderate gate voltages. The difference is less significant for large values of the gate voltage. On the other hand, Curves 2 and 4 are very similar. It is therefore critical to keep this in mind when the conventional extraction is applied to OFETs. It can also be concluded that the methods used to extract Curves 2 and 4 are the most appropriate for OFETs.

In metal and conventional semiconductors, charge transport is mainly limited by the scattering of the carriers on phonons (*i.e.*, scattering associated with the vibrations of the atoms due to heat energy) and occurs via delocalized states in the conduction and/or valence bands. Electrons (or holes) transport in these bands is similar to free carrier transport, characterized by an *effective mass*. The effective mass is a mathematical term used for convenience. It is used in place of the physical mass of an electron or hole. This term accounts for velocity and other characteristics of the particle, which make the mass of a particle appear to be different from its physical mass. Conduction is limited by the concentration of available empty states. When an increased gate voltage is applied, the Fermi level position becomes closer to the band edge and the density of available states increases significantly, resulting in higher apparent carrier mobility. The band theory has so far been successful in describing transport in crystalline inorganic materials. It also has been used with success in amorphous and polycrystalline inorganic semiconductors. However, in organic materials, the typical mean free path of carriers is very small (essentially, the electrons and holes cannot move very far on their own) and the charge transport is phonon-assisted (*i.e.*, the conductivity increases with temperature), and can occur via localized states. These localized states present in conjugated organic materials are associated with polarons, which result from the deformation of the conjugated chains due to the presence of a charge. The charge is self-trapped by this deformation and results in the creation of localized states. The existence of such states in doped conjugated polymers and oligomers has been confirmed by UV-visible spectroscopy. The role of phonons in the carrier transport mechanism can also be related to the temperature dependence of charge transport in organic materials, as discussed below.

The temperature dependence of the OFET field-effect mobility can be analyzed to provide significant information on the conduction mechanism responsible for the OFET operation.[36] However, the field-effect mobility also depends on the OFET device structure and should take into account the temperature dependence of parasitic effects, such as source and drain contacts and interface-specific phenomena. This is because in organic

materials charge transport occurs by tunneling/hopping through localized states. The transport process can be aided by phonons (*i.e.*, heat) and therefore be thermally activated. Hence, it is expected that the carrier mobility increases with increasing temperature. The band theory as used in inorganic semiconductors also predicts a temperature-activated behavior of the field-effect mobility associated with the distribution of localized states in the semiconductor gap and multiple trapping and release of carriers. Indeed, many authors have reported a significant temperature dependence of OFET electrical performances. More precisely, a temperature activated behavior of the device field-effect mobility has been reported.[37,38,39,40] This has been explained by both band theory[41] and the variable range hopping model.[34] However, other behaviors have also been observed, in which the temperature dependence of the field-effect mobility was not monotonic (*i.e.*, did not consistently increase or decrease with change in temperature).[42] In addition, different regimes occur for different temperature ranges, especially for very low temperatures, typically below 50 K (–223 °C).[41,43] A significant gate voltage dependence of the activation energy was observed for both a-Si:H TFTs and OFETs. It is believed that the gate voltage dependence of the activation energy can be related to the gate voltage dependence of the field-effect mobility described above. More precisely, Figure 4.2.23 shows that the activation energy decreases with increasing negative gate voltage. This is consistent with band theory, according to which the activation energy is associated with the energy difference between the Fermi level and band tail edge. Similar observations were made for the temperature activation of the drain current in a-Si:H TFTs. Based on these and other experimental results, the authors believe that the modified band theory developed for amorphous inorganic semiconductors can be applied to organic polymer semiconductors.

Initial investigations of the effect of the organic semiconductor film thickness have not shown any significant difference between OFETs fabricated with film thicknesses ranging from 600 to 1300 Å, as indicated by Figure 4.2.24. This could be explained by the bottom-contact device structure used for these experiments: the channel is created at the bottom of the film and the current path does not go through the whole thickness of the organic semiconductor film. In addition, it is possible that the quality of this portion of the film does not depend on the film thickness for the range presented here.

4.2.6.3 Gate Thin-Film Insulators

The gate dielectric layer is another critical material in organic thin-film transistors, since the electrical characteristics and the density of carriers

in the conducting channel of OFETs are in part controlled by the gate insulator capacitance, *see* Equations 4.2.32 and 4.2.33. The drain current of the OFET is linearly proportional to the capacitance of the dielectric material. Therefore, ultra-thin, pinhole-free thin-film dielectrics having high dielectric constants are very desirable for producing high-performance (high drain current values) OFETs that can operate at low gate voltages. In addition to affecting OFET on-current, the gate dielectric can also influence the OFET off-current (gate leakage current), the threshold voltage (fixed and trapped charges), the subthreshold slope (interface charges), the transfer and output characteristics hysteresis (trapped charges), and the conduction mechanism (trap-assisted hopping). The gate dielectric should act as a potential barrier to both electrons and holes. It needs to inhibit conduction resulting from emission of carriers into their bands, *i.e.*, the bandgap of the gate insulator material should be sufficiently large to ensure low gate leakage current. The gate insulator layer should also be thermodynamically stable in contact with the organic semiconductor and should have a low density of active defects at the interface with the organic semiconductor. Finally, it is desirable that the gate dielectric surface is as smooth as possible and material is electrically very stable (high breakdown voltage and very low leakage current). The flatness of the gate dielectric surface can enhance the ordering of the organic semiconductor molecules near the interface, which can be achieved through the planarization of the gate metal electrode.

A high dielectric constant of the gate insulator is very desirable for low-voltage operation of the OFET, but this type of material can introduce high polarization at or near the gate insulator/organic semiconductor interface.[44] As discussed below, a high polarization can result in an increase of the carrier localization within the conduction channel, and therefore lower carrier mobility. Consequently, a compromise must be reached between low gate voltage operation and high electrical performance.

In principle, both inorganic and organic gate dielectric materials can be used for OFETs. However, the fabrication of the inorganic or organic ultra-thin, pinhole-free films at low temperatures over large areas can be challenging. It would therefore probably be more practical to replace a single gate insulator layer having a film thickness under 100 nm by a multilayer gate dielectric having a total thickness around 200 to 400 nm.

The common inorganic insulators used in microelectronics include hydrogenated amorphous silicon oxide and hydrogenated amorphous silicon nitride deposited at low temperature by plasma-enhanced chemical vapor deposition (PECVD), titanium (TiO_2) and aluminum (Al_2O_3) oxides deposited by sputtering, tantalum (Ta_2O_5) and aluminum oxides prepared by anodization, and metal oxide films of barium zirconate titanate (BZT) or barium strontium titanate (BST) fabricated by sputtering. Among these

materials, TiO_2, in combination with other materials, shows promise for OFETs. Spin-on polymers, such as polyimides (PI), polymethylmethacrylate (PMMA), benzocyclobutene (BCB), polyhydroxystyrene, polyvinylalcohol (PVA), cyanoethylpullualan,[45] and silsesquioxanes[46] can also be used as gate dielectric materials. Uniform, mechanically flexible films can be deposited over a large area by spin-coating, printing, or dip-coating methods. These films also have low surface energy, which is desirable for OFETs. However, they have the disadvantage of relatively low dielectric constants, which could lead to high-voltage device operation. To reduce the OFET operation voltage (to achieve high-gate insulator capacitance), ultra-thin, pinhole-free organic dielectric films would be required, which might technologically be very difficult to realize in a single-layer configuration. However, these materials can be combined with other inorganic gate insulators with high dielectric constants in order to provide attractive multilayer gate insulators.

Recently it has been reported that OFETs based on polytriarylamine (PTAA) with good electrical performance (high field-effect mobility) can be fabricated with a low-permeability (*i.e.*, low dielectric constant) fluoropolymer, polyperfluoroethylene-co-butenyl vinyl ether ($\varepsilon \sim 2.1$) (PTAA2).[44] In this same work it was also shown that field-effect mobility increases with decreasing dielectric constant of gate dielectric layer. This increase was not due to morphology or special ordering, but to the reduced energetic disorder at the interface. It was argued that the energetic disorder in organic polymers is increased at the gate insulator interface when the insulator is more polar (higher dielectric constant). The increase of the density-of-states broadening with the increase of the dielectric constant of the gate insulator will lead to more band tail states and enhanced localization, *e.g.*, carrier localization is likely to be enhanced by dipole disorder. Therefore, low-polarity interfaces could be beneficial to OFETs, as discussed in more detail below. In general, the authors believe that a main disadvantage of low dielectric constant gate materials is that the operating voltage required will be high and device electrical stability will be poor.

It is also possible to replace a gate dielectric having low dielectric constant with an insulator having a similar thickness but a much higher dielectric constant. In this case, an accumulated carrier concentration similar to a low dielectric constant gate insulator could be attained at much lower gate voltage values. Hence, a lower electrical field will be achieved, with all other device parameters being similar.[47] Therefore, in a correctly engineered gate dielectric layer, high fields are not required to achieve high field-effect mobility when gate dielectrics with large dielectric constants are used. Indeed, it was shown that the gate voltage dependence of field-effect mobility in OFETs is due to the higher concentration of holes accumulated

in the channel. In addition, field-effect mobility variation with surface charge is very similar for gate layers with different dielectric constants, although very different gate voltages (and gate fields) are required in each to produce similar mobility values.[8]

In conclusion, the authors think that the best strategy for high-performance OFET gate insulators is a multi-layer structure comprising a gate planarization layer to produce smooth insulator surfaces, a high permittivity inter-layer to maximize the gate insulator capacitance, and a thin, low-polarity layer adjacent to the organic semiconductor to minimize trapping at the interface and to maximize the polymer ordering and alignment (polymer morphology is improved) near the interface.

4.2.6.4 Organic Semiconductor/Gate Insulator Interface

Since the OFET carrier channel region is two-dimensional and confined very close to the gate insulator/organic semiconductor interface, all of the channel charge is expected to be localized within the first few monolayers near the interface in the organic semiconductor.[48] These localized charges will screen out the electrical field in the rest of the semiconductor. This is consistent with the independence of the OFET field-effect mobility on the semiconductor film thickness mentioned above.

Carrier transport takes place at or near the organic semiconductor/gate insulator interface by thermally activated hopping between localized states, which may be formed by individual molecules or a number of molecules together. Therefore, the nature of this interface is very important for OFETs. As stated above, the carrier localization may be enhanced or reduced by local polarization and disorder effects that can distort these states. One method to control both the polarization and disorder effects is to chemically treat the gate insulator surface. Hexamethyldisilazene (HMDS), octadecyltricholorosilane (OTS), or other silane or alkyl treatments with reactive end-groups have been used to provide self-assembled monolayers (SAMs) with a well-defined, ordered surface for subsequent organic semiconductor deposition.[49] Most of these layers are hydrophobic, *i.e.*, they make the dielectric surface less polar and hence tend to repel water. Improvements in the electrical performance (higher field-effect mobility) of the OFETs have been attributed to improved molecular organization, grain size, morphology, spatial ordering of the organic semiconductor, or reduced surface roughness of the gate dielectric layer.[7] However, even if monolayer surface treatments with the organic layers having low dielectric constants indeed reduce the energetic disorder mentioned above, an effective screening from dipoles may require greater distances from a polar surface than a few monolayers. In addition, monolayer treatments of the surfaces in practice

are difficult to apply reproducibly over large areas, and this process takes a long time (sometimes several hours), especially if there is a reliance on chemical bonding to the surface. Their stability, sensitivity to water, and surface quality of electrodes present further difficulties. As a result, it can be argued that to fabricate reliable OFETs based on organic polymers it is desirable to use thin (50 to 70 nm) gate dielectric layers with low dielectric constant at the organic semiconductor/gate dielectric interface. Thin layers are necessary in order to reduce electrical instability and impact of the dielectric constant on the OFET threshold voltage. Finally, it would be very beneficial for OFET performance if this layer could also enhance ordering in the organic semiconductor layer. Indeed, it has been shown that ordering in organic polymers can be produced by a polyimide alignment layer in combination with a liquid crystal polymer. Rubbed polyimide allows the alignment of polymer chains in preferred directions. This ordering significantly enhanced OFET field-effect mobility by controlling the microstructure of the polymer films through a self-organization mechanism.[50,51]

4.2.7 Device Instabilities

4.2.7.1 Electrical Instabilities

OFETs can exhibit significant degradation in electrical performance after operation during even moderate lengths of time.[52,53] This electrical instability is a critical issue that needs to be addressed before these devices can be used in practical applications. The characterization of the device aging process (in other words, aging effects which are incurred when the device is powered) is usually based on the investigation of the effect of a *bias temperature stress* or BTS experiment. This experiment consists in applying a stress voltage on the OFET gate during a given time, at a given temperature, while the S/D voltage is kept constant. Transfer characteristic measurements have shown that the main effect of such electrical stress, for negative stress voltages, is a shift of the device threshold voltage, as seen in Figure 4.2.25. In Figure 4.2.26, it can be seen that, after a negative electrical stress, the device field-effect mobility and subthreshold swing do not change significantly. The device threshold voltage shift after a stress duration t_{stress} can be defined by

$$\Delta V_T(t_{stress}) = V_T(t_{stress}) - V_T(t=0) \qquad (4.2.73)$$

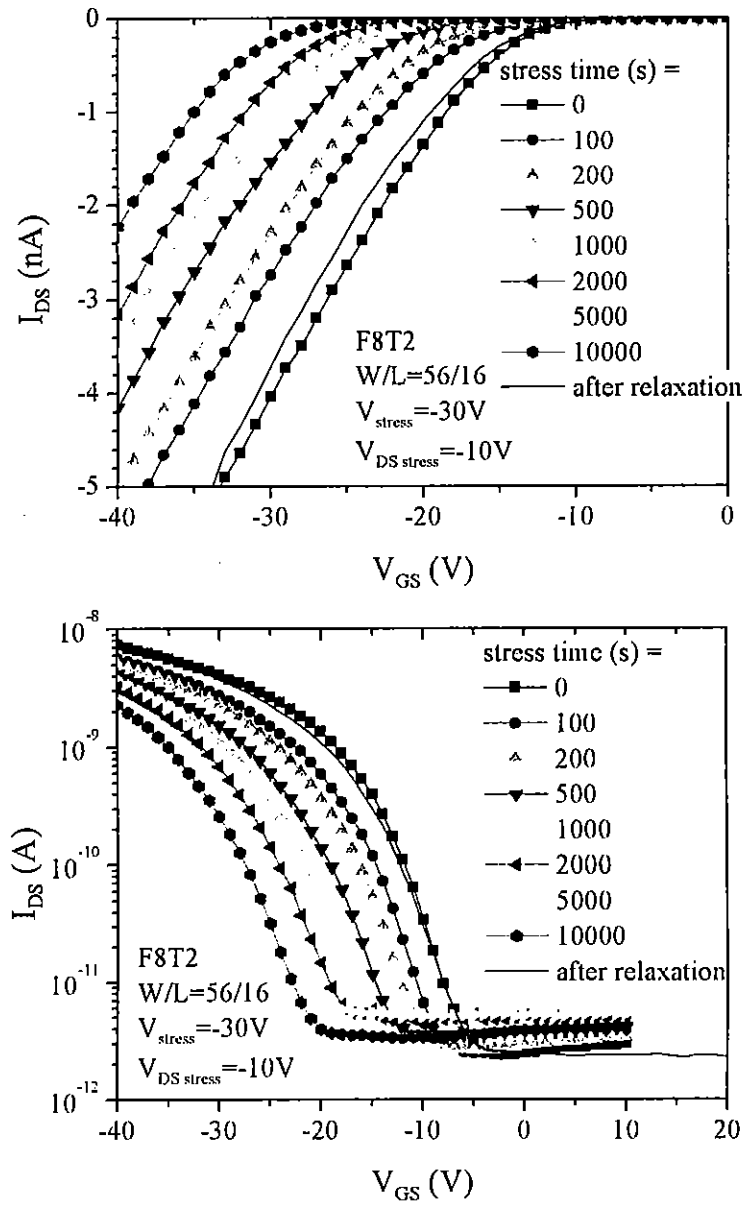

Figure 4.2.25. OFET transfer characteristic before and after bias temperature stress and after relaxation.

For negative stress voltage, the threshold voltage shift ΔV_T is negative (in a typical plot, the curve translates to the left) and can be as high as –20 V after 1000 s of continuous gate bias stress at –30 V at room temperature, as seen in Figure 4.2.27. It has also been observed that the effect of a large positive stress voltage (+30 V) is quite different: the threshold voltage shift is relatively small, but the main effect of the stress is a drastic degradation of the subthreshold swing. In this chapter, only the effect of negative stress voltages applied on the gate will be considered.

A common procedure to assess the effect of the BTS on the device electrical characteristics involves the interruption of the electrical stress at given stress times: the device characteristic is quickly measured and the bias stress immediately resumed. This method assumes that device relaxation during the measurement time is negligible and will not affect the device behavior under subsequent electrical stress. Alternatively, it is also possible to measure the device drain current during the stress and to calculate the corresponding threshold voltage shift from the drain current versus stress time curve and the initial device transfer characteristic. More precisely, if it is assumed that the measured change in the OFET drain current is only associated with a shift of the transfer characteristic, the threshold voltage shift can be calculated as illustrated in Figure 4.2.28. This method does not require any interruption of the stress, but is only applicable when the OFET is in accumulation during the stress (large negative stress voltages). In addition, because it assumes that the only effect of the stress is a shift of the threshold voltage, this method does not allow for the investigation of possible changes in field-effect mobility and subthreshold swing. Both methods usually yield consistent results.

Detailed analysis of the device electrical instabilities includes the evaluation of the dependence of the threshold voltage shift on the stress voltage, time, and temperature. Results obtained for inorganic amorphous semiconductor-based TFTs have led to the following expression of the threshold voltage shift

$$\Delta V_T = B\left(1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right) \tag{4.2.74}$$

where V_{stress} is the stress voltage applied to the gate, and B, τ, and β are fitting parameters that can depend on the stress voltage, stress temperature, and the device and material characteristics.[54] Using this equation, the authors have been able to fit experimental data as illustrated in Figure 4.2.27. Fitting parameters are summarized in Table 4.2.4. It can be noted that the values of β are quite high compared to typical room-temperature values

obtained for inorganic TFTs $\beta \approx 0.33$, where β is usually associated with the carrier dispersive transport in the amorphous semiconductor.[54] The prefactor B depends significantly on the stress voltage, and several equations have been used to describe it for inorganic TFTs[32,54]

$$B = V_{stress} - V_T(t=0) \tag{4.2.75}$$

or

$$B = K\left(V_{stress} - V_T(t=0)\right)^{\alpha} \tag{4.2.76}$$

where K is a fitting parameter and α a temperature dependent coefficient. Further analysis is required to determine the best equation describing the stress voltage dependence of the prefactor B in OFETs.

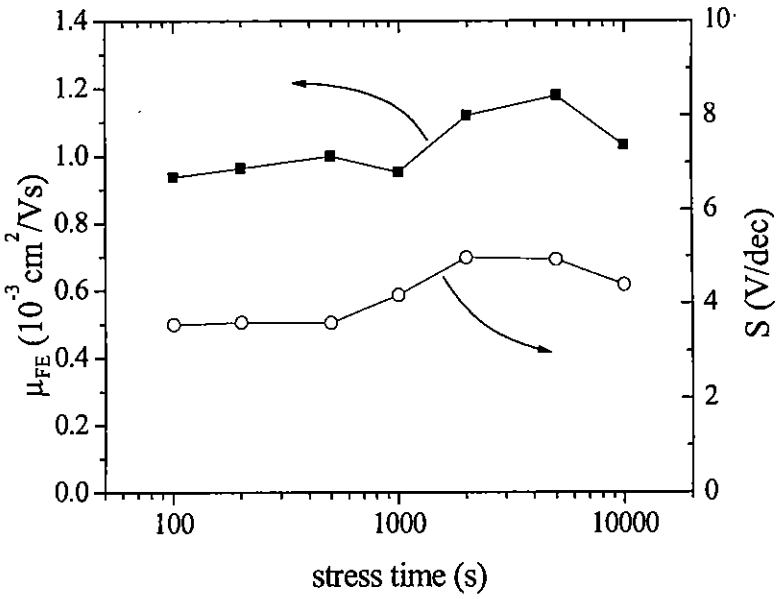

Figure 4.2.26. Variations of the OFET field-effect mobility and subthreshold swing with stress time.

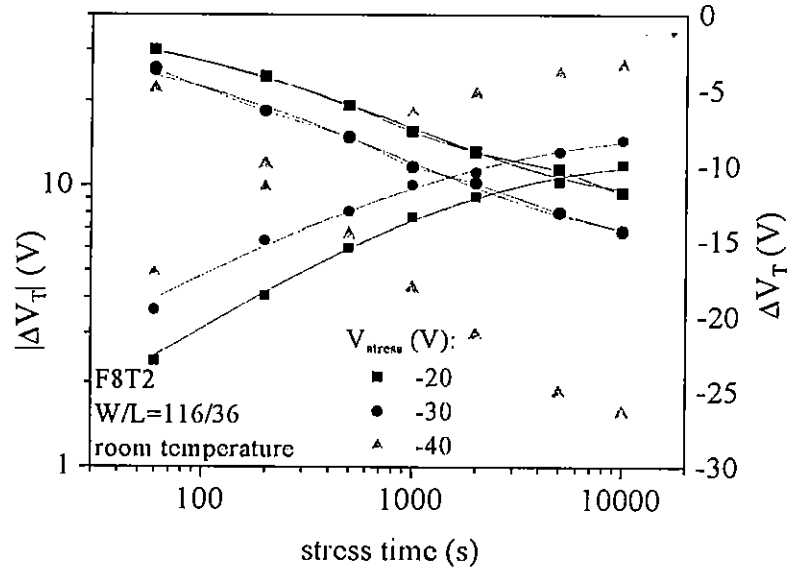

Figure 4.2.27. Threshold voltage shift variations with stress time. Symbols show experimental data, solid line shows fit to Equation 4.2.74.

Table 4.2.4. Fitting parameters used for the threshold voltage shift curves shown in Figure 4.2.27.

V_{stress} (V)	−20	−30	−40
V_{Ti} (V)	−14.6	−25.4	−18.2
B (V)	12	15	26.5
β	0.51	0.44	0.57
τ (s)	1060	910	810

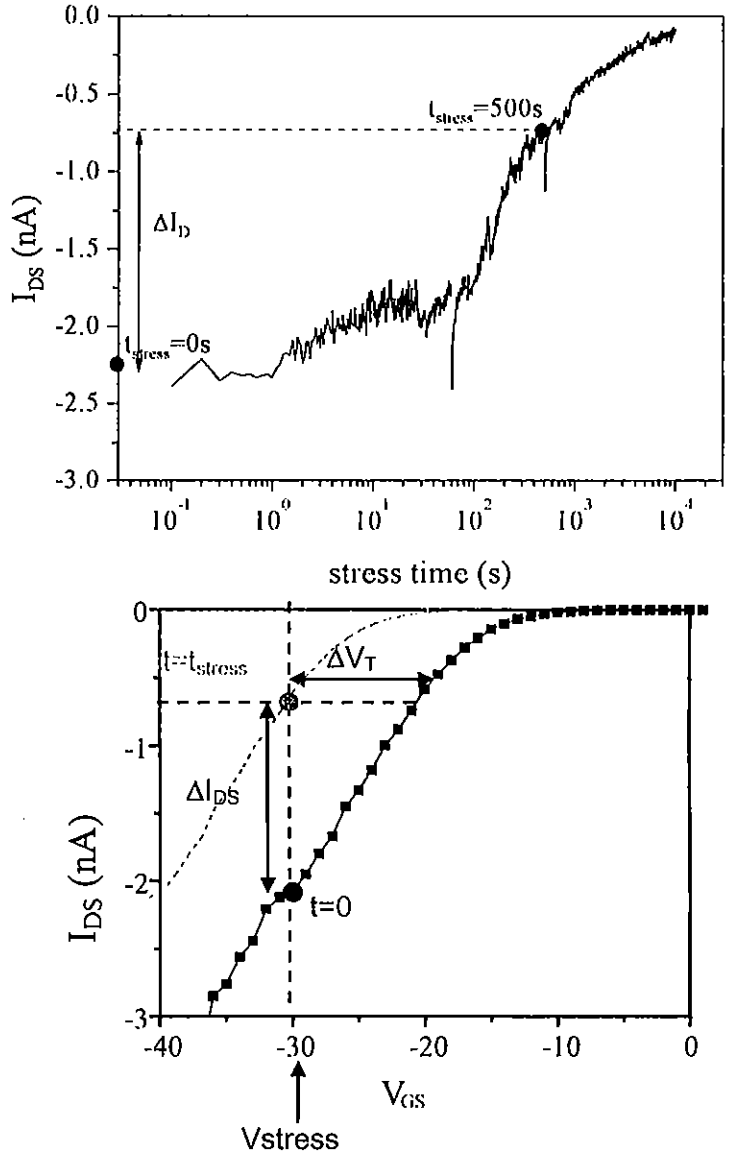

Figure 4.2.28. (top) Long-term time dependence of the OFET drain current resulting form electrical instabilities. *(bottom)* Method to calculate equivalent threshold voltage shift from curve shown in *(top)*.

Possible mechanisms responsible for the threshold voltage shift include injection and trapping of carriers into the gate insulator, trapping of carriers in the organic semiconductor near the gate insulator/semiconductor interface, and creation of defects in the organic semiconductor. Ion movement in the gate insulator has also been observed in devices using polymeric gate insulators.[54] However, in OFETs using benzocyclobutene and PECVD amorphous silicon nitride as a gate insulator bilayer, the authors have observed negative threshold voltage shifts for all negative stress voltages, regardless of the applied source-drain voltage. This suggests that the ion effect observed by others on devices using polymeric gate insulators is most likely not significant in our case. In addition, it was observed for the OFETs shown here that the threshold voltage shift is fully reversible, *e.g.*, the OFET characteristic measured after relaxation was usually similar to the initial curve, as shown in Figure 4.2.25. The authors have observed that this relaxation is significantly accelerated by exposing the OFET to illumination. These observations could suggest that the mechanism responsible for the threshold voltage shift may be trapping of charges (holes) in the organic semiconductor film in shallow defect states, and that defect creation or charge injection in the gate insulator are unlikely.

4.2.7.2 Effect of Illumination on Device Electrical Characteristics

The electrical characteristics of OFETs can be affected by light (photons) if it is absorbed by the organic semiconductor.[55] The device off-current can increase by several orders of magnitude depending on the level of illumination, while the on-current is often not significantly affected, as seen in Figure 4.2.29. The drain current increase in the 'off' state can be explained by the photo-generation of holes and electrons in the TFT channel due to the light absorption.

The photoelectric effects within organic materials, which is not yet fully understood, is often different from what occurs in inorganic semiconductors, because of the strong electron-phonon interactions. One of the main differences is that photo-excitation in those materials does not automatically lead to the direct generation of free charge carriers, but to bound electron-hole pairs (so-called *excitons*), with a binding energy of about 0.4 eV. These excitons need to be split up (or *dissociated*) before the charge can be transported through the channel and collected at the source and drain contacts. It should be noted that such excitons and charge transport in organic polymers usually require thermally activated hopping/tunneling processes from chain to chain. Thus, close packing of the chains is assumed to decrease the width of the inter-chain barriers. In addition, flat molecule structure should also generally lead to better transport

properties and high absorption coefficient. It has been observed that the density of photo-generated excitons depends directly on the size (area) of the OFET, and that the diffusion length is small (typically about 10 nm) compared to the device thickness (typically 100 nm). Finally, impurities present within the organic polymer, such as oxygen, can also be involved in the exciton dissociation into separate charges.

Absorption of photons will lead to photo-generation of *excitons* (bound electron-hole pairs), rather than free carriers. The excitons carrying energy, but no net charge, may diffuse to dissociation sites (traps or impurities) where the charges can be separated. Under the influence of the source-drain voltage, the excitons will be separated into free charges that will then travel to respective device electrodes (holes to the drain and the electrons to the source), thereby increasing the total drain current.

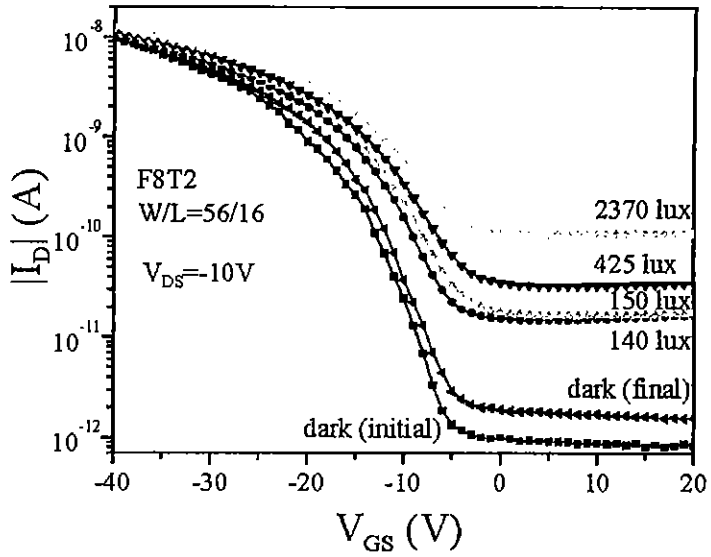

Figure 4.2.29. OFET transfer characteristics in the dark and under broadband illumination.

The ratio of the drain current under illumination to the drain current in the dark (*photoconductive gain*) can be defined as

$$R_{L/D} = \frac{I_D^{illum}}{I_D^{dark}} \qquad (4.2.77)$$

and is a function of the OFET gate voltage (V_{GS}), and the amount of light received by the device (illuminance, *IL*, in lux). In the strong accumulation regime, $R_{L/D}$ decreases because of the dominant effect of the gate voltage on the concentration of accumulated carriers. In the 'off' state, $R_{L/D}$ can reach two to three orders of magnitude, depending on the level of illumination, and is not strongly dependent on the gate voltage V_{GS}, as seen in Figure 4.2.30. It should be noticed that high values of $R_{L/D}$ are obtained at $V_{GS} = 0$ V.

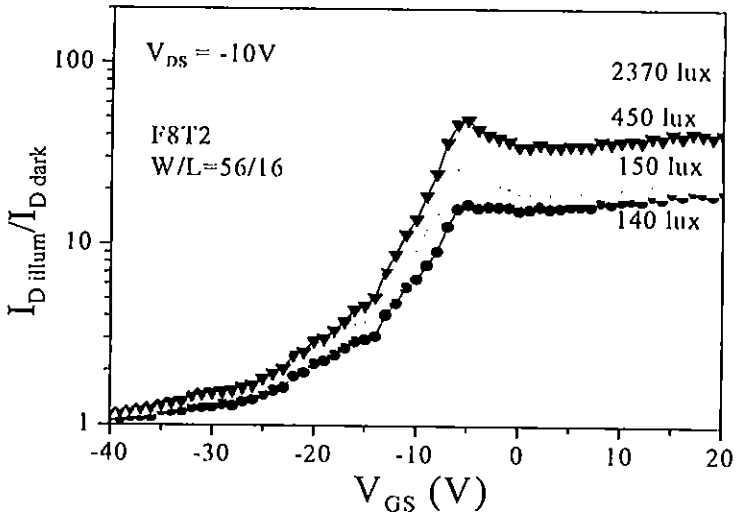

Figure 4.2.30. Ratio of illumination to dark OFET current under different illumination conditions.

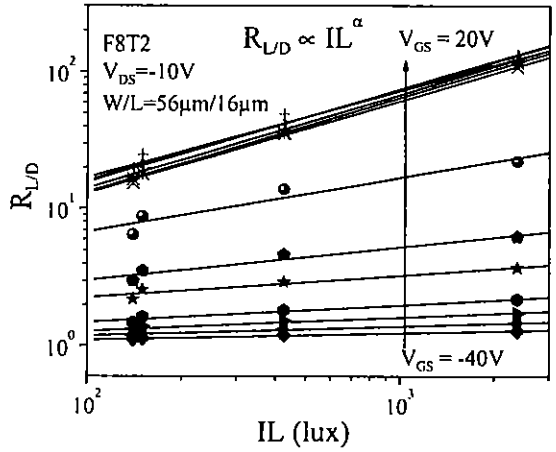

Figure 4.2.31. Variations of $R_{L/D}$ with white light illumination for several values of the gate voltage. Symbols show experimental data, solid lines represent power law fit with exponent α.

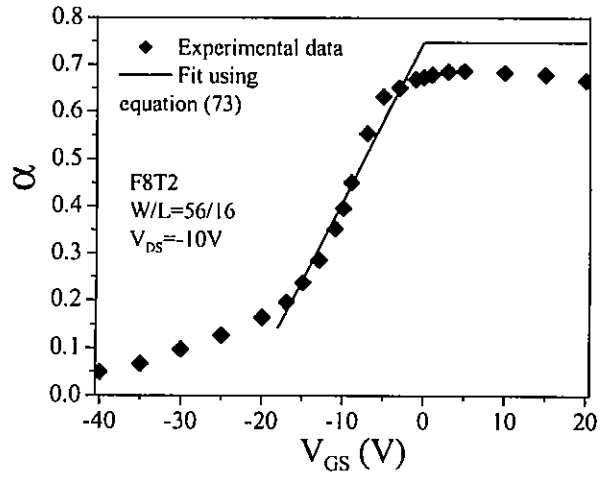

Figure 4.2.32. Gate voltage dependence of the parameter α extracted from Figure 4.2.31. Also fit of experimental data to Equation 4.2.79 is shown (*solid line*).

It has also been observed that $R_{L/D}$ exhibits a power law dependence on the illumination level, as seen in Figure 4.2.31 where the experimental data is fitted by

$$R_{L/D} = IL^{\alpha} \tag{4.2.78}$$

where α is a function of the applied gate voltage as shown in Figure 4.2.32 and as described by the following equations[56]

$$\alpha(V_{GS}) = \alpha_0\left(1 - \frac{V_{GS}}{V_{GC}}\right) \text{ for } V_{GS} < 0 \tag{4.2.79a}$$

$$\alpha(V_{GS}) = \alpha_0 \text{ for } V_{GS} > 0 \tag{4.2.79b}$$

In this equation, α_0 is a material-dependent constant, V_{GS} is the applied gate-to-source bias, and V_{GC} is a parameter that has been associated in inorganic semiconductors with the total density of states at the midgap.[56] For the authors' devices, the values of α_0 and V_{GC} that were obtained were approximately 0.75 and –21 V, respectively.[57] This power-law dependence on illumination is expected when trapping and subsequent de-trapping of the carriers are involved in the channel conduction process., *e.g.*, dispersive transport.[56]

The timescale for the device to respond to the illumination is typically several seconds at room temperature, while the timescale for the device to return to the original state, after the illumination is removed, is on the order of one hour at room temperature.[58]

4.2.7.3 Effect of Air on Device Electrical Characteristics

In general, most of the solution-processed organic polymers are unintentionally extrinsically *p*-type, doped by either residual impurities left from synthesis or atmospheric oxygen. It is argued that oxygen is acting as traps for electrons (this can produce *p*-type organic semiconductors), and polymer sensitivity to unintentional doping is due to its low ionization potential. In comparison to P3HT (poly-3-hexylthiophene), the OFETs based on F8T2 discussed in this chapter exhibit a higher stability against doping by atmospheric oxygen and other impurities as evidenced by high on/off current ratio. This is due to high ionization potential of F8T2 in comparison to P3HT. Most of the OFETs that are sensitive to air show very

low on/off current ratio (on the order of 10 to 100) and high 'off' current. These OFETs characteristics can be improved by performing all solution preparation and device processing steps, and measurements under dry nitrogen with a residual oxygen concentration lower than 2 to 4 ppm.[59] For P3HT OFETs fabricated in a dry box, exposure to air for a few minutes is sufficient to produce extrinsic doping. In this case, a thin capping layer or device packaging inside a dry box is required to achieve improved OFETs characteristics. For low-cost organic electronics, air-stable OFETs are needed.

4.2.8 Conclusion

The low field-effect mobility values of OFETs can lead to low frequency electronics and, if the minimum length scales of silicon technology are sacrificed in order to realize a cheap technology, polymer-based electronics will be orders of magnitude slower than equivalent silicon-based circuits. However, for some applications, speed is less of an issue than cost. Therefore, organic electronics has the potential to create new business opportunities, which will multiply in tandem with improvements in OFET performance. High doping of the organic semiconductor may be able to increase the device field-effect mobilities but only at the expense of increased bulk conductivity, which could subsequently lead to insufficient drain current modulation. Higher device field-effect mobilities at low doping concentrations are very desirable for future organic devices. To achieve high field-effect mobilities, there must be both short distances between hopping or tunneling sites and a good inter-site π-electron overlap. Crystalline packing of through-conjugated material represents the optimal organic system for intrinsic high field-effect mobility devices. To maintain low cost, these materials should be processed at low temperature and from solution, and must be stable in air at room temperatures or higher. The alternative approach would be to use liquid crystal (LC) polymers that can be aligned by an alignment layer, an electrical field, or a thermal treatment. This alignment of the LC polymers will enhance material ordering and improve device electrical performance.

4.2.9 Acknowlegments

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