20.7 A 13.8μW Binaural Dual-Microphone Digital ANSI S1.11 Filter Bank for Hearing Aids with Zero-Short-Circuit-Current Logic in 65nm CMOS

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This paper presents an ANSI S1.11 1/3-octave filter-bank chip for binaural hearing aids with two microphones per ear. Binaural multimicrophone systems significantly suppress noise interference and preserve interaural time cues at the cost of significantly higher computational and power requirements than monophonic single-microphone systems. With clock rates around the 1MHz mark, these systems are ideal candidates for low-power implementation through charge-recovery design. At such low clock frequencies, however, charge-recovery logic suffers from short-circuit currents that limit its theoretical energy efficiency [1]. The chip described in this paper is designed in 65nm CMOS using a new charge-recovery logic, called zero-short-circuit-current (ZSCC) logic, that drastically reduces short-circuit current. It processes 4 input streams at 1.75MHz with a charge recovery rate of 92%, achieving 9.7× lower power per input compared with the 40nm monophonic single-input chip that represents the published state of the art [2].

The structure and operation of ZSSC logic are described in Fig. 20.7.1. ZSSC is a dynamic dual-rail logic consisting of two pull-up (PUN) and two pull-down (PDN) networks with high-V_{th} NMOS devices for evaluation, and two low-V_{th} PMOS devices as state elements, all supplied by a charge-recovery power-clock waveform PC. A four-phase power clock generated by two H-bridges operating in quadrature is used to synchronize ZSSC cascades. Driven by two 180-degree out-of-phase pulses with tunable duty cycle, each H-bridge uses an inductor to replenish dissipated energy by resonating the parasitic capacitance of the clock distribution network and ZSSC gates. ZSSC operation is divided into four stages: evaluate, hold, recover, and wait. During evaluate, inputs are held stable by the fanin gates, and function evaluation is performed, with one of the output nodes charged through PUN and pulled to full swing by the PMOS pair. During hold, outputs are held stable, and fanout gates evaluate. During recover, the charge at the output nodes is recovered by the power-clock, and output voltage is brought back to V_{th} levels. During wait, any residual charge that has not been recovered is discharged to ground or PC before the next cycle begins.

Unlike previous charge-recovery logic families, such as SBL [1], that introduce multiple short-circuit-current paths due to interleaving of stages, the four-phase clock in ZSSC divides gate operation into fine-grain stages, providing time to reset outputs, and preventing complementary output signals from overlapping. Moreover, ZSSC logic does not use a DC supply, preventing the possibility of connecting power and ground during operation. As shown in the simulation results in Fig. 20.7.1, no current flows into ground except during wait, when residual output charges are discharged. Compared with the charge-recovery logic in [3], ZSSC limits voltage drop between PC and output nodes through the introduction of the two PUNs, preventing current spikes during operation and forcing the charging NMOS devices in deep triode region to function as ideal resistors. As shown in Fig. 20.7.1, the output voltage closely tracks PC during evaluate, consistent with adiabatic design principles that require only small voltage drops across conducting resistive paths.

To enable an automated place-and-route flow, a ZSSC library is implemented consisting of 64 cells with a variety of drive strengths. Schematic and layout of a ZSSC Booth selector cell are shown in Fig. 20.7.2. Using NMOS in PUN and removing input inversion, a compact cell layout is obtained with 8% area penalty over its static CMOS counterpart. With state embedded in each gate, flip-flops are eliminated from ZSSC pipelines, saving area and power compared to static CMOS design.

Four interleaved clock meshes, implemented in top-level metal-9 and 8 as shown in Fig. 20.7.3, are used to distribute the four clock phases with minimal skew. Each top-level mesh is connected directly to metal-3 power-clock stripes running along the cell rows. During placement, each cell is automatically placed in the row immediately above or below the metal-3 stripe of the corresponding power-clock phase, minimizing local clock interconnect and yielding a placement density of 81.4%. Two off-chip inductors resonate the parasitic capacitance of the four-phase clock distribution network and the ZSSC gates through 4 local pairs of on-chip H-bridge drivers. Each driver is designed with programmable widths (5.4μm to 37.8μm NMOS) to support different clock speeds and enable tuning for maximum energy efficiency. The H-bridges are driven by four pulses in quadrature generated by a finite-state machine PG running off a reference clock. To allow for energy efficiency tuning, PG can be programmed to generate pulses with duty cycle ranging from 2.5% to 25%. Symmetric distribution of the pulses reduces skew at the H-bridges, resulting in 135.6ps of worst-case skew at 0.6V supply based on simulations of extracted layout.

As shown in Fig. 20.7.4, the binaural chip time-multiplexes 4 inputs (two inputs per ear) onto a datapath consisting of 4 second-order biquad sections that are cascaded to implement 18 ANSI S1.11 1/3-octave frequency bands F22 to F39. Each section consists of three 2.25-cycle (9-phase) multiply-accumulate units, each designed by merging a hybrid carry-lookahead/carry-select adder and a Booth-encoded multiplier. Two shift registers record the most recent audio cycle states to avoid pipeline stalls. Four-phase clocking lowers overall cycle count and latency, enabling the use of a relatively slow clock frequency.

Fabricated in a 65nm CMOS process, the chip is tested at various clock frequencies using two 4.95×3.81mm^2 surface-mount inductors to resonate parasitic capacitance. Fig. 20.7.5 shows measured energy per clock cycle and power vs. operating frequency for different inductance values. The graph shows the scaling of energy consumption with frequency, as expected from charge recovery design. The ANSI S1.11 standard is met at 1.75MHz with 7.87pJ per cycle. Minimum energy consumption is 7.36pJ per cycle at 1.47MHz with supply voltage VDD = 0.57V and 5% pulse duty cycle. Unlike SBL [1], no sharp increase in energy consumption from short-circuit currents is observed at lower clock frequencies, with energy per cycle gradually increasing below 1MHz due to leakage current.

Figure 20.7.6 compares the chip in this paper with the state-of-the art hearing-aid chip in [2] and a silicon cochlea for an IoE detection task from [4]. Compared to the 40nm single-input chip in [2], this 65nm 4-input chip achieves 9.7× lower power per input/band. Compared to the chip for audio sensing applications in [4], that greatly benefits from efficient analog approaches, this charge-recovery low-power digital filter provides superior energy efficiency and programmable filter coefficients that support the adjustments necessary with hearing aids.

A die microphotograph is shown in Fig. 20.7.7. To reduce the parasitic resistance of wirebonding and I/O pads, the two off-chip inductors are connected to the die with three pads per clock phase. A built-in-self-test (BIST) circuit is implemented with static CMOS logic to verify functionality of the hearing aid. This ZSSC-based hearing-aid chip demonstrates the reduction of energy consumption in a low clock-frequency application by almost an order of magnitude through charge-recovery design using an automated flow.

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References:
[1] W. H. Ma, et al., "187 MHz Subthreshold-Supply Charge-Recovery FIR," *JSSC*, vol. 45, no.4, pp. 793-803, 2010.
[2] J. S. Wang, et al., "A 0.36V, 33.3 μW 18-band ANSI S1.11 1/3-Octave Filter Bank for Digital Hearing Aids in 40nm CMOS," *IEEE Symp. on VLSI Circuits*, pp. 254-255, 2013.
[3] Y. Moon, et al., "An Efficient Charge Recovery Logic Circuit," *JSSC*, vol. 31, no. 4, pp. 514-522, 1996.
[4] M. Yang, et al., "A 0.5V 55μW 64×2-Channel Binaural Silicon Cochlea for Event-Driven Stereo-Audio Sensing," *ISSCC*, pp. 388-389, 2016.

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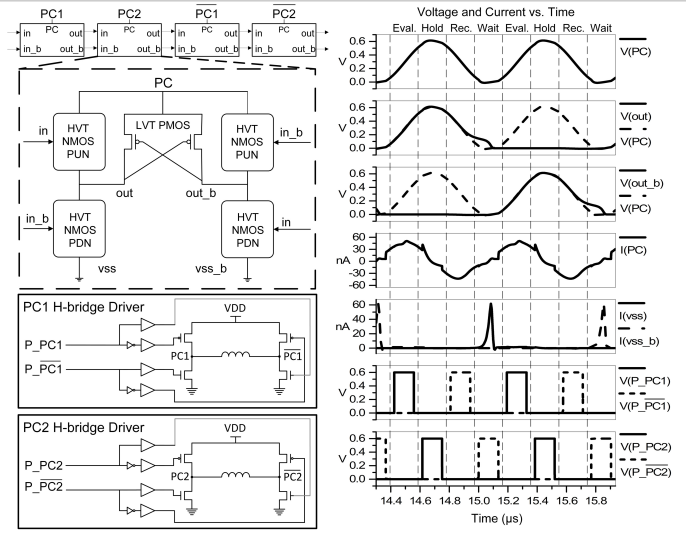

Figure 20.7.1: Schematic of a ZSSC gate, cascade of ZSSC gates, four-phase power-clock generator, and simulated operating waveform.

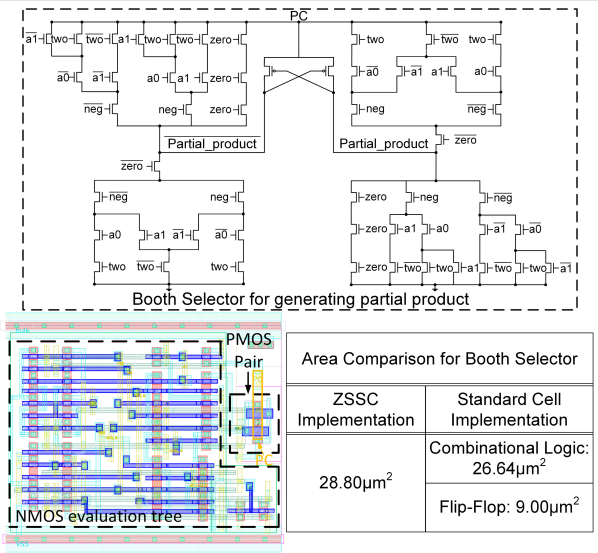

Figure 20.7.2: Schematic, layout and area comparison of a Booth selector.

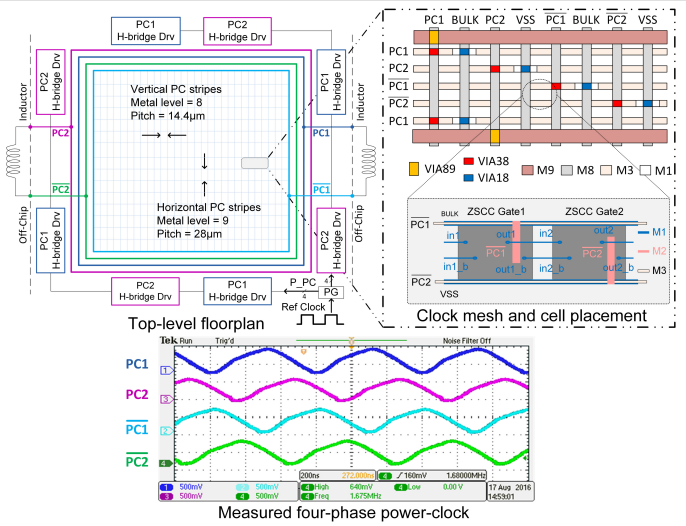

Figure 20.7.3: Top-level floorplan showing four-phase clock mesh and cell placement, and measured four-phase clock waveform.

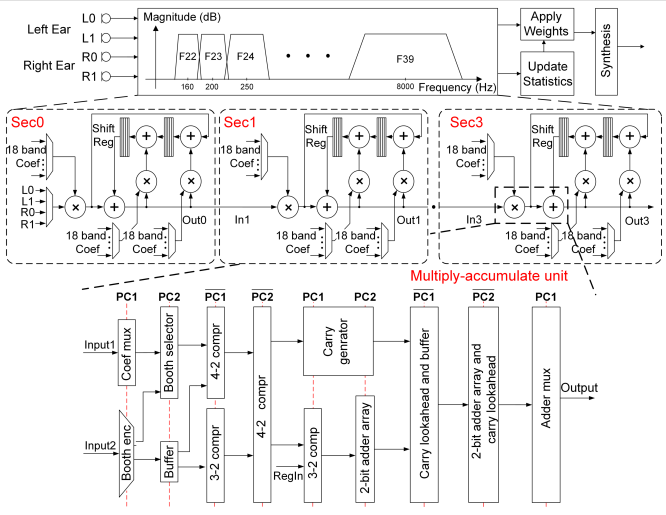

Figure 20.7.4: ANSI S1.11 1/3-octave binaural hearing aid: bands F22 to F39, datapath block diagram, and detail of multiply-accumulate unit four-phase pipeline implementation.

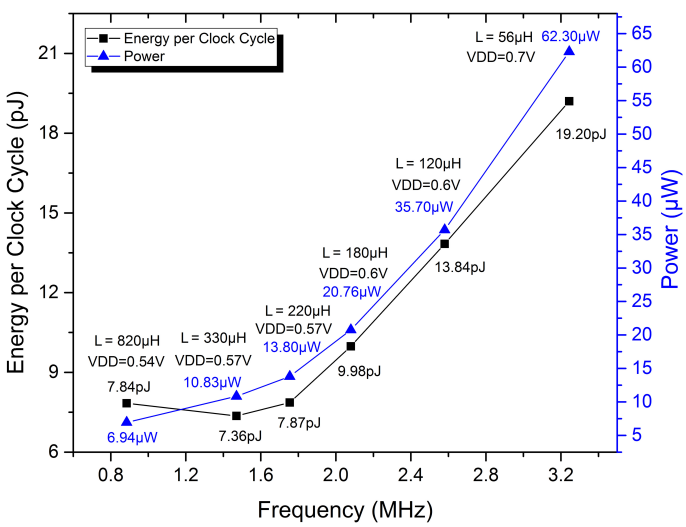

Figure 20.7.5: Measured energy per clock cycle and power versus frequency.

	This Work	VLSI'13 [2]	ISSCC'16 [4]
Technology	65nm	40nm	180nm
Application	Hearing Aid	Hearing Aid	Silicon Cochlea for IoE
Processing	Digital Filter Bank	Digital Filter Bank	Analog Filter Bank + Event coding
Standard	ANSI S1.11 1/3 Octave	ANSI S1.11 1/3 Octave	N/A
Binaural	Yes, 2x2 inputs	No, 1 input	Yes, 2x1 inputs
# Bands	18x4	18	64x2
Technique	ZSSC	TBLB[1]	Analog Filtering + ADM[2]
Programmability	Digital coefficients	Digital coefficients	Bias current
Area per band (10^{-3}mm²)	9.34	5.27	262
Clock Frequency (MHz) / Sampling rate (kHz)	1.75 / 24	12 / 24	N/A
Power Supply (V)	0.57	0.36	0.5
Power (µW)	13.8	33.3	55
Power per input (µW)	3.45	33.30	27.50
Power per band (µW)	0.19	1.85	0.43

Area and power are not normalized for technology scaling.
[1] Time borrow and local boost (TBLB)
[2] Asynchronous delta modulation (ADM)

Figure 20.7.6: Chip summary and comparison with state of the art.

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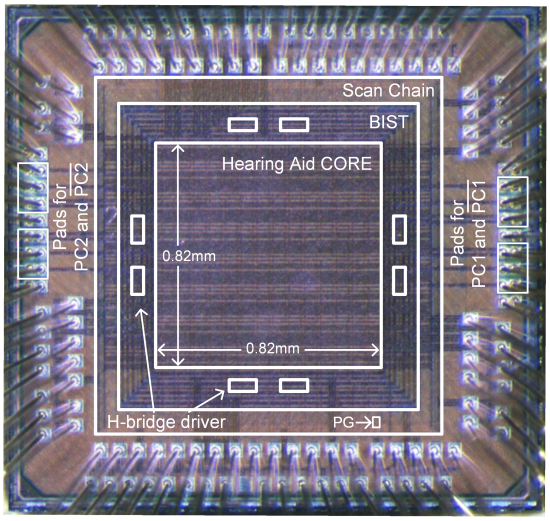

Figure 20.7.7: Microphotograph of the ZSSC hearing aid test chip in 65nm CMOS.

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