24.3 An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis

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Electrocardiography (ECG) is a critical source of information for a number of heart disorders. In arrhythmia studies and treatment, long-term observation is critical to determine the nature of the abnormality and its severity. However, even small body-wearable systems can impact a patient's everyday life and signals captured using such systems are prone to noise from sources such as 60Hz power and body movement. In contrast, implanted devices are less susceptible to these noise sources and, while having closer-spaced electrodes, can obtain similar quality ECG signals due to their proximity to the heart [1]. In addition, implanted devices enable continuous monitoring without affecting patient quality of life. As in other implantable systems, low power consumption is a critical factor; in this case to provide a sufficiently long operating time between wireless recharge events.

This paper reports a syringe-implantable ECG recording and analysis device targeted primarily at arrhythmia monitoring (Fig. 24.3.1). In contrast to surgically implanted devices with large batteries such as pacemakers, the device is designed for daily wireless recharging, allowing for a much smaller battery. In order to pass through the needle canula during implantation, device width is limited to 1.5mm while overall system length is designed to be 2cm, providing sufficient distance between two electrodes to yield an acceptably large potential difference. The signal from electrodes is filtered, amplified, and converted to the digital domain by an analog front-end (AFE). A digital signal processing (DSP) module analyzes the waveform within a 10-second search window and detects abnormal cardiac events. When an abnormal event is detected, the device stores the current search window waveform into local memory; it can then be transferred to an external device through means such as a wireless transceiver for further analysis by clinicians. Assuming nightly wireless data readout and battery recharge, the design targets 5-day lifetime (providing a safety margin) when powered by an on-chip thin-film Li battery (5μA•hr, 4V). This translates to 167nW average system power consumption, presenting a challenging power constraint given that comparable systems in the literature typically consume 10 to 30μW [2, 5-7].

The AFE consists of a low-noise instrumentation amplifier, a variable-gain amplifier, and a successive-approximation register (SAR) analog-to-digital converter (ADC). To reduce power consumption, all building blocks except the ADCs clocked comparator are biased in the subthreshold regime. Due to the resulting high performance variability, the amplifier gain, bandwidth, and input-referred noise are all tunable by the subsequent digital blocks. Similar to other noise-limited amplifier designs [2], the first stage of the amplifier dominates total AFE power consumption. This design uses an inverter-based amplifier for high noise efficiency and its tail current can be tuned to match the desired noise level. Aided by the DSP algorithms, the system accurately detects arrhythmia with up to 15μV noise when tested under a database of ECG data collected from arrhythmia patients (Fig. 24.3.2). Since first-stage current consumption is largely dictated by input referred noise magnitude, we target a 9μV noise floor (excluding ADC distortion and margins), reducing AFE and system power by 6.7× and 2.15×, respectively, compared to typical ECG signal acquisition designs that require noise levels of ≤3μV [2]. Subsequent amplifiers are not noise-limited and therefore are designed to consume only 100s of pAs. A common problem of the inverter-based design is that the bias point is vulnerable to PVT variations. Therefore, a DC servo loop is used to stabilize the differential output to half V_{DD} (Fig. 24.3.2, left). Due to the large tissue-electrode impedance, the AFE input amplifier requires very high input impedance and, therefore, both AC coupling and an impedance-boosting loop are implemented.

Analog-to-digital conversion uses an 8b single-ended asynchronous SAR ADC with 500Hz sampling rate. Traditional asynchronous logic uses dynamic logic, which suffers from high leakage in a low voltage/frequency ECG application. Therefore, dynamic nodes are implemented with latches that are clocked by internal signals and delay lines (Fig. 24.3.3). To improve energy efficiency, a 10fF DAC unit capacitor and split capacitor array topology are used, enabling 1.97× ADC power reduction. Also, the comparator is a clocked 1-stage design chosen for low dynamic power consumption. However, the 1-stage clocked comparator and small capacitor array make the comparator input vulnerable to kickback noise. A split footer comparator [3] combined with cross-coupled compensation addresses this issue, reducing kickback noise by 84.9× (simulated). The measured amplifier current consumption is 31nA at 0.6V with input-referred noise at signal band of 6.52μV.

Figure 24.3.4 shows the digital processing back-end. The back-end detects the incoming signal amplitude and tunes AFE gain accordingly. Input samples from the ADC are first processed by a 600ms moving average filter (MAF) that removes the relatively slow baseline shift. To minimize power, we use frequency-domain processing with a lower sampling rate (yet comparable detection performance) than conventional QRS-peak detection algorithms. The frequency dispersion metric (FDM) block performs an FFT on the 10× downsampled ECG waveform and observes whether dominant clear peaks exist in a specific frequency range, which represents a stable heartbeat. A 512-point real-valued FFT accelerator takes in data from one of two ping-pong buffers and computes the FFT on a separate local buffer, thereby preserving the stored waveform. Once an arrhythmia is detected, the ping-pong buffer storing the last search window no longer accepts new samples until the waveform is fully read out through a data bus; meanwhile the other buffer acts as the primary input data channel. The actual arrhythmia detection algorithm is performed in an ARM Cortex-M0+ core and instruction memory can be programmed with different algorithms for flexibility.

Due to the low throughput requirement, the required operating voltage/frequency pair is located below the minimum energy point (Fig. 24.3.4). Therefore, the system operates at the minimum energy point (MEP) with the Cortex-M0+ core working in burst-mode (~6× faster than required). The core is then power-gated after processing of each 10s window is complete. This duty cycling ensures each operation consumes the minimum possible energy, reducing power of the duty-cycled block by 40%. The design can also perform standard QRS-peak detection (R-R block), which uses peak-to-peak distances to determine ECG signal regularity. A reconfigurable 80-tap FIR filter performs a band-pass filter on the input signal. Finally QRS peaks are detected using a threshold on the differentiated signal and the variance of peak-to-peak distance is used in detecting arrhythmia. A clinician can enable one of the two processing paths (FDM or R-R) with the other power gated.

The ECG monitoring SoC is fabricated in 65nm LP CMOS. It successfully communicates with other chips including a power management unit and external memory from [4] over a data bus; the complete system configuration is described in Fig. 24.3.5. The SoC is tested under different scenarios including an ECG simulator as well as an isolated sheep heart; measured waveforms are shown in Fig. 24.3.5. The SoC consumes 64nW and 110nW when running the FDM and RR algorithms, respectively, enabling >5 day lifetime with a 3.7mm² (5μA•hr) thin-film battery.

References:

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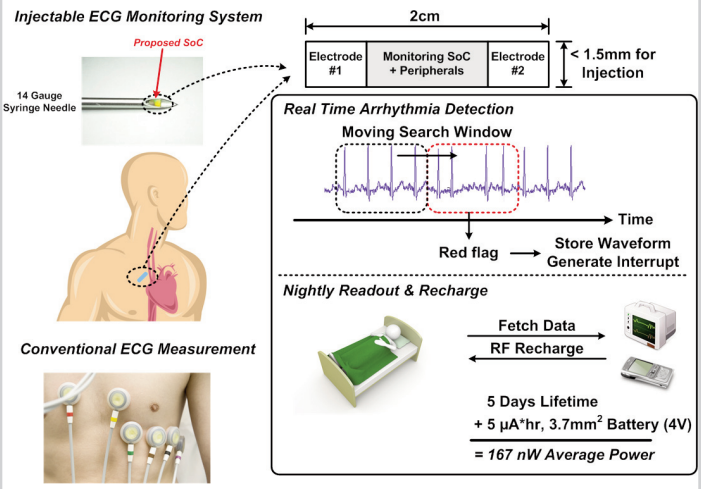


Figure 24.3.1: System overview of ECG monitoring SoC.

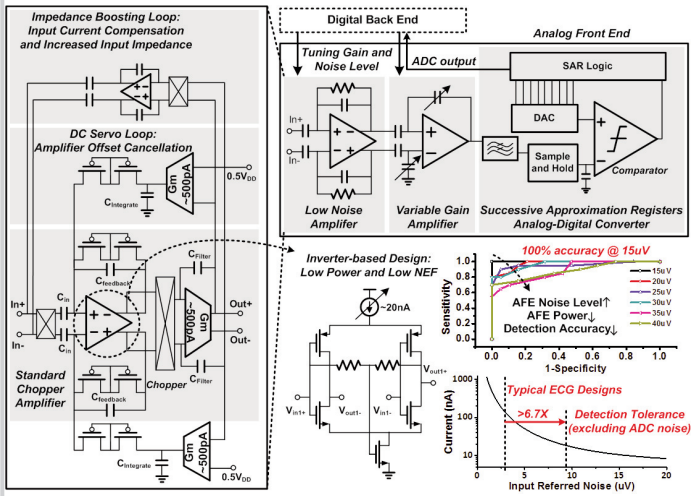


Figure 24.3.2: 31nA analog front-end.

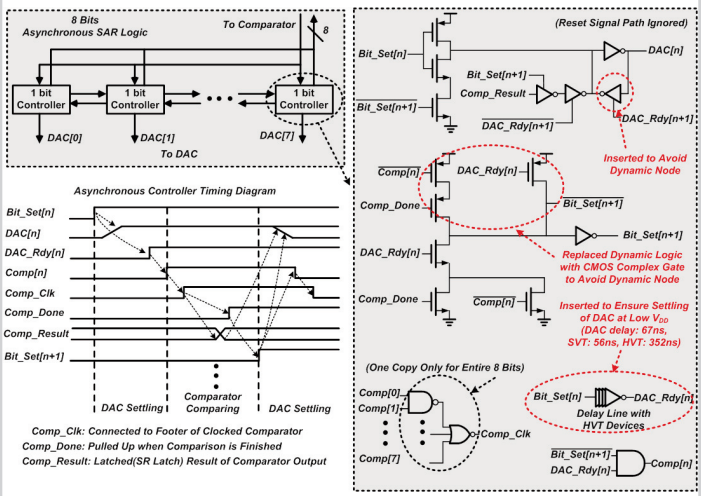


Figure 24.3.3: Robust asynchronous controller for ADC.

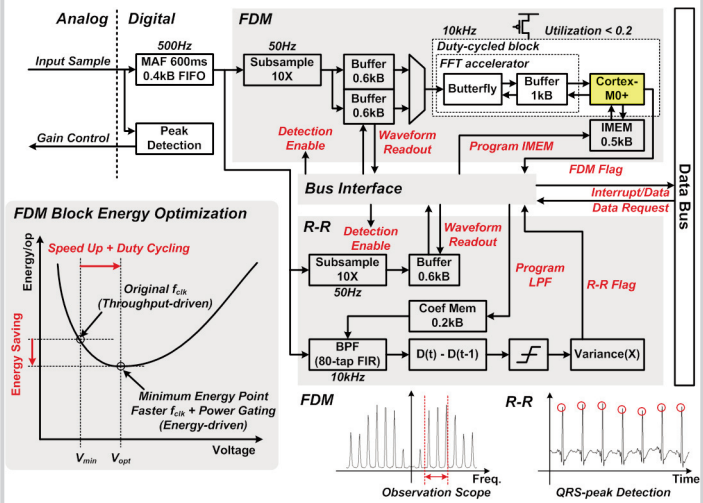


Figure 24.3.4: Digital back-end with two algorithms.

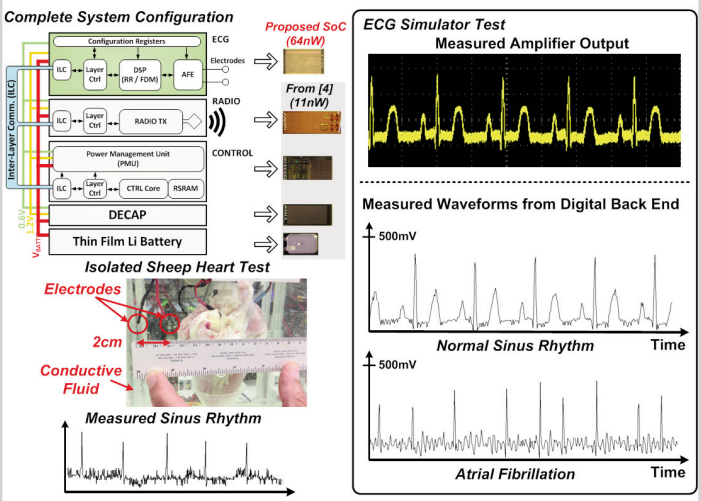
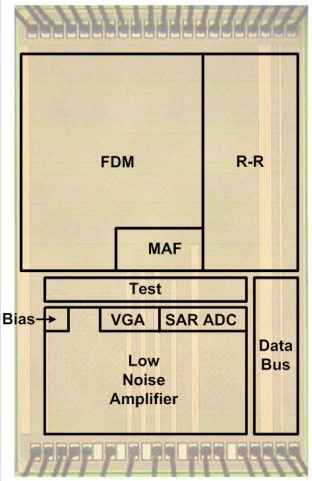


Figure 24.3.5: Complete system and measurement results.

		This Work	ISSCC '12 [5]	VLSI '12 [6]	ISSCC '13 [7]
Target Signals		**ECG**	ECG, EMG, EEG	ECG, VCG, PCG	ECG, Bio-Impedance
Technology		**65 nm**	130 nm	90 nm	180 nm
AFE	V_{DD}	**0.6 V**	1.2 V	0.5 V	1.8 V
	Current	**31 nA**	4 μA	20.44 μA (8-Bit, 2kHz Sampling)	-
	Gain	**51 ~ 96 dB**	40 ~ 78 dB	40 ~ 64 dB	40 ~ 64 dB
	Bandwidth	**250 Hz**	320 Hz	0.5 ~ 1 kHz	0.5 ~ 1 kHz
	Input Referred Noise	**253 nV/√Hz**	-	-	200 nV/√Hz
	ADC Bits	**8 Bits**	8 Bits	8/12 Bits	9.3 Bits (ENOB)
	ADC Sampling Frequency	**500 Hz**	-	250 Hz ~ 100 kHz	-
DSP	V_{DD}	**0.4 V**	0.3 ~ 1.2 V	0.5V (1.0V for SRAM)	- (Analog Signal Processing)
	Power Consumption	**45 nW**	2.1 μW	-	
	Clock Frequency	**10 kHz**	2 kHz ~ 1.7 MHz	25 MHz	
System Total Power Consumption		**64 nW**	6.9 μW	22.6 μW	11.3 μW
Power Calculation Configuration		**AFE + DSP Arrhythmia Detection (FDM)**	AFE + DSP R-R Extraction	AFE (BSI) + DSP + OSC Arrhythmia Detection	AFE (3ch ECG + RA) + ASP + OSC Arrhythmia Detection

Figure 24.3.6: Comparison with recent prior works.



Technology		65 nm
Die Area		1.45 × 2.29 mm^2
AFE	V_{DD}	0.6 V
	Current	28 nA (LNA + VGA) 3 nA (ADC)
	Gain	51 ~ 96 dB
	Bandwidth	250 Hz
	Input Impedance	> 10 MΩ
	Input Referred Noise	253 nV/$\sqrt{Hz}$ (Noise Floor) 6.52 µV (RMS)
	NEF	2.64
	NEF×VDD^2	0.95
	ADC Bits	8 Bits
	ADC Sampling Frequency	500 Hz
DSP	V_{DD}	0.4 V
	Clock Frequency	10 kHz
	Total Memory	3.7 kB
	Power Consumption	45 nW (FDM) 92 nW (R-R)
	Main Processing Units	ARM Cortex-M0+ 16-b 512-pt RV FFT 80-tap FIR

Figure 24.3.7: Die photo with summary table.