Characterization of Heavy-Ion-Induced Single-Event Effects in 65 nm Bulk CMOS ASIC Test Chips

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***Abstract*—Two 65 nm bulk complementary metal-oxide-semiconductor (CMOS) digital application-specific integrated circuit (ASIC) chips were designed, and then tested in a heavy ion accelerator to characterize single-event effects (SEE). Test chip 1 incorporates test structures, and test chip 2 implements an unhardened and a hardened digital signal processing (DSP) core. Our testing results reveal the radiation effects on the low-voltage and high-frequency operations of the ASIC chips. At a low supply voltage of 0.7 V, cross sections increase by a factor of 2 to 5 at low linear energy transfer (LET), while the increase in cross section at high LET is almost negligible, suggesting that the charge conveyed by heavy ion has far exceeded the critical charge and tuning the supply voltage is not effective. Increasing the clock frequency increases the relative importance of single-event transients (SET) compared to single-event upsets (SEU), especially in hardened designs due to their better SEU immunity. The hardened DSP core experiences a factor of 2 increase in cross section when its clock frequency is increased from 100 MHz to 500 MHz.**

***Index Terms*—Error-resilient design, radiation hardening, single-event effect, single-event transient, single-event upset, soft error.**

I. Introduction

SINGLE-EVENT EFFECTS (SEE), including single-event upset (SEU), multiple bit upset, single-event transients (SET), and latchup, present a major challenge to the function and reliability of integrated circuits in spaceflight systems [1], [2]. Research has been conducted in the past to characterize SEE [3], [4], and overcome SEE through circuit design, e.g., by increasing the critical charge, or Q_{crit}, through upsizing and circuit topology [5], by adding circuitry to prevent upsets following temporal or logical masking principles [6], [7], or by adding redundant information for error checking [8], [9].

A comprehensive heavy-ion radiation experiment of 180 nm to 28 nm flip-flops shows that as CMOS technology scales, D flip-flop SEU cross sections decrease and approach those of the hardened flip-flops [10]. Without additional layout spacing, the difference between unhardened and hardened flip-flops is narrowing. Therefore it is plausible to use unhardened flip-flops in deep submicron ASIC designs to achieve better area and energy efficiency. The effect of supply voltage and clock frequency on 28 nm flip-flops and combinational circuits [11] were investigated in an alpha particle radiation experiment. Two important conclusions were drawn: (1) the supply voltage has a strong impact on the alpha particle SEU of flip-flops, while the combinational circuits are relatively unaffected by supply voltage variations, and (2) the clock frequency has a much stronger impact on SET compared to SEU [12]. Therefore low-voltage and high-frequency chips will most likely incur higher error rates due to both SEU and SET.

This work is motivated by the goal of designing a deep submicron bulk complementary metal-oxide-semiconductor (CMOS) application-specific integrated circuit (ASIC) chip for a satellite application. The application places tight constraints on power consumption and silicon area, requiring circuits of the minimum area and power, so a commercial ASIC design flow with no extra layout spacing was explored to reduce power and area.

To establish a proof of concept and to mitigate risks, we designed two test chips that were fabricated in a Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm bulk CMOS technology. Chip 1 contains common ASIC building blocks, including unhardened flip-flops of different sizes, and custom-designed hardened dual-interlocked storage cell (DICE) flip-flops [13], [14] and triple modular redundant (TMR) flip-flops [15], and various combinational depths and sizes. Chip 2 contains two digital signal processing (DSP) cores, one built using unhardened flip-flops and the other using hardened DICE and TMR flip-flops. Heavy-ion radiation testing was carried out at the Texas A&M University K500 superconducting cyclotron facility [16]. Our measurements cover an array of heavy ions from neon to gold for chip 1 and from helium to silver for chip 2. The two test chips allow us to characterize SEE at both circuit and system level.

Recent studies have demonstrated the radiation effects of 65 nm and sub-65 nm CMOS circuits [10], [11], but the heavy-ion testing results are not entirely available. This work fills in the blanks, e.g., voltage scaling effect in heavy-ion testing, which is important for low-power operations. We also evaluate the effectiveness of common radiation hardening techniques in a heavy-ion radiation environment to show the vulnerabilities of hardened designs, e.g., hardened storage cells could be more error sensitive due to the change of clock frequency than unhardened ones.

The rest of this paper is organized as follows. In Section II, we review the design of the two test chips and the radiation test

Manuscript received February 07, 2014; revised April 29, 2014; accepted July 10, 2014. Date of publication August 19, 2014; date of current version October 09, 2014. This work was supported by the National Aeronautics and Space Administration (NASA) and Defense Advanced Research Projects Agency (DARPA) under cooperative agreement HR0011-13-2-0006.

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Digital Object Identifier 10.1109/TNS.2014.2342872

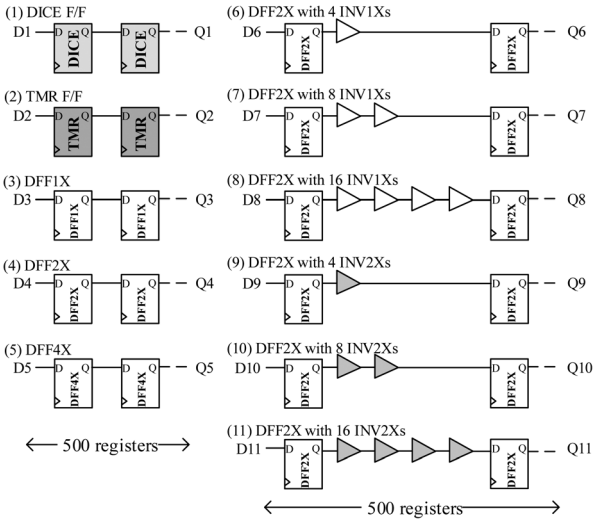

Fig. 1. Shift register chains implemented on test chip 1. Each chain consists of 500 flip-flops. Chain 6 to 11 each has a varying number and size of inverters.

setup. Chip 1 results are presented in Section III to show circuit design considerations including redundancy, sizing, combination depth and sizing, and input patterns. The voltage and frequency test results of both chips are summarized in Section IV, showing the effect of supply voltage on SEE, and the clock frequency effect on the relative importance of SEU and SET. Conclusions are presented in Section V.

II. Test Chip Designs and Test Setup

Two test chips were designed and fabricated in a TSMC 65 nm bulk CMOS process. Chip 1 was dedicated to characterizing SEE on basic ASIC chip building blocks, including unhardened and hardened flip-flops, and to isolate the effects of supply voltage, sizing, combinational and sequential circuits. The testing was done at a 50 MHz clock frequency to allow for probing of each individual test structure.

Chip 2 is a synthesized ASIC chip based on standard cells. The purpose of chip 2 is to characterize SEE of a practical ASIC chip at the system level. The testing was done at two clock frequencies, 100 MHz and 500 MHz, and two supply voltages, 1.0 V and 0.7 V, to study the effects of clock frequency and supply voltage on the SEE in a unhardened DSP core and a hardened DSP core. The results from both test chips are related to draw conclusions on the protection against heavy ion impact by redundancy and to identify voltage and frequency dependency.

A. Test Chip 1

Test chip 1 measures 1.2 mm $\times$ 1.5 mm in size, and it contains 11 independent shift register chains, each consisting of 500 stages of D flip-flops as shown in Fig. 1. Chain 1 and 2 are built using DICE [13], [14] and TMR flip-flops [17], respectively. DICE, shown in Fig. 2(a), is a dual redundant flip-flop that prevents an upset on any one node from propagating and corrupting the stored bit. TMR flip-flop, shown in Fig. 2(b), uses three copies of storage and majority vote to enhance the protection against any single upset. Following [14], the spacing between

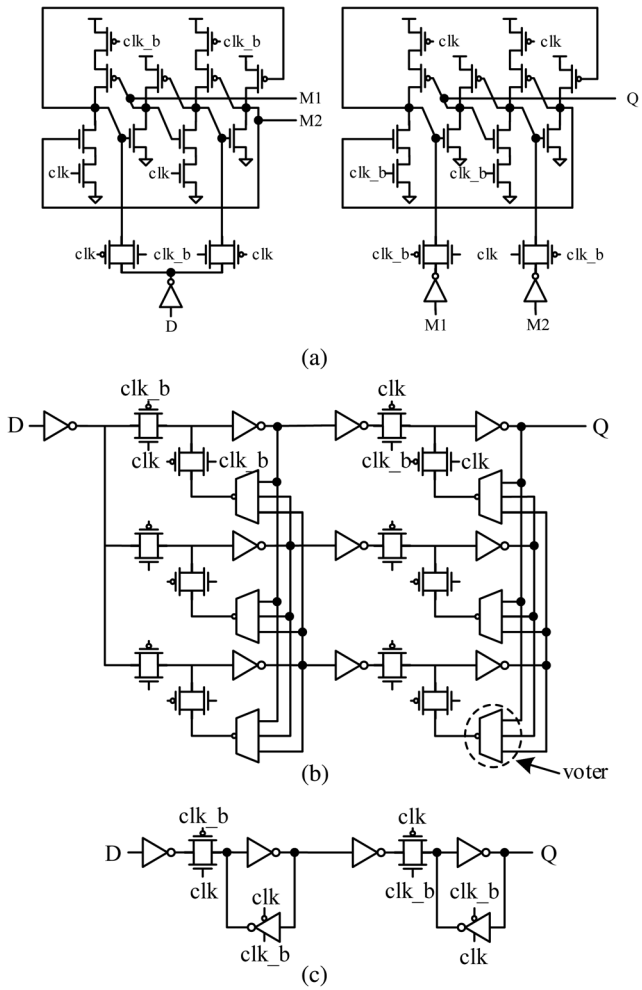

Fig. 2. Three types of D flip-flops: (a) DICE flip-flop [13], [14], (b) TMR flip-flop [17], and (c) unhardened D flip-flop.

critical nodes in the DICE flip-flop is 1.5 μm. The spacing between the closest pair of redundant nodes in the TMR flip-flop is 2.4 μm, and the spacing between the second closest pair of redundant nodes is 3 μm. These hardened flip-flops are evaluated against unhardened flip-flops available in a commercial standard cell library that make up chain 3, 4 and 5, where the flip-flops in chain 3 are minimum sized (DFF1X) and those in chain 4 and 5 are upsized using DFF2X and DFF4X cells respectively. Upsizing increases Q_{crit} but also increases charge collection area.

To investigate SET, we insert inverters in chain 6 to 11. Specifically, in chain 6, 7 and 8, minimum sized inverters (INV1X) are used, and the combinational logic depth is varied by having 4 inverters per shift register stage in chain 6, 8 inverters in chain 7, and 16 inverters in chain 8. Deeper combinational logic increases the collection of SET. When an SET is propagated and sampled by a flip-flop, it results in an error. In chain 9, 10 and 11, upsized INV2X inverters are used. Upsizing combinational circuits increases Q_{crit}, but also increases SET collection. As commonly done in standard cell based designs, body contacts are placed at regular intervals. In our designs, body contacts are placed every 20 μm. These test structures

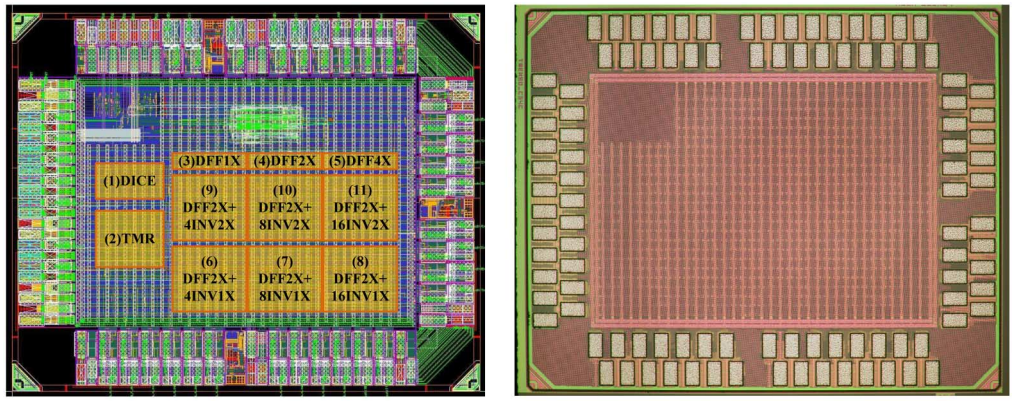

Fig. 3. (a) Test chip 1 layout, and (b) microphotograph.

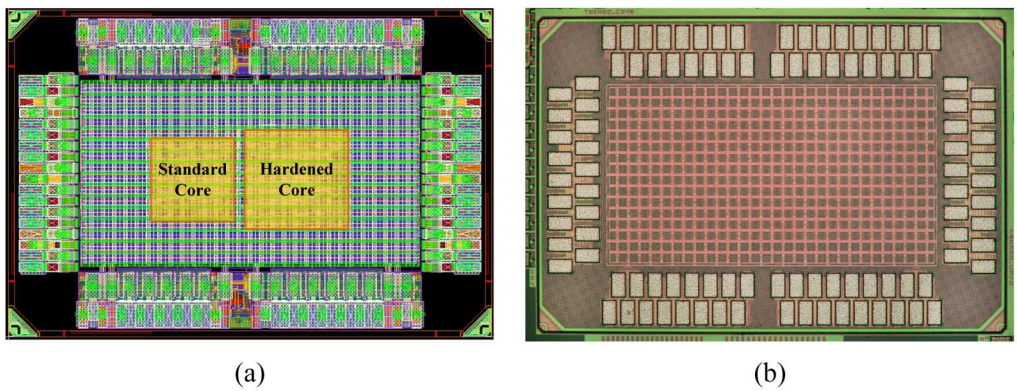

Fig. 4. (a) Test chip 2 layout, and (b) microphotograph.

allow us to investigate SET and SEU, as well as the impact of sizing and depth of combinational circuits.

The layout and microphotograph of test chip 1 are shown in Fig. 3. In implementing the test structures, we first construct chain 11 as the baseline; then replace the INV2X cells with INV1X cells to make chain 8; remove every other inverter to make chain 10; and so on. In this way, we construct chain 6 to 11 using an identical footprint, thus the impact due to layout difference is minimized. Similarly, chain 3 to 5 also share an identical footprint. The empty space is filled with tie cells (body contacts), supply decoupling cells, and filler (empty) cells. The area outside the test structures is filled with tie cells, filler cells and power and ground routing.

B. Test Chip 2

Test chip 2 measures 1.5 mm × 1.0 mm in size, and it consists of two DSP cores, an unhardened core and a hardened core, that compute cross-correlations. Test chip 2 was developed as part of the geostationary synthetic thinned aperture radiometer (GeoSTAR) project [18], [19] led by the Jet Propulsion Laboratory. Each DSP core computes the cross-correlations of 5 inputs with another set of 5 inputs every clock cycle, and accumulates the correlations for 10 ms. Following each 10-ms integration cycle, the correlation values are read out, and the values are reset for the next integration cycle.

Test chip 2 was synthesized using standard cells of logic gates and flip-flops. The unhardened core uses unhardened flip-flops, while the hardened core incorporates custom-designed hardened DICE flip-flops for datapath and TMR flip-flops for control to provide stronger SEE protection. The layouts of DICE and TMR flip-flops were drawn to ensure adequate spacing between sensitive nodes. These standard cells were used as the basic units for synthesis, place and route. Test chip 2 provides self test capability by generating test vectors on chip using linear feedback shift registers (LFSR). The layout and microphotograph of test chip 2 are shown in Fig. 4. The unhardened core measures 0.28 mm × 0.28 mm and the hardened core is 0.33 mm × 0.33 mm. The area outside the cores is filled with tie cells, filler cells and power and ground routing.

C. Test Setup

The ion beam testing was carried out in two 16-hour windows. In ion beam testing, a test chip is mounted on a test board that is connected to a field-programmable gate array (FPGA) board using a high-speed connector. During the radiation testing, the lids of the test chips are removed and the chips are fully uncovered as shown in Fig. 5. We ran test chip 1 at 50 MHz, a relatively low clock frequency. The FPGA is clocked by the same 50 MHz clock source so it remains synchronous with the test chip. The FPGA provides constant 0 and constant 1 inputs to each of the 11 shift register chains

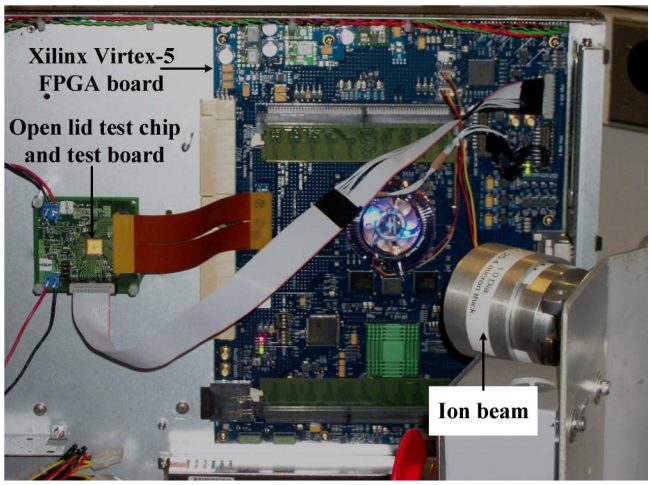

Fig. 5. Radiation test setup.

in chip 1, and it records the outputs of the shift register chains and checks for errors. Error counters are accumulated in the FPGA. Each test run lasts 3 billion clock cycles, or 1 minute. After each test run, the error counters are downloaded from the FPGA through a serial interface, and the ion beam or the beam angle is changed before the next run.

Our test structure in chip 1 supports testing using dynamic input patterns, but even infrequent upsets on the clock tree will result in errors enabling and disabling the flip-flops in the long shift register chain, resulting in very unreliable bit error count. If the clock signal of one flip-flop is incorrectly disabled for one cycle, the output sequence may look completely different, resulting in a very high bit error count. The long 500-stage shift register chain is good for collecting upsets for a characterization study, but not representative of a practical datapath pipeline that is usually much shorter. Therefore, we tested chip 1 with only static input patterns, so that the clock tree upsets are masked. In chip 2, the two DSP cores are tested using dynamic test vectors generated on chip. It is a practical setup that captures the effect of dynamic input patterns.

Test results are expressed in cross section per bit across a range of linear energy transfer (LET) values. Cross section represents the upset susceptibility, or more specifically, the number of upsets per unit ion fluence. Cross section per bit can be interpreted as the upset rate per unit ion fluence, i.e.,

$$\sigma(\mathrm{LET}) = \frac{N}{M\Phi} \tag{1}$$

where σ is cross section per bit as a function of LET, N is the number of observed upsets, M is the number of flip-flops or bits, and Φ is the time-integrated flux or fluence.

The average flux applied in our tests ranges from 1.17×10^5 to 2.63×10^5 ions/cm^{2}s for chip 1, and from 2.76×10^5 to 1.42×10^6 ions/ cm^{2}s for chip 2. The ions used and their LET values are listed in Table I.

Chip 2 was tested at a 100 MHz and a 500 MHz clock frequency using random input vectors generated by on-chip LFSRs. Each test run consists of 10,000 10-ms integration

TABLE I
IONS APPLIED IN RADIATION TESTING AND THEIR NOMINAL LET

Ion	LET(MeV-cm^2/mg)	Ion	LET(MeV-cm^2/mg)
He	0.106	Kr	36.2
N	1.4	Ag	44.5
Ne	2.8	Xe	54.7
Ar	8.9	Au	88.4

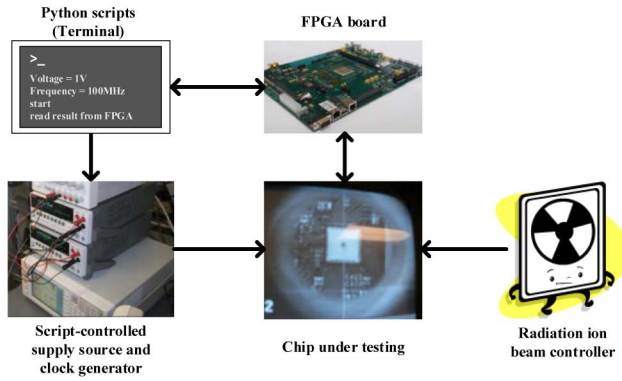

Fig. 6. Illustration of automated testing of chip 2.

cycles, each followed by a readout. The continuous testing requires frequent readouts from the ASIC. To automate the testing, we used a Python script to pre-compute the expected outputs in each run and store them in the memory on FPGA before each run. The Python script also controls the supply voltage and clock frequency of the ASIC. Unlike in the test of chip 1, the FPGA clock is not synchronized with the chip 2 clock. To start each 10-ms integration cycle, the FPGA activates a set of control signals to chip 2, and chip 2 will then run independently of the FPGA. The FPGA polls the status of the integration complete signal from chip 2. Upon detecting integration complete, the FPGA checks the ASIC outputs for errors by comparing with the pre-computed expected outputs stored in memory. An error is recorded if any bit in a set of cross-correlation values is wrong. Error counters are accumulated before another integration cycle is initiated. Each test run consists of 10,000 10-ms integration cycles, or 1 minute and 40 seconds. After each test run, the error counters are downloaded from the FPGA, and the ion beam or the beam angle is changed before the next run. The automated test setup is illustrated in Fig. 6.

An error recorded in the radiation testing of chip 2 can be caused by a single SEE occurrence or multiple occurrences during a 10-ms integration cycle. The error count is an indication of the effect of SEE on this particular DSP core over a given time period, rather than a measure of the number of SEE occurrences. We report the test chip 2 results in cross section per bit by normalizing the number of errors by the number of flip-flops in the design and the fluence over the integration cycle as in equation (1). The reported cross section per bit is lower than the actual number of SEE occurrences as multiple upsets would only be seen as one. However, it is a reasonable estimate since in most of the integration periods, we had no or very few errors.

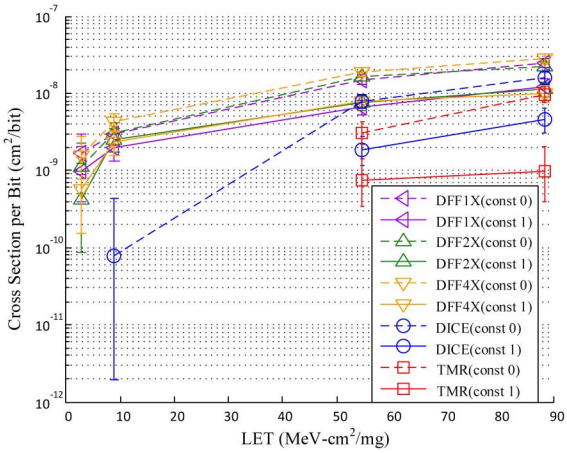

Fig. 7. Cross section per bit with ion energy for unhardened, DICE and TMR flip-flops.

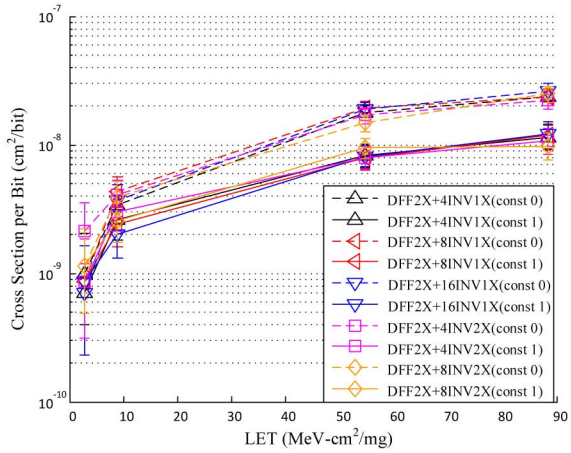

Fig. 8. Cross section per bit after adding combinational circuits.

III. Circuit Design Considerations

Circuit design choices, including circuit topology, sizing, and logic depth, determine the circuit's radiation tolerance. The test structures in chip 1 are subject to the same radiation environment, and the cross sections are compared in Fig. 7.

A. Radiation Hardening by Redundancy

Radiation-hardened DICE [13], [14] and TMR flip-flops [17] are commonly used in spaceflight systems to offer better protection against SEE. In low-LET neon (2.8 MeV-cm^2/mg) and argon (8.9 MeV-cm^2/mg) testing of chip 1, DICE and TMR flip-flops provide at least one order of magnitude improvement in cross section per bit compared to the unhardened D flip-flops as shown in Fig. 7. At higher LET levels (above 50 MeV-cm^2/mg), DICE and TMR become less effective, which is partly due to the lack of additional layout spacing between redundant storage nodes [10] and partly due to the increasing multiple bit upsets. Heavier ions such as xenon (54.7 MeV-cm^2/mg) and gold (88.4 MeV-cm^2/mg) deliver much more energy and likely induce more multiple bit upsets [20], making DICE and TMR less effective at high LET levels.

In general, scaling makes DICE and TMR less effective because scaling shrinks the circuit layout and redundant copies in DICE and TMR are physically placed closer to the primary copy [10]. Therefore it becomes more likely for both the redundant and primary copies to be affected by a particle strike, especially at high LET levels. To make DICE and TMR more effective, redundant copies need to be placed further apart for isolation at the cost of area. Cell interleaving [21], [22] is a promising approach, but it adds extra overhead for metal routing. The extra and longer wiring increases the average capacitive loading, resulting in a higher power consumption, longer delay, and lower clock speed.

B. Increasing Critical Charge by Upsizing

Scaling reduces device sizes and the critical charge, or Q_{crit}, required to hold a logic level, making circuits more vulnerable to SEE [23]. Previous work suggests that upsizing increases Q_{crit} and immunity against soft errors because of larger capacitance on storage nodes. Upsizing also increases the device drive strength, which helps error recovery [5]. However, we observe in the testing of chip 1 that the difference in cross section per bit between DFF1X, DFF2X and DFF4X is negligible, as shown in Fig. 7, which is contrary to previous beliefs. One explanation is that increasing Q_{crit} and drive strength to improve upset immunity is counteracted by the larger drain areas to collect charge.

The weak dependence of cross section on Q_{crit} is also a result of the amount of charge injected by heavy ions that is much higher than the Q_{crit} even with moderate upsizing. When the charge injected is comparable to Q_{crit}, the minimum charge needed for an upset, we expect increasing Q_{crit} by upsizing to play a stronger role. However, in a deep submicron bulk CMOS design where Q_{crit} is very low, upsizing is ineffective and inefficient.

C. Depth and Sizing of Combinational Circuits

Combinational circuits also contribute to errors through SET. If a SET of a long enough duration happens to be sampled, an error is registered. A SET often does not lead to errors, as the SET can be electrically attenuated along the path (electrical masking), or is blocked from propagating due to off-path inputs (logical masking), or the SET arrives too late to be sampled by the flip-flop (temporal masking). For these reasons, the cross section due to SET depends on logic design and topology, sizing, and timing. With all the masking effects, it is unclear whether SET is an important factor in determining the cross section.

We evaluate the effect of SET using shift register chains incorporating inverters of various sizes and stages in test chip 1. A longer and upsized chain increases the SET collection area, but also allows the SET to be more electrically attenuated due to higher capacitance and longer path. The results in Fig. 8 show that the cross section per bit is almost independent of the depth and sizing of combinational circuits, and adding combinational circuits results in no significant increase in cross section per bit. SEUs still dominate in the 50 MHz testing of chip 1.

Past work pointed out that increasing transistor density can reduce SET cross section by up to 70% compared to a low-density circuit [24]. Therefore, chain 8 and 11 in our test chip 1 may have fewer SET-induced errors compared to chain 6 and 9. However, at a 50 MHz clock frequency, SET-induced errors

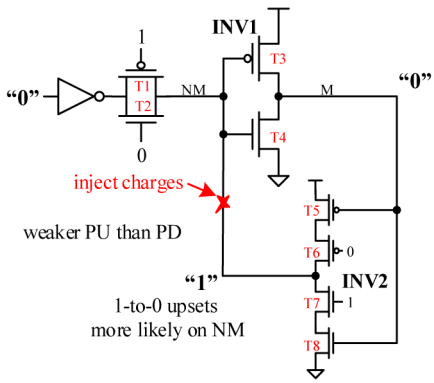

Fig. 9. Latch design results in unequal upsets.

are much less significant compared to SEUs [11], [12], and the effect of density on the cross sections is not noticeable as shown in Fig. 8.

Note that as a simple combinational circuit, an inverter chain does not offer any logical masking. In a realistic combinational circuit with logical masking, the cross section due to SET will be lower. Second, in a relatively low frequency 50 MHz testing, the temporal masking [25] has downplayed the importance of SET, as the slow sampling misses most of the SETs of a short duration. In Section IV.B, we will compare the chip 1 test results to the high frequency chip 2 test results to evaluate the effects of temporal masking and also account for logical masking in realistic combinational circuits.

D. Data Dependence

The cross section per bit is dependent on the test pattern: more upsets occur in constant data 0 testing compared to constant data 1 testing as shown in Fig. 7, suggesting 0-to-1 upsets are more likely than 1-to-0 upsets. This result is consistent among all shift registers chains and across LET levels higher than 30 MeV-cm^2/mg. Some previous work has also recorded this behavior in the testing of flip-flops [4], [26], [27].

The unequal cross sections are found to be a result of the latch design and sizing in the master-slave flip-flops. The two cross-coupled inverters in the latch schematic illustrated in Fig. 9 are sized differently, resulting in unequal drive strength. The tristate inverter in the feedback path (INV2) is stacked and weak. As a result, the output of INV2, node NM, which holds the inverted input, is more likely to be affected by charge injection compared to node M. Further, INV2 has a relatively stronger pull-down than pull-up and it holds 0 at its output node NM better than 1, making 1-to-0 upsets on NM more likely and causing more data 0 upsets for the latch.

The cross section of P- and N-diffusion is another factor behind the unequal upsets. Previous study shows that P-diffusion has a lower cross section than N-diffusion [23]. Therefore, N-diffusion will collect more charge, contributing to 1-to-0 upsets on NM. This effect is less pronounced at node M as T3 is sized larger than T4, resulting in a larger P-diffusion area connected to node M that offsets the cross section difference between P- and N-diffusion.

E. Angle Effects

Due to the limitation of the setup and the way that the ASIC board is connected to the FPGA board, we were only able to change the tilt angle at a fixed 90° roll angle for chip 1, and change the tilt angle at a fixed 0° roll angle for chip 2. We observe that increasing the tilt angle for chip 1 has no consistent effect on the chip 1 results, but increasing the tilt angle for chip 2 increases its cross sections. The difference is attributed to the roll angles. Standard cells are placed in rows. At a 90° roll angle, the ion beam path is perpendicular to the standard cell rows, while at a 0° roll angle, the ion beam path is parallel to the standard cell rows, making multiple bit upsets more likely.

F. Latchup and Total Ionization Dose

Compared to the recent reports on latchup in deep submicron processes [28]–[31], latchup was not observed in our testing. There are three possible reasons to explain the absence of latchup in our testing: (1) the supply voltage in our testing was 1.0 V or 0.7 V, low enough that latchup may never occur. In [28]–[31], a nominal 1.2 V supply voltage was used; (2) our testing was done at room temperature (20°C); and (3) tie cells (body contacts) are placed at regular intervals and extra tie cells are used as fillers in our designs. Our results also indicate that the two 65 nm test chips built in a bulk CMOS process are immune to total ionization dose (TID) effects above 100 krad(Si) TID. TID effects such as thresholds shifts, latchup events or permanent damages have been a problem in older CMOS technology nodes. Chip 1 and chip 2 were tested up to a TID of 634 krad(Si) and 1950 krad(Si), respectively with no noticeable degradation in the chip functionality, performance or power consumption.

IV. Voltage and Frequency Dependence

Supply voltage and clock frequency are two primary knobs to adjust the performance and power consumption of an ASIC chip. Voltage and frequency scaling also have direct implications on SEE. We evaluate the supply voltage effect using the test structures in chip 1 and the two DSP cores in chip 2, and the frequency effect by comparing chip 2 results at 100 MHz and 500 MHz.

A. Supply Voltage Scaling

Supply voltage scaling reduces Q_{crit} and makes circuits more vulnerable to upsets. Fig. 10 shows a consistent increase in cross section per bit for the unhardened, DICE and TMR flip-flops when the supply voltage is reduced from 1.0 V to 0.7 V. The effect of reducing supply voltage is more noticeable at low LET levels and in DICE and TMR flip-flops, but the difference becomes much narrower at high LET levels. Attempts to increase Q_{crit} by increasing the supply voltage have little effect at high LET levels because the injected charge by the heavy ions is already much higher than Q_{crit}.

The results of 100 MHz dynamic testing of chip 2 at 1.0 V and 0.7 V are illustrated in Fig. 11. The hardened DSP core equipped with DICE flip-flops for datapath and TMR flip-flops for control exhibits an order of magnitude lower cross section per bit than the unhardened DSP core at low LET levels, but the difference is diminished at high LET levels. Voltage scaling makes a less

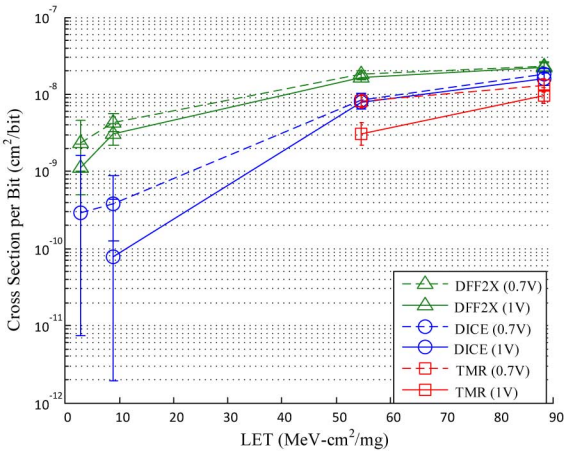

Fig. 10. Cross section per bit of D flip-flop, DICE and TMR flip-flops at supply voltage of 1.0 V and 0.7 V.

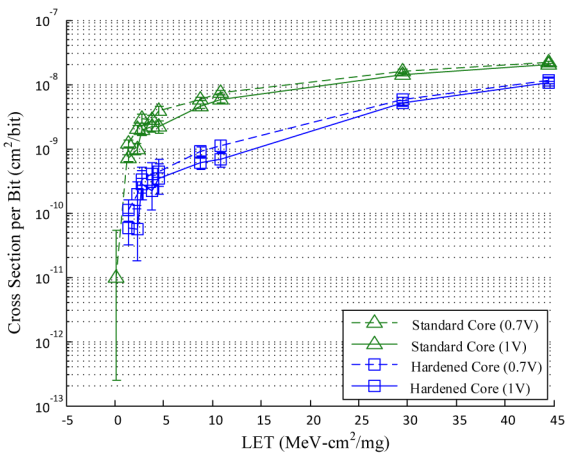

Fig. 11. Cross section per bit of unhardened and hardened DSP cores at supply voltage of 1.0 V and 0.7 V (clock frequency of 100 MHz).

pronounced difference, and the difference also becomes negligible at high LET levels, which agrees with the test chip 1 results above. The insight confirms that supply voltage scaling does not necessarily lead to a large increase in cross section, making it a viable option for power reduction in spaceflight ASIC chips if a small increase in cross section is acceptable.

B. Clock Frequency Effects

Clock frequency affects the cross section following two mechanisms: at a high frequency, frequent sampling causes more SET-induced errors; at a lower frequency, fewer SETs are registered (known as temporal masking), but flip-flops need to retain data for a longer period, which makes them more vulnerable to SEUs. Frequency shifts the relative importance of SET and SEU. SEU dominates at a lower frequency, and more SET-induced errors are expected at a higher frequency.

The results of chip 2 frequency testing are shown in Fig. 12. In the unhardened DSP core, increasing the clock frequency from 100 MHz to 500 MHz has little effect at low LET levels, indicating the dominance of SEU at low LET, a phenomenon also observed in the 50 MHz testing of chip 1. At high LET

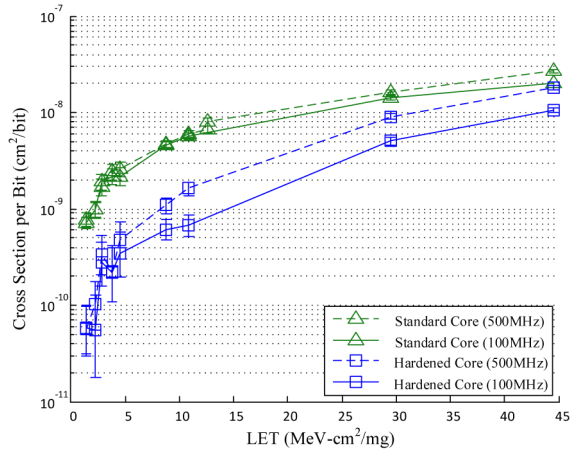

Fig. 12. Cross section per bit of unhardened and hardened DSP cores at 100 MHz and 500 MHz (1.0 V supply voltage).

levels, the cross section per bit at 500 MHz is slightly higher than at 100 MHz, which is attributed to the combined effect of more SETs under high energy particle impact and high frequency sampling that causes more SET-induced errors.

The hardened DSP core shows a stronger frequency dependence than the unhardened core across a wide range of LET levels. The DICE and TMR flip-flops in the hardened core offer a better protection against SEUs, thus the SEU is noticeably lower than in the unhardened core, especially at low LET levels. Increasing the clock frequency in the hardened core causes SET-induced errors to become relatively more significant.

The high frequency test results suggest that hardening flip-flops alone is insufficient for ASIC chips operating at 100 MHz or higher clock frequency. SET-induced errors play an important role at a high clock frequency, and it is necessary to incorporate techniques to detect and overcome SET for the complete protection.

V. Conclusion

We evaluate SEE using two 65 nm bulk CMOS ASIC test chips. Test chip 1 contains shift register chains as test structures to evaluate the effectiveness of hardening, sizing, and the relative influence of SET. Test chip 2 contains DSP cores to evaluate the impact of SEE on system errors.

Our test results show the heavy-ion radiation effect on the low-voltage and high-frequency operations of the ASIC chips. At a low supply voltage of 0.7 V and low LET, the cross sections of flip-flops and DSP cores increase by a factor of 2 to 5. At high LET, the increase in cross sections is almost negligible, suggesting that the charge conveyed by heavy ion strikes has far exceeded the critical charge and tuning the supply voltage is ineffective. Increasing the clock frequency increases the relative importance of SET especially in hardened designs due to their better SEU immunity. The cross section of the hardened DSP core increases by a factor of 2 when its clock frequency is increased from 100 MHz to 500 MHz, whereas the cross section of the unhardened DSP core increases by a much smaller amount at a higher clock frequency. The results from chip 1 agree with chip 2, confirming the validity of the findings.

ACKNOWLEDGMENT

The authors would like to thank Chris Ruf, Darren McKague, Todd Gaier and Alan Tanner for advice and leading the GeoSTAR project that sponsored the radiation testing. They acknowledge the help by Thomas Chen, Roger Backhus, Eric Cameron and Sterling Whitaker for support of the radiation testing, Farokh Irom for help with CREME and interpreting radiation test results, and Michael Flynn, Dennis Sylvester and Keith Bowman for suggestions.

REFERENCES

[1] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.

[2] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, 2005.

[3] T. Karnik, P. Hazucha, and J. Patel, "Characterization of soft errors caused by single event upsets in CMOS processes," *IEEE Trans. Depend. Secure Comput.*, vol. 1, no. 2, pp. 128–143, 2004.

[4] P. Roche *et al.*, "A commercial 65 nm CMOS technology for space applications: Heavy ion, proton and gamma test results and modeling," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 2079–2088, Aug, 2010.

[5] V. Joshi, R. R. Rao, D. Blaauw, and D. Sylvester, "Logic SER reduction through flip flop redesign," in *Proc. Int. Symp. Quality Electron. Design*, 2006.

[6] A. Ejlali, B. M. Al-Hashimi, M. T. Schmitz, P. Rosinger, and S. G. Miremadi, "Combined time and information redundancy for SEU-tolerance in energy-efficient real-time systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 4, pp. 323–335, 2006.

[7] J. Furuta, C. Hamanaka, K. Kobayashi, and H. Onodera, "A 65 nm bistable cross-coupled dual modular redundancy flip-flop capable of protecting soft errors on the C-element," in *Proc. IEEE Symp. VLSI Circuits*, 2010, pp. 123–124.

[8] Y.-H. Huang, "High-efficiency soft-error-tolerant digital signal processing using fine-grain subword-detection processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 2, pp. 291–304, 2010.

[9] B. Shim and N. R. Shanbhag, "Energy-efficient soft error-tolerant digital signal processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 4, pp. 336–348, 2006.

[10] N. Gaspard *et al.*, "Technology scaling comparison of flip-flop heavy-ion single-event upset cross sections," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4368–4373, Dec. 2013.

[11] N. Mahatme *et al.*, "Impact of supply voltage and frequency on the soft error rate of logic circuits," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4200–4206, Dec. 2013.

[12] N. Mahatme *et al.*, "Analysis of soft error rates in combinational and sequential logic and implications of hardening for advanced technologies," in *Proc. IEEE Int. Rel. Physics Symp.*, 2010, pp. 1031–1035.

[13] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[14] P. Hazucha *et al.*, "Measurements and analysis of SER-tolerant latch in a 90-nm dual-VT CMOS process," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1536–1543, 2004.

[15] D. G. Mavis and P. H. Eaton, "Soft error rate mitigation techniques for modern microcircuits," in *Proc. IEEE Int. Rel. Physics Symp.*, 2002, pp. 216–225.

[16] Radiation effects facility [Online]. Available: http://cyclotron.tamu.edu/ref/

[17] Single-event effect mitigation in RTAX-DSP spaceflight FPGAs [Online]. Available: http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtax-dsp

[18] B. Lambrigtsen *et al.*, "GeoSTAR-a microwave sounder for geostationary satellites," in *Proc. IEEE Int. Geosci. Remote Sens. Symp.*, 2004, vol. 2, pp. 777–780.

[19] A. Tanner *et al.*, "Initial results of the geostationary synthetic thinned array radiometer (GeoSTAR) demonstrator instrument," *IEEE Trans. Geosci. Remote Sens.*, vol. 45, no. 7, pp. 1947–1957, 2007.

[20] J. D. Black *et al.*, "HBD layout isolation techniques for multiple node charge collection mitigation," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2536–2541, Dec. 2005.

[21] H.-H. K. Lee *et al.*, "LEAP: Layout design through error-aware transistor positioning for soft-error resilient sequential cell design," in *Proc. IEEE Int. Rel. Physics Symp.*, 2010, pp. 203–212.

[22] S. Baeg, S. Wen, and R. Wong, "SRAM interleaving distance selection with a soft error failure model," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2111–2118, Aug. 2009.

[23] P. Hazucha, C. Svensson, and S. A. Wender, "Cosmic-ray soft error rate characterization of a standard 0.6-um CMOS process," *IEEE. J. Solid-State Circuits*, vol. 35, no. 10, pp. 1422–1429, 2000.

[24] N. M. Atkinson *et al.*, "Effect of transistor density and charge sharing on single-event transients in 90-nm bulk CMOS," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2578–2584, Dec. 2011.

[25] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Proc. Int. Conf. Dependable Syst. Netw.*, 2002, pp. 389–398.

[26] D. Rennie *et al.*, "Performance, metastability, and soft-error robustness trade-offs for flip-flops in 40 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1626–1634, 2012.

[27] G. Gasiot *et al.*, "Experimental soft error rate of several flip-flop designs representative of production chip in 32 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4226–4231, Dec. 2013.

[28] J. M. Hutson *et al.*, "The effects of angle of incidence and temperature on latchup in 65 nm technology," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2541–2546, Dec. 2007.

[29] J. M. Hutson *et al.*, "Evidence for lateral angle effect on single-event latchup in 65 nm SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 1, pp. 208–213, Feb. 2009.

[30] N. Dodds *et al.*, "Selection of well contact densities for latchup-immune minimal-area ICs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3575–3581, Dec. 2010.

[31] N. Dodds *et al.*, "Effectiveness of SEL hardening strategies and the latchup domino effect," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2642–2650, Dec. 2012.