An Injectable 64 nW ECG Mixed-Signal SoC in 65 nm for Arrhythmia Monitoring

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***Abstract*—A syringe-implantable electrocardiography (ECG) monitoring system is proposed. The noise optimization and circuit techniques in the analog front-end (AFE) enable 31 nA current consumption while a minimum energy computation approach in the digital back-end reduces digital energy consumption by 40%. The proposed SoC is fabricated in 65 nm CMOS and consumes 64 nW while successfully detecting atrial fibrillation arrhythmia and storing the irregular waveform in memory in experiments using an ECG simulator, a live sheep, and an isolated sheep heart.**

***Index Terms*—Analog front-end (AFE), asynchronous logic, capacitive feedback chopper stabilized instrumental amplifier (CCIA), electrocardiography (ECG), fast Fourier transform (FFT), implantable system, kickback noise, minimum energy point (MEP), mm^3.**

I. Introduction

ELECTROCARDIOGRAPHY (ECG) is the record of electrical activity in the heart and serves as a critical source of information for the diagnosis and study of many heart disorders. Arrhythmia is one of the most prevalent heart diseases. In particular, according to a 2010 National Institutes of Health report [1], 2.7 million people suffer from atrial fibrillation (AF), which is the most common type of arrhythmia, and the number of people impacted continues to increase over time [1].

In ECG waveform with AF, normal-shaped peaks (dubbed QRS complexes) corresponding to the ventricles are seen, but with an irregular rhythm, but the peaks corresponding to the atrial activity (dubbed P waves) are either abnormal in shape and/or size, appear at fast irregular rates and/or non-discrete. Therefore, by monitoring the rate and shape irregularities on the ECG, AF can be detected. However, arrhythmia can occur very rarely (e.g., only a few times a day) with each event lasting only a handful of seconds. Consequently, in arrhythmia studies and treatment, long-term but fast observation is essential to assess the abnormality and its severity [2].

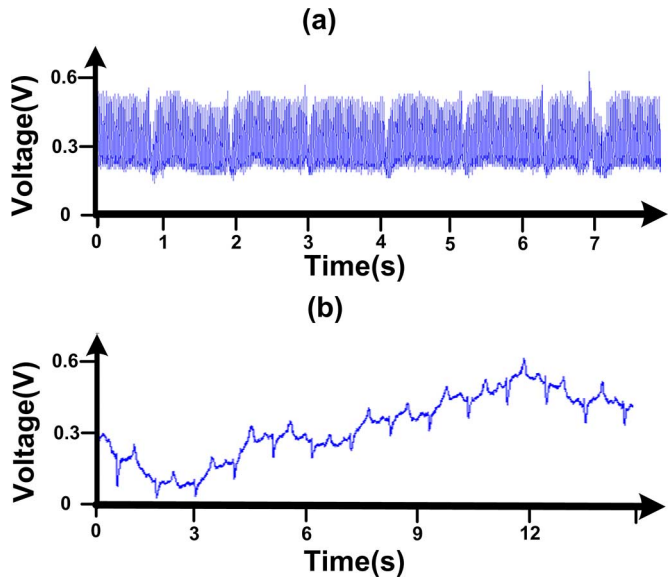

Fig. 1. (a) ECG waveform showing 60 Hz interfering noise as recorded by proposed system. (b) Sheep ECG waveform suffers from low-frequency drift (measured by proposed system). Note that the gain is reduced by 10× in this measurement.

To enable ECG monitoring, body-wearable systems are a widely used solution for long term observation. Two or more of patches are attached to the skin and connected to a body-wearable device for continuously monitoring the ECG and storing the waveform on demand. However, there are some challenges in arrhythmia monitoring when using such an approach. First, even small body-wearable systems severely impact a patient's everyday life. Second, physical contact between patches and the skin can suffer from impedance changes due to body movement, which results in low frequency baseline wander of the output voltage, degrading signal quality and even saturating the amplifier [3]–[5]. Third, the signals captured using such systems are prone to coupled noise from outside sources such as 60 Hz noise from power lines. Example ECG waveforms showing interference from 60 Hz noise and exhibiting low-frequency wandering are shown in Fig. 1.

In contrast, implanted systems can be an attractive alternate solution; modern devices have a form factor roughly comparable to a USB flash drive [6]. Since these devices are inserted

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under the skin, the impact on patient daily life is dramatically reduced once installed. This approach also offers stable physical contact between electrodes and the tissue. The signal strength and quality degradation due to the smaller electrode spacing relative to a surface patch-based recording approaches is compensated by subcutaneous embedding and proximity to the heart, yielding similar signal quality to wearable devices as will be shown later. Moreover, the subcutaneous device is less susceptible to noise sources outside the body. However, the major drawback of implanted systems is the need for expensive and risky surgery. Device lifetime is also critical and is often required to be several years; as a result, a large battery and low power system are needed. To extend lifetime for both body wearable and implantable systems, there has been a significant focus on low-power ECG systems, for example, in [7]–[15].

To address this set of challenges, this paper proposes a small form-factor syringe-injectable ECG recording and analysis device targeted primarily at atrial fibrillation arrhythmia monitoring. The device can be injected under the skin near the heart using a syringe needle to avoid surgery while retaining the benefits of an implantable system.

The paper is organized as follows. Section II provides an overview of the system. Section III describes the analog front end while Section IV discusses the digital back end of the system. Section V presents the result of several experiments using the proposed system. Section VI then concludes the paper.

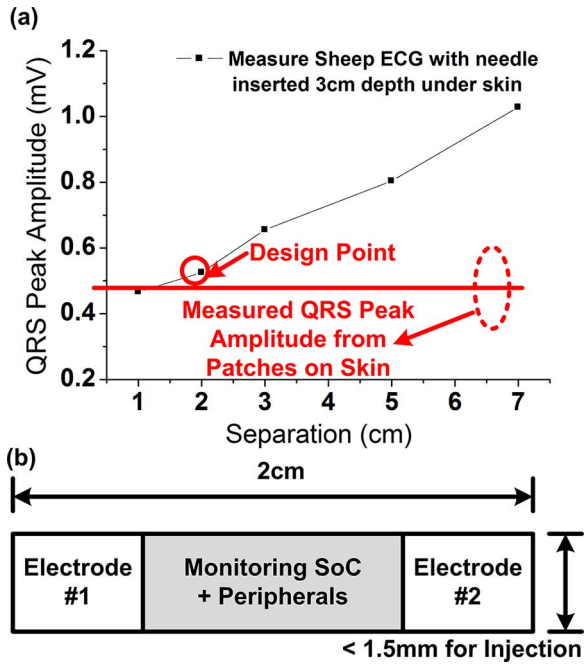

Fig. 2. (a) Measured QRS peak amplitude versus electrode (use needles as the electrodes directly) separation under the skin in a sheep experiment. Note that with $>$ 2 cm separation, the amplitude is larger than the traditional approach with two patches attached to neck and wrist. (b) Dimensions of the proposed system.

II. Overview of the System

A. Dimension of the System

System size is determined as follows: to achieve a syringe-implantable design, the entire system must pass through the 14-gauge syringe needle during the implantation. Hence, the device width is limited to 1.5 mm. In contrast, the length is less constrained and the two electrodes attached to either side of the device require 2 cm separation [Fig. 2(a)] in order to provide sufficient separation to yield an acceptably large potential difference. The target dimensions of the proposed system are shown in Fig. 2(b).

Furthermore, the size constraint also severely limits battery size and hence its capacity. Therefore, in contrast to surgically implanted devices such as pacemakers with large batteries, the proposed device is designed for daily wireless recharging, enabling a much smaller battery. While the patient sleeps, a host station [depicted in Fig. 3(a)] near the bed could recharge and retrieve the stored data through a wireless channel. The lifetime between recharging is set to be five days to provide a safety margin. Matching battery size to device size allows for a 5 μA$\cdot$hr, 3.7 mm^2 Li battery, which constrains system power consumption to be less than 167 nW. This represents a challenging power constraint given that comparable systems in the literature typically consume 1–30 μW [7]–[14].

B. System Overview

The proposed ECG monitoring SoC is 1.4 mm wide and consumes 64 nW while continuously monitoring for arrhythmia. The ability of the system is focus on low power consumption and arrhythmia monitoring depends in part on efficient algorithms. The system consists of analog signal acquisition and digital back end blocks. The signal from electrodes is filtered, amplified, and converted to the digital domain by an analog front end (AFE). A digital signal processing (DSP) module analyzes the waveform within a 10-s search window and detects abnormal cardiac events. Whenever an abnormal event is detected, the device stores the current search window waveform ($10\times$ down sampled) into local memory; it can then be transferred to an external device through means such as a wireless transceiver for further analysis by clinicians. It is also compatible with other ultralow-power sensor node peripherals as shown in Fig. 3(b) [16].

III. Implementation of the AFE

Fig. 4 shows the AFE top level block diagram. The AFE consists of three blocks: a low-noise instrumentation amplifier (LNA), a variable-gain amplifier (VGA), and a successive approximation register analog-to-digital converter (SAR ADC). To reduce power consumption, the AFE supply voltage is 0.6 V and all building blocks except the ADCs clocked comparator are biased in the subthreshold regime for low power and high current efficiency. Note that the low supply voltage may incur non-linearity in the final output signal, especially in the amplifier stage. However, based on simulation results final arrhythmia detection is unaffected with $<$ 3.5% (THD) nonlinearity. Therefore, the nonlinearity design target is set to 3% for the AFE to best balance system performance and power consumption.

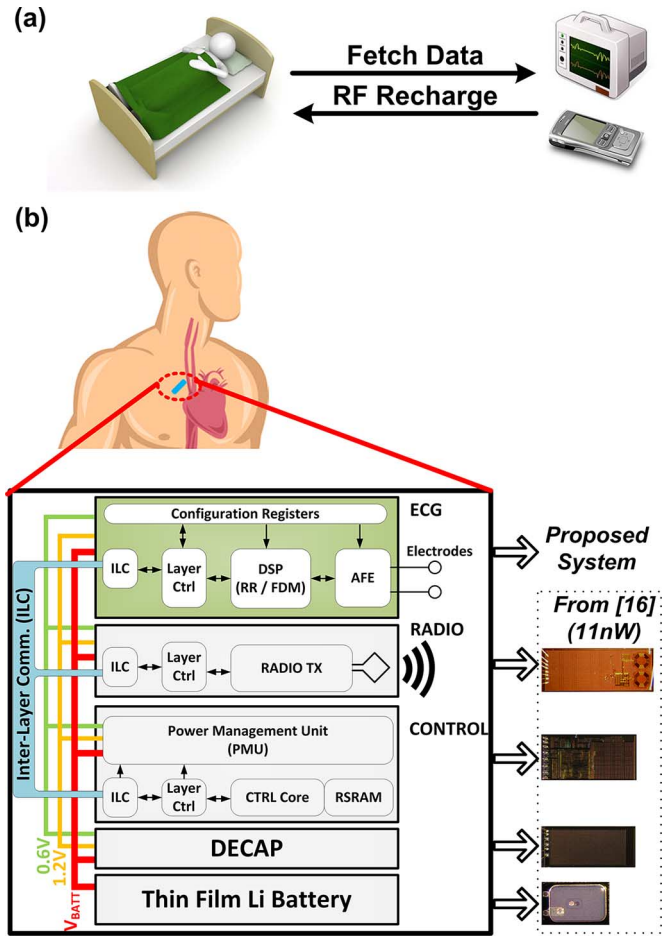

Fig. 3. (a) Proposed nightly readout and recharge of the system. (b) Other required peripheral.

A. Noise Specification

Similar to other noise-limited amplifier designs [17], the total power consumption of the analog front end is dominated by the first stage of the LNA. Typical ECG designs usually target extremely low input referred noise level [around 3 μV [18], [19]; see the red dashed line in Fig. 5(a)] for best signal quality. However, due to the direct relationship between current consumption and input referred noise, this leads to currents of larger than 100 nA assuming a noise efficiency factor (NEF) of 3 and 500 Hz bandwidth. In order to reduce total power, we optimize amplifier performance by observing its impact on the final proposed arrhythmia detection accuracy. The effect of noise levels on the accuracy of binary classification between atrial fibrillation and normal sinus rhythm was assessed by applying our atrial fibrillation detection algorithms [20] (see Fig. 14 and Section IV-B below) on the collected ECG waveforms with artificial additive white Gaussian noise (AWGN) at various levels (from 0 to 40 μV). The collected ECG waveforms were collected from 40 un-discriminated patients that were referred to the University of Michigan hospital for diagnosis and treatment of atrial fibrillation and the noise levels added was designed to surpass the typical ECG noise level [ECGs were recorded during an EP procedure under supine and sedation condition by an EP-Med System (St. Jude Medical, St. Paul, MN, USA)]. Fig. 5(a) shows that with a relaxed noise constraint, AFE power consumption reduces significantly, but the receiver operating characteristics (ROC) curves in Fig. 5(b) demonstrate that the detection accuracy drops as well. Nevertheless, the proposed system and detection algorithm suffers no performance degradation (100% sensitivity and specificity) with up to 15 μV input-referred noise. As a result, the design is targeted to 15 μV input-referred noise to minimize power consumption while maintaining high atrial fibrillation detection accuracy. In the final design, the amplifier specification is tightened to 10 μV input-referred noise across process corners to allow for a 10 μV ADC noise budget. This optimization reduces AFE power by $6.7\times$ from 132 to 17 nW and system power by $2.45\times$ from 177 to 72 nW, compared with typical ECG signal acquisition designs that require noise levels of $\leq$ 3 μV. Due to the resulting high-performance variability and the possibility of the environmental and process changes, the amplifier gain, bandwidth, and input-referred noise can be adjusted by the digital blocks to maximize the useful signal range.

B. Amplifier Implementation

As shown in the AFE top-level diagram, two amplifiers are used in series to provide low noise and high gain. The first amplifier focuses on low noise while the second amplifier enables tunable gain. Due to the large tissue-electrode impedance (measured to vary from 1 to 5 MΩ across different instances of the same model of electrodes, with $\sim$4 MΩ average) the input amplifier requires very high input impedance. In addition, the signal is located in the flicker noise bandwidth and requires chopper stabilization [21]. Therefore, a capacitive feedback chopper-stabilized instrumental amplifier (CCIA) topology is employed for the first-stage amplifier to ensure high input impedance and low noise. The design targets of the CMRR and PSRR are set to be higher than 80 dB as the standard requirement of the ECG amplifier [18], [19]. The target input impedance is set to be larger than 10 MΩ to have sufficient signal amplitude similar to [22]. The target gain is set to be 72 dB and design to be tunable to provide sufficient gain to amplify the 1 mV peak to peak signal to rail-to-rail output and tunable dynamic range. The amplifier also target at handling the dc offset up of the electrodes to 300 mV as required standard [19] by capacitive input. Fig. 6 provides a diagram of the CCIA. The capacitive feedback provides fixed 40 dB gain, and parallel resistive feedback generates the high-pass corner to filter out dc offset and low-frequency drift of the signals. To generate a < 0.5 Hz ultralow high-pass corner with reasonable chip area, a pseudo-resistor is employed.

To further boost input impedance, a positive feedback impedance boosting loop (IBL) similar to [22] is implemented. The IBL generates a current similar to the input current to the core amplifier and feeds it back to the input to compensate the input current and increase the input impedance. The amplifier shown in the figure in the impedance boosting loop serves is design to avoid unwanted signal feeding through the feedback path. Since the input of the amplifier in the IBL is an amplified signal, this amplifier is not noise limited. Therefore, 500 pA is allocated with little impact on the overall power budget.

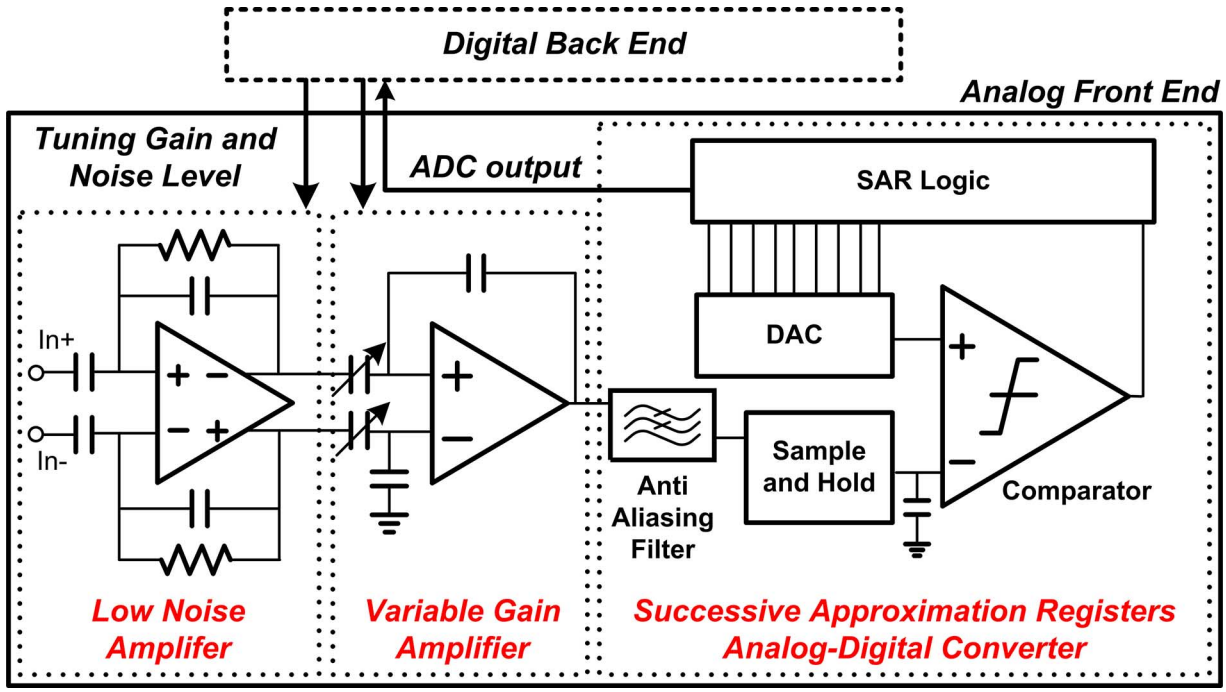

Fig. 4. Top-level diagram of the analog front end.

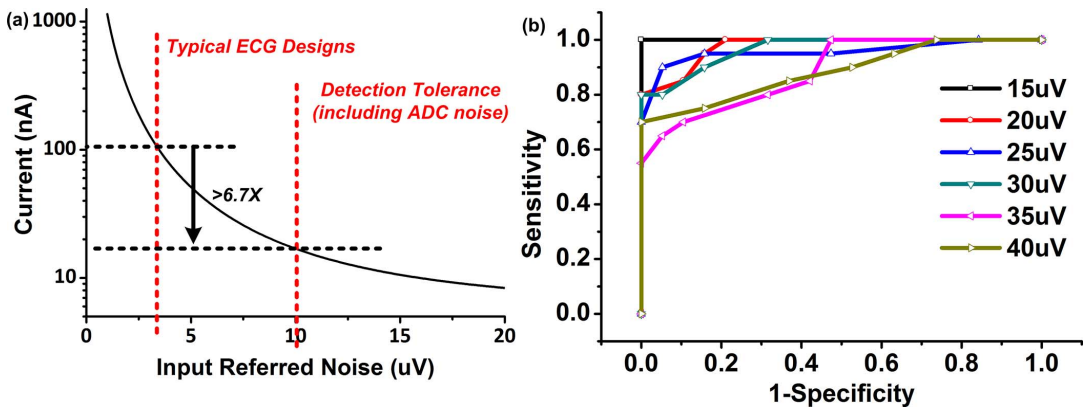

Fig. 5. (a) Tradeoff between amplifier current consumption and input referred noise assumed constant (NEF). (b) The error rate across different noise levels with sweeping threshold. In this plot, the X-axis is true negative rate and the Y-axis is true positive rate. The line pass through $(\mathrm{X}, \mathrm{Y}) = (0, 1)$ shown in the 15 μV case imply that there is a threshold existed without any error in detection. Other line without passing $(\mathrm{X}, \mathrm{Y}) = (0, 1)$ imply there is at least one false alarm when all the a-fib arrhythmia is detected for any possible threshold.

To remove harmonics from the chopper, a Gm-C filter is implemented in the next stage with 250 Hz bandwidth. Note that the chopper is inserted in front of $\mathrm{C_{in}}$ to reduce the mismatch of $\mathrm{C_{in}}$ and improve the CMRR of the amplifier, as in [23].

Fig. 7 shows the core amplifier of the CCIA. The first stage amplifier uses 20 nA current to meet the noise requirement discussed in Section III-A. This current can be tuned by a 4-bit binary code from the digital back end to match the desired noise level (ranging from 3 to 12 μV). To efficiently use the current, an inverter-based amplifier topology, similar to [24], [25], is adopted to achieve low NEF. Common mode feedback is provided by both the bottom NMOS and the pseudo resistors (used to implement a $<$0.1 Hz filter), guaranteeing the output common mode stays at half $\mathrm{V_{DD}}$.

From simulation, the first stage amplifier gain is 32 dB, which is not sufficient to provide the overall 40 dB gain target through the feedback network. Therefore, a second amplifier stage is required within the core amplifier. Since the subsequent amplifier receives an amplified signal, the noise constraint is significantly relaxed; this stage consumes only 500 pA and allows the CCIA to achieve 61 dB gain overall. Simulation results of the CCIA overall gain are shown in Fig. 8.

A common issue with inverter-based amplifier design is vulnerability of the bias point to PVT variations. Therefore, a dc servo loop (DSL), similar to [22], is adopted to stabilize the differential output and reduce offset by fixing the dc output to half $\mathrm{V_{DD}}$. From simulation results, the DSL reduces dc offset from 1.52 to 0.071 mV.

Table I summarizes the performance of the simulated CCIA. The midband gain is 39 dB with 250 Hz bandwidth (limited by the Gm-C filter for the choppers). Through the use of chopping, the impedance boosting loop, and the DSL, all ECG amplifier requirements are met.

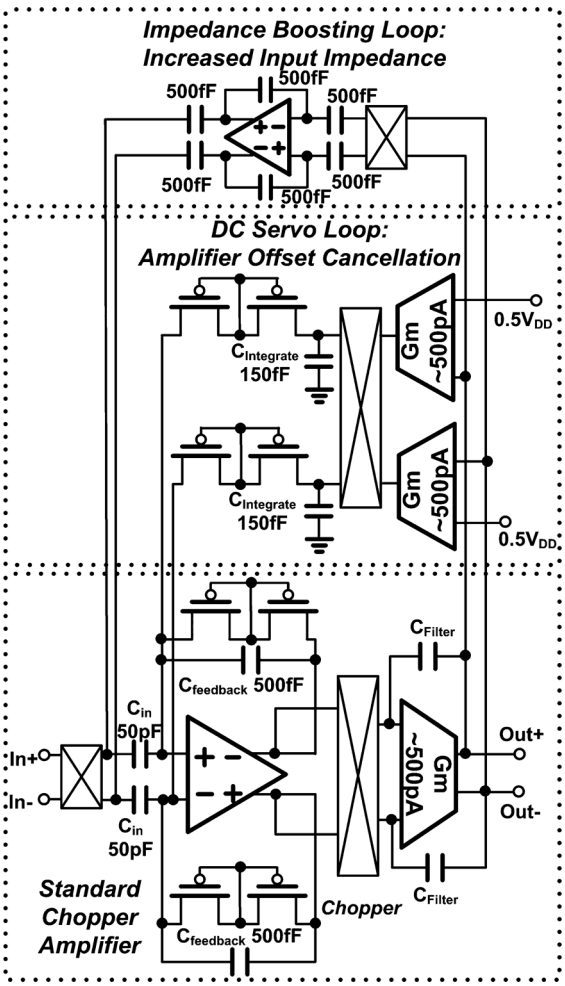

Fig. 6. First stage of the low-noise amplifier, including all building blocks: chopper, dc servo loop, and impedance boosting loop.

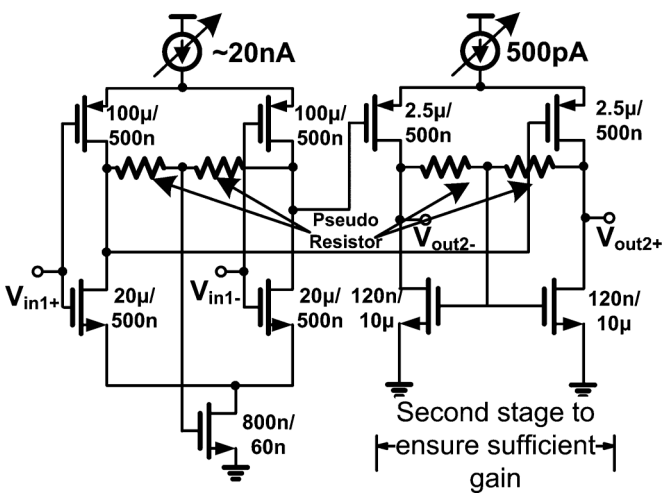

Fig. 7. Core amplifier inside the CCIA.

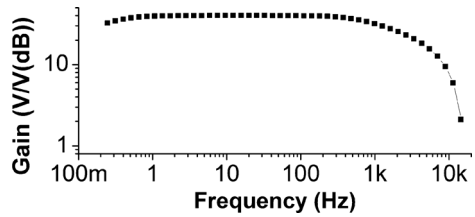

Fig. 8. Simulated CCIA gain versus frequency (without Gm-C filter).

TABLE I
SIMULATED SPECIFICATIONS OF THE CCIA TOGETHER WITH GM-C FILTER

Topology	CCIA
V_{DD}	0.6V
Midband Gain	36.92dB
Input Referred Noise	8.4uV (with chopper)
	5.8uV(without chopper)
Input Impedance	> 110 MΩ (with IBL)
	> 10 MΩ (without IBL)
offset	0.071mV (with DSL)
	1.52mV (without DSL)
Low 3dB	0.117Hz
High 3dB	547.7Hz
NEF	2.258
PSRR	>80dB for < 500Hz
CMRR	>80dB for < 500Hz
THD	2.24%

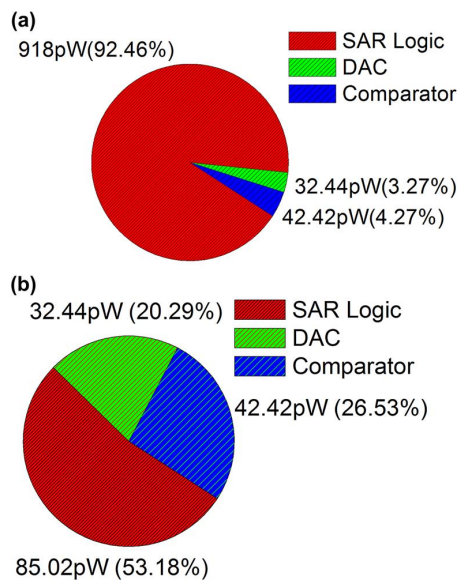

Fig. 9. (a) SAR ADC power breakdown with ADC logic implemented using HVT standard cells. Note that SAR logic consumes 92% of total power when operating at 500 Hz. (b) SAR ADC power breakdown with custom asynchronous logic.

C. ECG SAR ADC Overview

The system's analog to digital conversion is performed by an 8 bit single-ended asynchronous SAR ADC with 500 Hz sampling rate. To avoid alias from other frequency band, a 250 Hz anti-aliasing Gm-C filter is built with a 500 pA amplifier in front of the ADC.

Although SAR ADC consumes less power compared to amplifier in the ECG system, the long term goal of the mm^3 system [16] is to build a platform for all the available sensors. Therefore, the minimizations of the power consumption are conducted

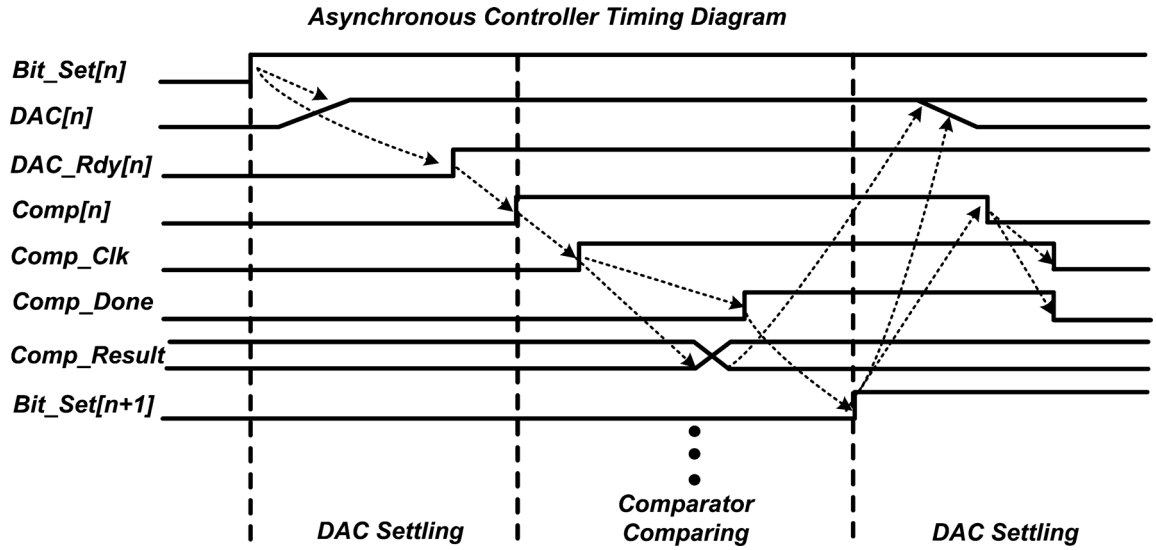

Fig. 10. Detailed signal flow diagram of the asynchronous controller inside the SAR ADC.

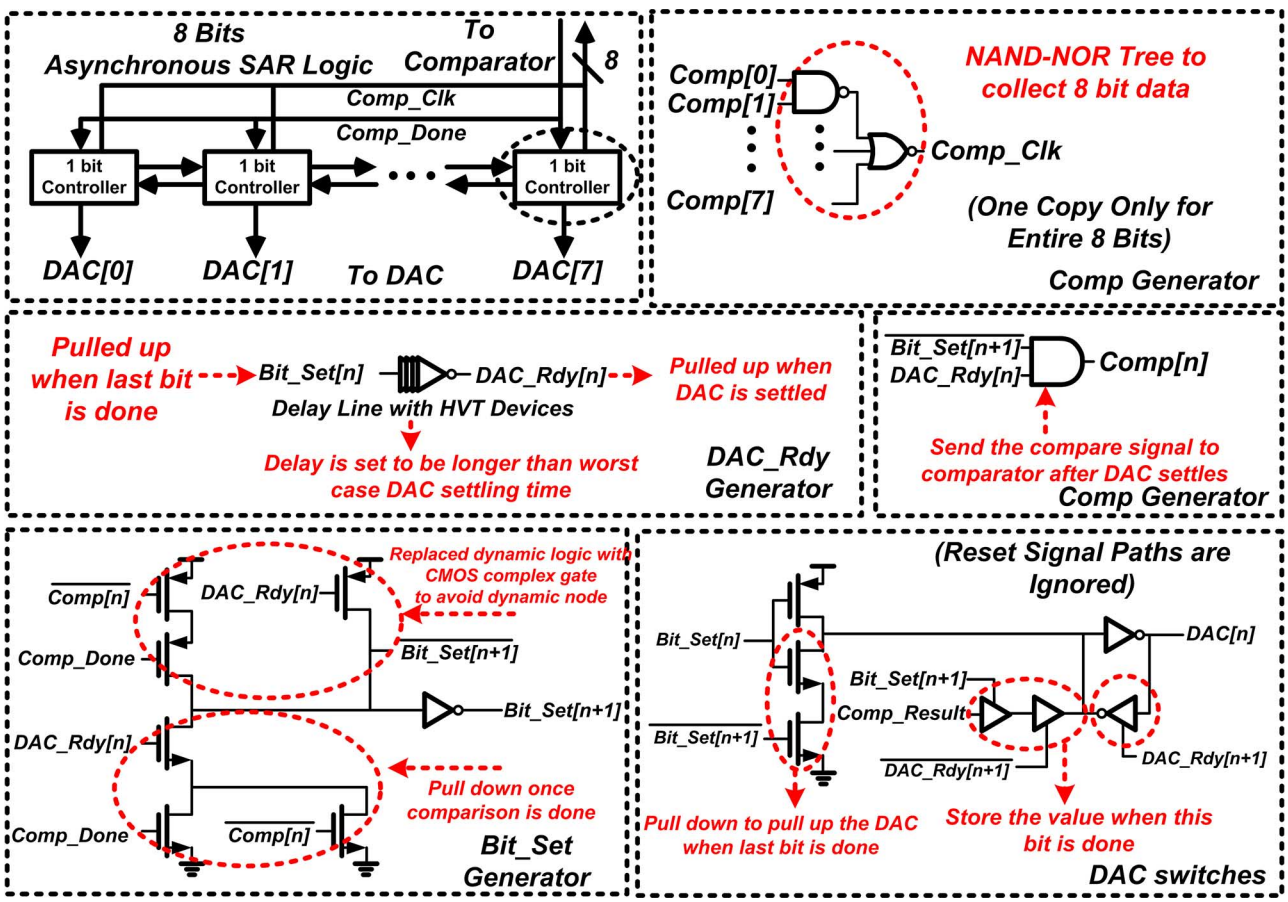

Fig. 11. Detailed diagram of asynchronus logic in the SAR ADC. Note that some of the reset path and the double stacked transistors (to reduce leakage) are not shown.

at each building part separately including the ADC. Power consumption of the SAR ADCs are well studied in recent years. However, most prior work focuses on high sampling rates that far exceed the requirements of this ECG system. Among those SAR ADCs that operate in the kHz range and offer nW-level power consumption [26]–[28], it is found that approximately 50% of total energy consumption comes from digital logic due to leakage and long cycle times. This is in contrast to most SAR ADCs which operate at much higher sample rate and hence have power dominated by DAC switching. The importance of digital logic in this application will be heightened due to the sub-kHz sampling rates; simulated power consumption of a standard 8 b

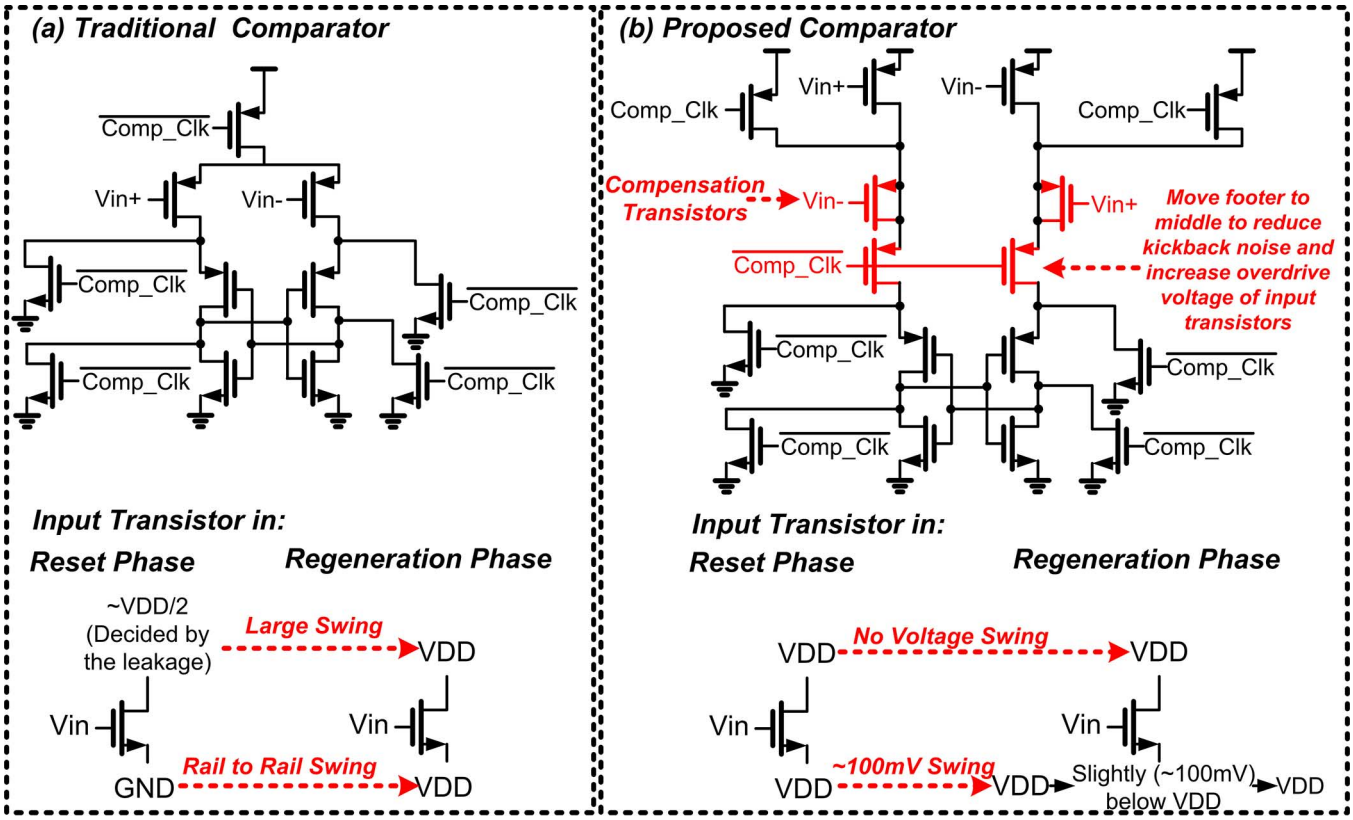

Fig. 12. (a) Traditional comparator and source of kickback noise. (b) Proposed comparator with suppressed kickback noise sources.

500 S/s SAR ADC is shown in Fig. 9(a). Here, standard cells are used for the digital logic and leakage is the main source of power consumption in the digital block.

D. Implementation of SAR Control Logic

To reduce digital power consumption, a novel asynchronous logic is proposed to reduce transistor count and hence the leakage power of SAR logic. Conventional asynchronous logic is typically implemented with dynamic logic to achieve peak energy efficiency [29]. However, dynamic logic is not well suited to low-frequency applications due to leakage. Therefore, in this work, all dynamic nodes are implemented with latches clocked by internal signals and delay lines.

Fig. 10 shows the detailed signal flow of a one-bit controller as an example. There are four internal signals: 1) the "bit_set" signal implies the operation of the previous bit is done; 2) the "DAC" signal is connected to the DAC and toggles the DAC directly; 3) the "DAC_rdy" signal is triggered after the DAC is settled and ready for comparison; and 4) the "comp" signal requests a compare event in the comparator.

Once the result of the last bit comparison is done, the "bit_set" signal is pulled up by the previous stage. The circuit to pull up the "bit_set" signal is shown at the bottom left of Fig. 11. The "DAC" signal is then set to 1 by the circuit shown in the bottom right of Fig. 11 (note that the DAC is set to 0 initially and floating nodes are completely avoided through the use of latches). Once the DAC is settled, "DAC_rdy" goes high. Since direct detection of the DAC settling to 8 bit accuracy would consume significant energy, the circuit triggering the "DAC_rdy" signal is implemented with a delay line set to be longer than the expected DAC settling time across all corners. Since a long delay line can also consume high power, I/O HVT devices are used to reduce the number of stages and save power. Once the DAC has settled, the "Comp" signal goes high and sends a comparator clock signal to trigger the comparison. After the comparison result is generated, "comp_result" and "comp_done" are sent by the comparator. The controller saves the result into the DAC and raises the "bit_set" signal for the next stage.

The transistors count of the proposed design is 34 compared with the 48 transistors of the traditional 2 DFF design, and 29% of reduction is achieved. To further reduce power, all leakage paths are double stacked, reducing subthreshold leakage by $1.92\times$ from 163 to 85 pW. As shown in Fig. 9(b), the proposed asynchronous logic reduces simulated power consumption to 85 pW, marking a $10.79\times$ (from 918 to 85 pW) improvement compared with SAR logic using synthesized standard cells.

E. Implementation of DAC and Comparator

Considering the impact of mismatch [30] and thermal noise on ADC accuracy, a 10 fF DAC unit capacitor and typical split capacitor array topology are chosen. Further, the comparator is a clocked one-stage design that is chosen for its low dynamic power consumption. However, the combination of first stage clocked comparator and small capacitor array make the comparator input vulnerable to kickback noise. The proposed design uses a split footer comparator [31] combined with cross-coupled compensation to address this issue. Fig. 12 shows the schematic of the proposed comparator. Note that the kickback noise mainly

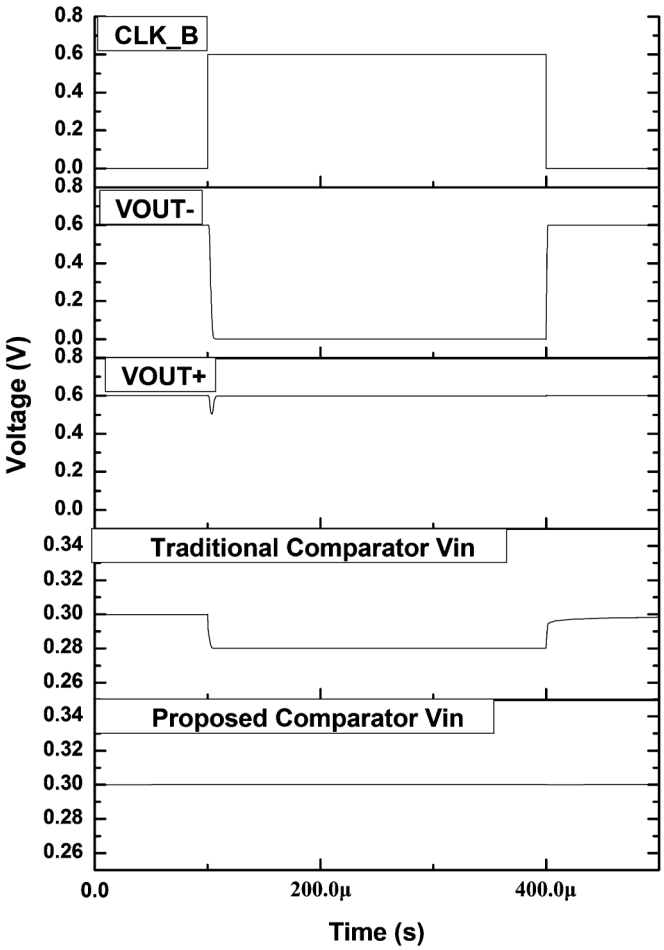

Fig. 13. Simulated waveforms of kickback noise in the proposed and traditional comparators. Kickback noise in the traditional amplifier is 19.8 mV and is reduced to 0.2 mV in the proposed design.

stems from the rapidly change drain and source voltages of the input transistor. In the proposed design, these changes are limited to ∼100 mV and the residual kickback noise is reduced by the compensation transistors. In the simulation results of Fig. 13, the kickback noise is reduced by $84.9\times$ (from 19.8 to 0.2 mV) in the proposed comparator design.

Table II shows the power breakdown of the complete analog block. Note that ADC power is dominated by the anti-aliasing filter due to the use of low-power asynchronous logic.

IV. Implementation of Digital Back End

A. Overview of the Digital Algorithm

The back-end digital block first detects the incoming signal amplitude and tunes AFE gain accordingly to set the waveform to full range. Arrhythmia detection is performed in a moving 10 s window, as shown in Fig. 14(a). Since the irregular session lasts several seconds, there is no overlapping between the windows. If an arrhythmia is detected in a window, the $10\times$ down-sampled 10 s waveform is temporarily stored in the memory and an interrupt signal is sent out for further processing.

The first implemented detection algorithm is conventional time-domain detection [32]. This approach first detects the largest QRS peaks and then calculates the peak-to-peak time interval. The variance of peak-to-peak intervals is then calculated. As the peaks are generated more irregularly during arrhythmia, we apply a simple thresholding technique to the variance to detect an abnormal activity. As a second approach we perform arrhythmia detection in the frequency domain. Under normal conditions, peaks are generated at approximately constant intervals, which translate to a clear dominant frequency and harmonics in the frequency spectrum. However, as shown in Fig. 14(b), under abnormal rhythm, a single dominant frequency is less prominent and the frequency spectrum shows more dispersion. Therefore, under arrhythmia such as atrial fibrillation, peaks have varying intervals in the frequency domain, and the arrhythmia can be detected by inspecting the variance of intervals. The stored 50 Hz sampled waveform is sufficient for detection of fast rhythms such as atrial fibrillation in the frequency domain, where cardiac activation rate is always $<$25 Hz, but it is not suitable for time domain analysis where precision of $<$40 ms is required, such as in sequential QRS intervals detections. Thus, the stored 50 Hz sampled waveforms may not be suitable for some clinical interpretations.

Fig. 15(a) shows an overview of the digital back-end based on the two detection algorithms described earlier. First, input samples taken from the ADC output pass through the moving average filter (MAF) of 600 ms to remove slow baseline wandering by subtracting the output of MAF from the original input to obtain filtered result. At the same time, the circuit sense the input codes from the ADC and tunes the gain such that the swing is within 75% to 90% of the ADC output range. There are two separate processing paths for the frequency- and time-domain algorithms. In the time-domain R-R algorithm, the feature is the distance between adjacent QRS peaks, and it uses the variance of these intervals to detect irregular peaks. The frequency-domain FDM algorithm [20] directly looks at the frequency spectrum and checks if there exists clear peaks which represent constant intervals. Further details are given below in Section IV-C.

B. Implementation of R-R Detection

The proposed design can also perform standard QRS-peak detection [32] (R-R block), which uses peak-to-peak distances to determine ECG signal regularity. The input signal goes through the bandpass filter based on an 80-tap FIR filter. The signal is then differentiated to obtain the slope. If the signal slope exceeds a threshold a QRS peak is declared. The variance of R-to-R intervals is directly used as a decision value in arrhythmia detection. The bus interface can program the algorithms and retrieve the stored data when an arrhythmia is detected. This data is passed to peripherals on the other chips through the data bus. The implemented design allows for one of the two different algorithms to be run, allowing for power savings by power gating the unselected processing path.

C. Implementation of the Frequency Dispersion Metric (FDM)

The proposed FDM detects an arrhythmia in the frequency domain. The input is first down-sampled by $10\times$, and stored in one of two 0.6 kB ping-pong buffers. A 512-point real-valued FFT accelerator is implemented with a radix-4 256-point complex-valued FFT shown in Fig. 16. First, the Blackman–Harris window observing the 3–15 Hz frequency range is applied to the

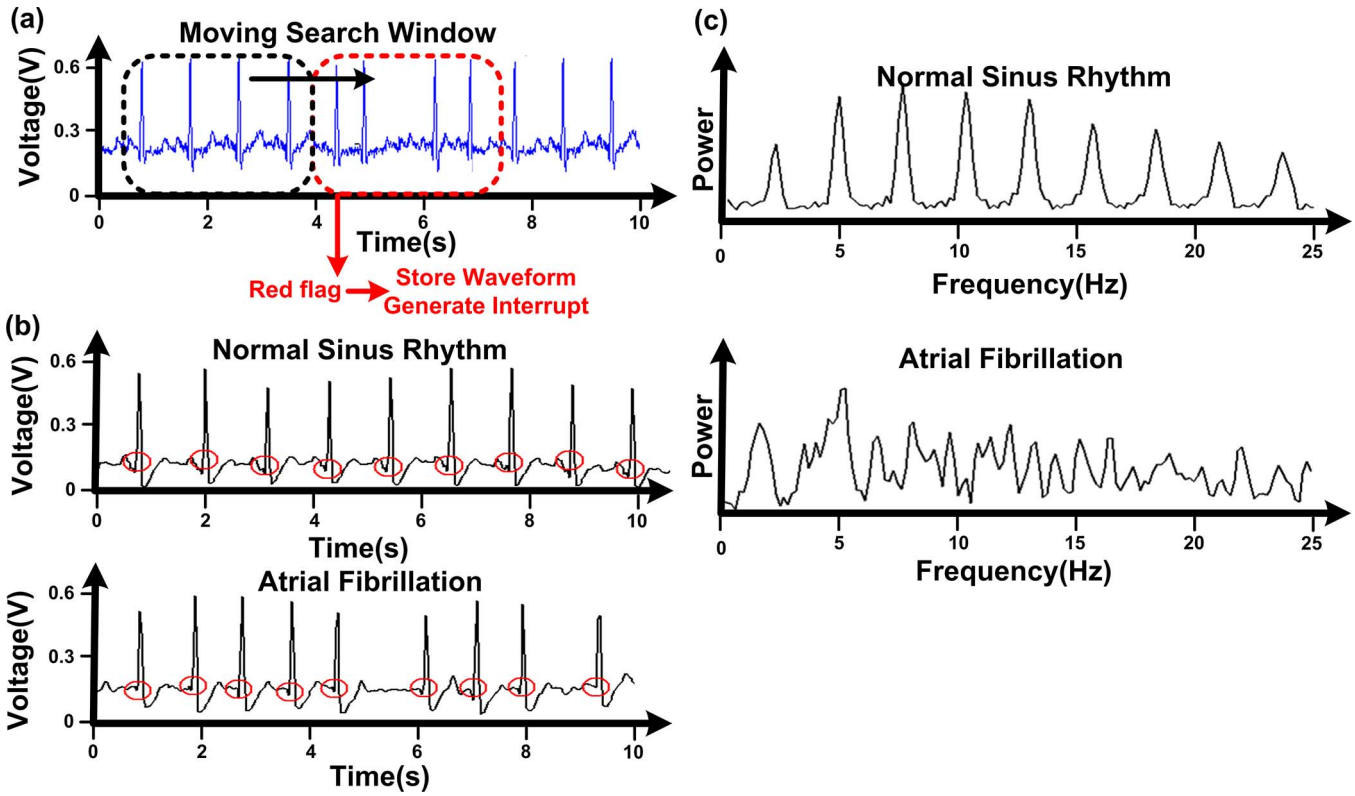

Fig. 14. (a) Search windows of the proposed algorithm. (b) Example waveform of normal ECG waveform and the arrhythmia ECG waveform. (c) Corresponding power spectrum of the ECG waveforms shown in (b). Noted that the block floating point scheme is implemented and the y-axis is showing relative numbers without unit.

TABLE II
SIMULATED POWER BREAKDOWN OF AFE

LNA		12.5nW
LNA	Core: First Stage	10.9nW
	Core: Second Stage	0.3nW
	Impedance Boosting Loop	0.3nW
	DC Servo Loop	0.6nW
	Gm-C Filter	0.3nW
VGA		3nW
SAR ADC		0.46nW
SAR ADC	Anti-Alias Filter	0.3nW
	SAR Logic	85.02pW
	Comparator	42.42pW
	DAC	32.44pW

signal, then the FFT block will calculates the frequency spectrum, and the ARM Cortex-M0+ core performs the actual detection algorithm to observe the existence of the dominant peaks in a specific frequency range, which represents a stable heartbeat. Once an arrhythmia is detected, the ping-pong buffer storing the last search window no longer accepts new samples until the waveform is fully read out through a data bus. During this time, the other buffer acts as the primary input data channel. Therefore, the ping-pong buffers, along with the local buffer of the FFT, make continuous arrhythmia detection possible while temporarily storing any previous abnormal activity. Note that the ARM core instruction memory can be user-programmed to provide added flexibility such as changes to the peak detection algorithm in the frequency spectrum or the frequency monitoring window. To deal with false alarm of changes in the heart rate due to changing levels of activity, since the irregular peaks from arrhythmia usually generate faster and abrupt changes compared with normal changes from changing levels of activity. The algorithms can distinguish it by choosing right decision values in the threshold stage.

D. Optimization for Minimum Energy Computation

To further reduce energy consumption of the FDM block a technique called minimum energy computation [33], [34] is applied. As the supply voltage is lowered both leakage and dynamic power reduce. However, the system clock is slowed, and the leakage energy per cycle increases. Eventually, the leakage energy increase overcomes the dynamic energy savings and total energy starts to increase. Therefore, it has been shown that an optimal point exists, i.e., the minimum point of the plot in Fig. 15(b). In simulation, V_{opt} and V_{min} are 300 and 250 mV, whereas we could achieve the same performance as V_{opt} in simulation at 400 mV in measurement due to discrepancy between simulation and measurement. And the energy per operation is 797 pJ/op at V_{opt}. Arrhythmia detection is done only once in a 10 s window, and each detection takes approximately 500 cycles. Hence, 500 Hz input sampling frequency is sufficient to meet performance constraints and is chosen for the proposed system. However, the minimum supply voltage that matches this frequency constraint lies below the energy optimal point and therefore consumes substantial leakage energy due to the corresponding long cycle time. Therefore, we use a faster (10 kHz) clock and operate the detection in burst-mode (20× faster than required). After the detection event completes the

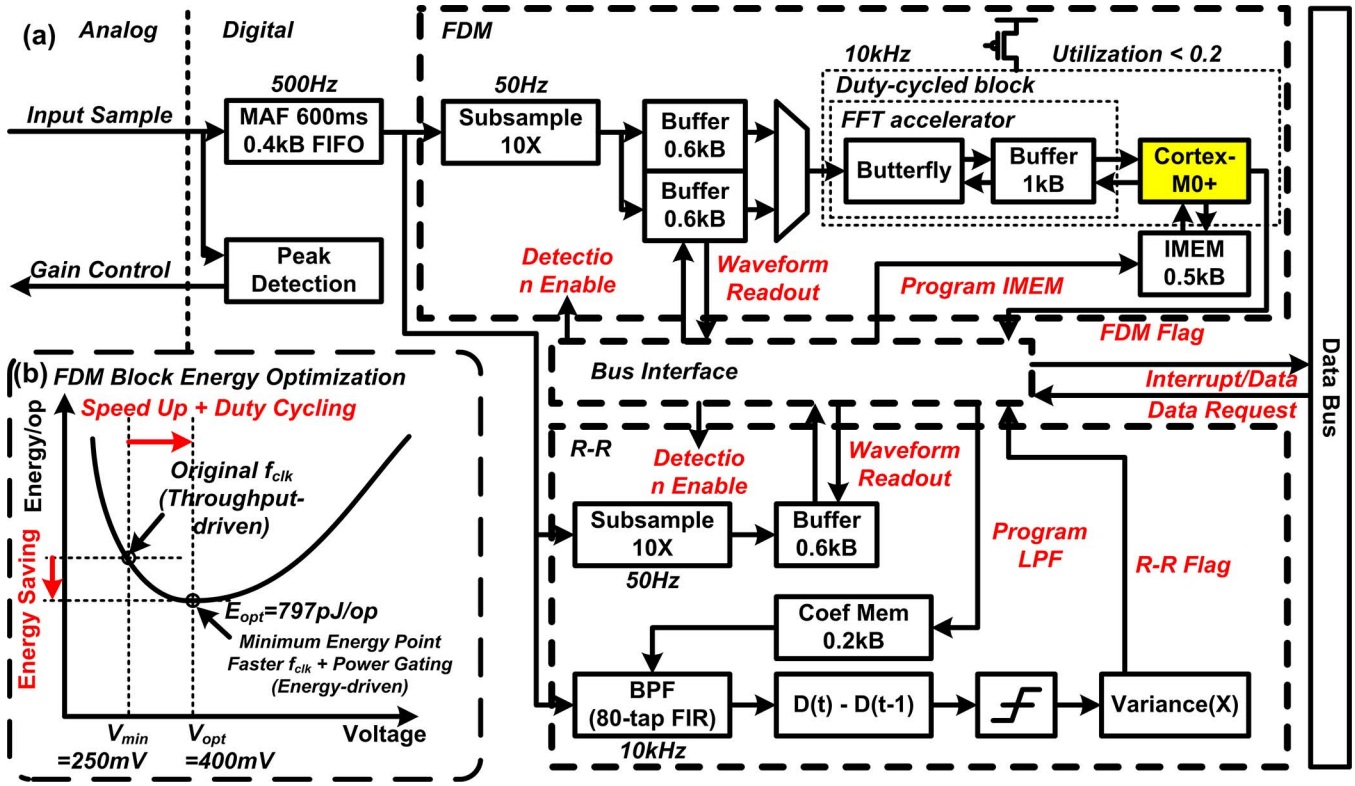

Fig. 15. (a) Top level of the proposed digital back end. (b) Energy/operation versus voltage shows the minimum energy point of the FDM block.

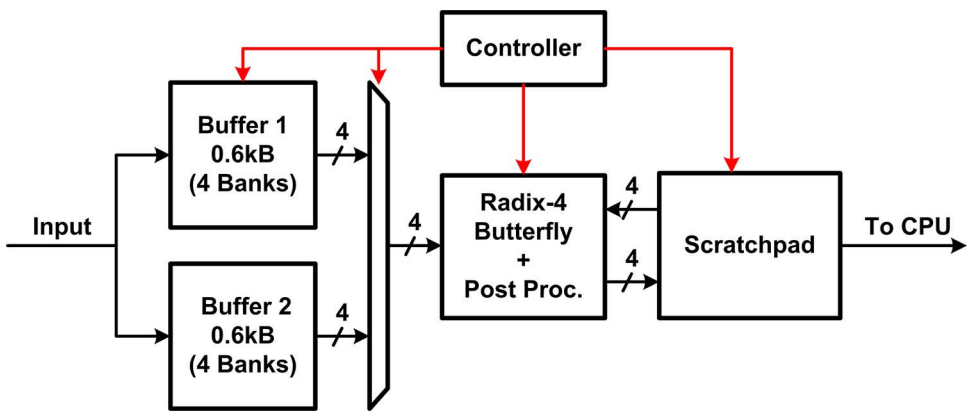

Fig. 16. Block diagram of FFT, peripheral buffers, and controller.

entire block, including the FFT and M0+ core, is power gated with an NMOS header using a boosted enable signal. Although a higher operating voltage is needed for this faster clock frequency, the leakage energy per computation is greatly reduced and minimum possible energy consumption is achieved. Compared to the supply voltage corresponding to just-in-time computation, this technique increases supply voltage by 50 mV while reducing energy by 40%.

V. Measurement Results

A. Proposed AFE Measured Results

Fig. 17(a) is the chip microphotograph of the proposed SoC, and Fig. 17(b) shows the chip inside the syringe needle. It is fabricated in 65 nm LP CMOS technology. The amplifier achieves 2.64 NEF with 31 nA current consumption and 6.52 μV input-referred rms noise. The measured amplifier gain ranges from 51 to 96 dB with 250 Hz bandwidth. The frequency response of the amplifier is shown in Fig. 18. The amplifier CMRR and PSRR are measured to be 55 and 67 dB, respectively. The measured SNR and THD with 0.5 mV peak-to-peak input sine wave with rail-to-rail output are 48.6 dB and 2.87% (-30.8 dB).

The measured maximum DNL and INL of the SAR ADC are ± 1.0 and ± 1.8 respectively. Note that the nonlinearity resulted from the DNL and INL are still less than the amplifier non linearity as shown in the SNDR. The SNDR and the ENOB are 44.8 dB and 7.14 bits respectively. The FOM of the ADC is 25.5 fJ/conv-step. The SNDR of the entire AFE are 30.7 dB which is dominated by the nonlinearity of the amplifier.

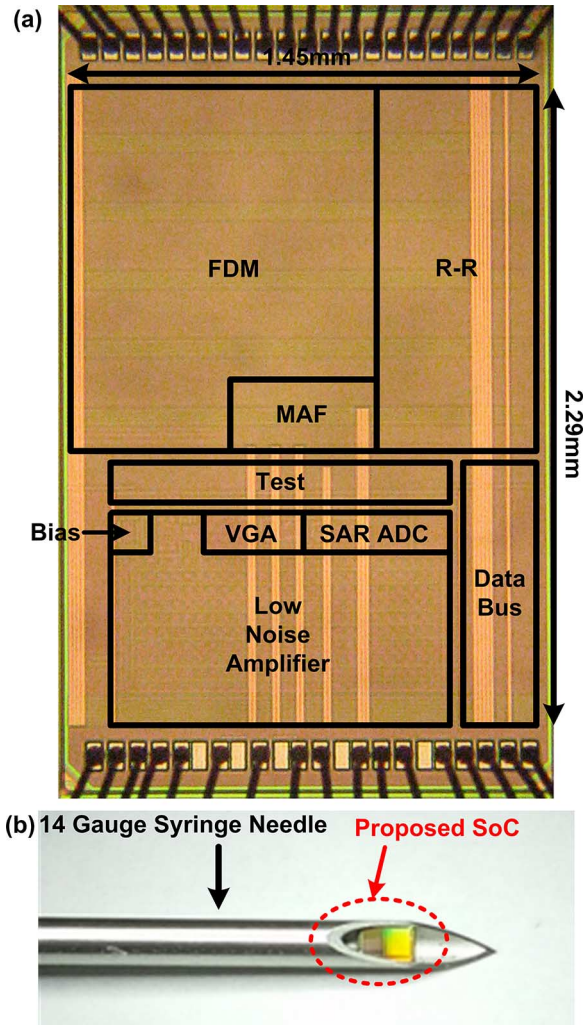

Fig. 17. (a) Die photograph of proposed SoC in 65 nm LP CMOS. (b) Photograph of proposed SOC and a 14 gauge syringe needle.

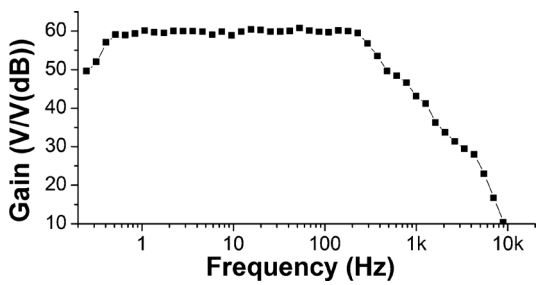

Fig. 18. Measured frequency response of the amplifier with the midband gain set to 59 dB.

B. Proposed SoC Measured Results

Table III shows the overall measured system results. The digital back-end operates at 0.4 V with a clock frequency of 10 kHz. The digital power consumption (including the clock power) is either 45 nW (FDM) or 92 nW (R-R), depending on the detection algorithm used. The proposed SoC consumes 64 nW (110 nW) in total when running the FDM (R-R) algorithm, enabling > 5 day lifetime with a 3.7 mm^2 (5μA·hr) thin-film battery. The functionality of the digital block and the analog front end are tested with an atrial fibrillation signal generated by the

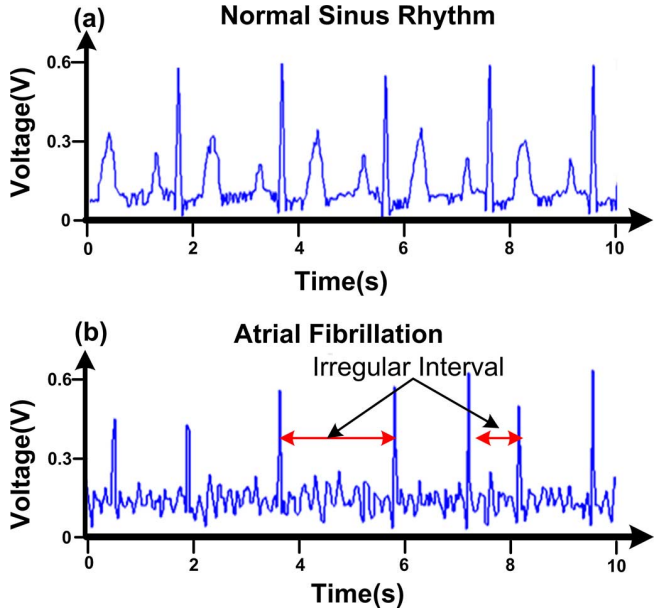

Fig. 19. (a) Normal ECG waveform generated by ECG simulator and recorded by the proposed system. (b) Arrhythmia waveform generated by ECG simulator and recorded and detected by the proposed system.

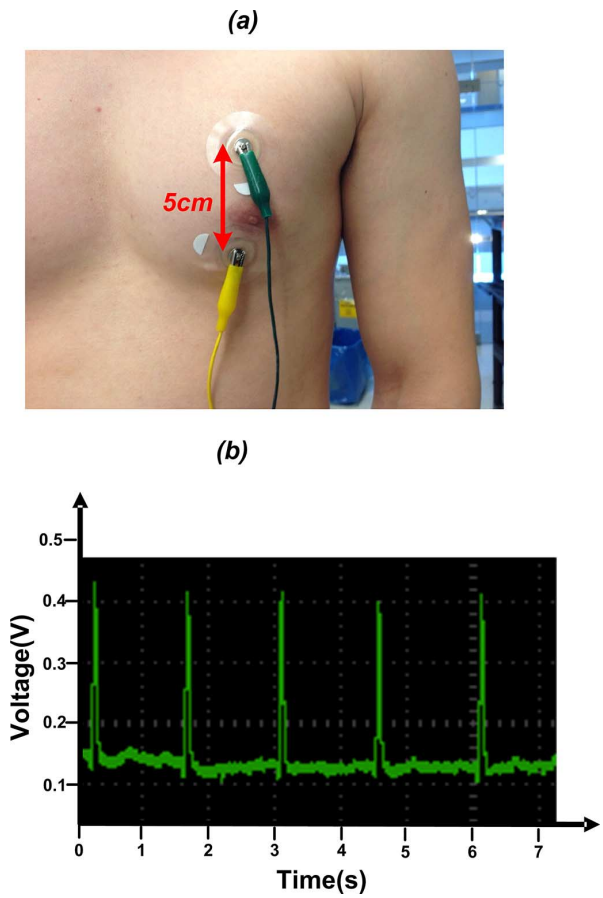

Fig. 20. (a) Test setup of the Human Chest Experiment. (b) Amplified waveform observed from the amplifier output terminal by the Agilent oscilloscope. The Vol/Div is 100 mV/Div and the Time/Div is 0.5 s/Div.

ECG signal simulator (PS410 Patient Simulator, Fluke Biomedical, Everett, WA, USA). The recorded waveform from the entire system is shown in Fig. 19. The system successfully cap-

TABLE III
SUMMARY OF MEASURED RESULTS FOR SOC

Technology		65 nm
Die Area		1.45 × 2.29 mm^2
AFE	V_{DD}	0.6 V
	Current	28 nA (LNA + VGA) 3 nA (ADC)
	Gain	51 ~ 96 dB
	Bandwidth	250 Hz
	Input Impedance	> 100 MΩ for <500hz
	Input Referred Noise	253 nV/√Hz (Noise Floor) 6.52 μV (RMS)
	Amplifier SNR	86dB
	NEF	2.64
	NEF×VDD^2	0.95
	CMRR@60Hz	55dB
	PSRR@60Hz	67dB
	THD	2.87%
	ADC Bits	8 Bits
	Sampling Frequency	500 Hz
	ADC Max DNL/INL	±1.0/±1.8
	ADC SNDR	44.8dB
	ADC ENOB	7.14
	ADC FOM	25.5fJ/conv-step
	AFE SNDR	30.7dB
DSP	V_{DD}	0.4 V
	Clock Frequency	10 kHz
	Total Memory	3.7 kB
	Power Consumption	45 nW (FDM) 92 nW (R-R)
	Main Processing Units	ARM Cortex-M0+ 16-b 512-pt RV FFT 80-tap FIR

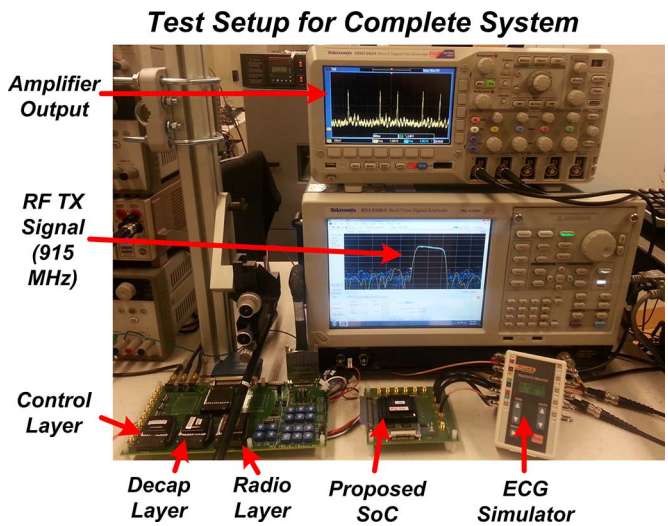

Fig. 21. Test setup of complete system with simulator, proposed SoC, and [16].

tures the arrhythmia signal in Fig. 19(b) under noisy supply and signals. As shown in Fig. 20, the system also tested with human body on the chest and commercial standard ECG electrode with 5 cm separation.

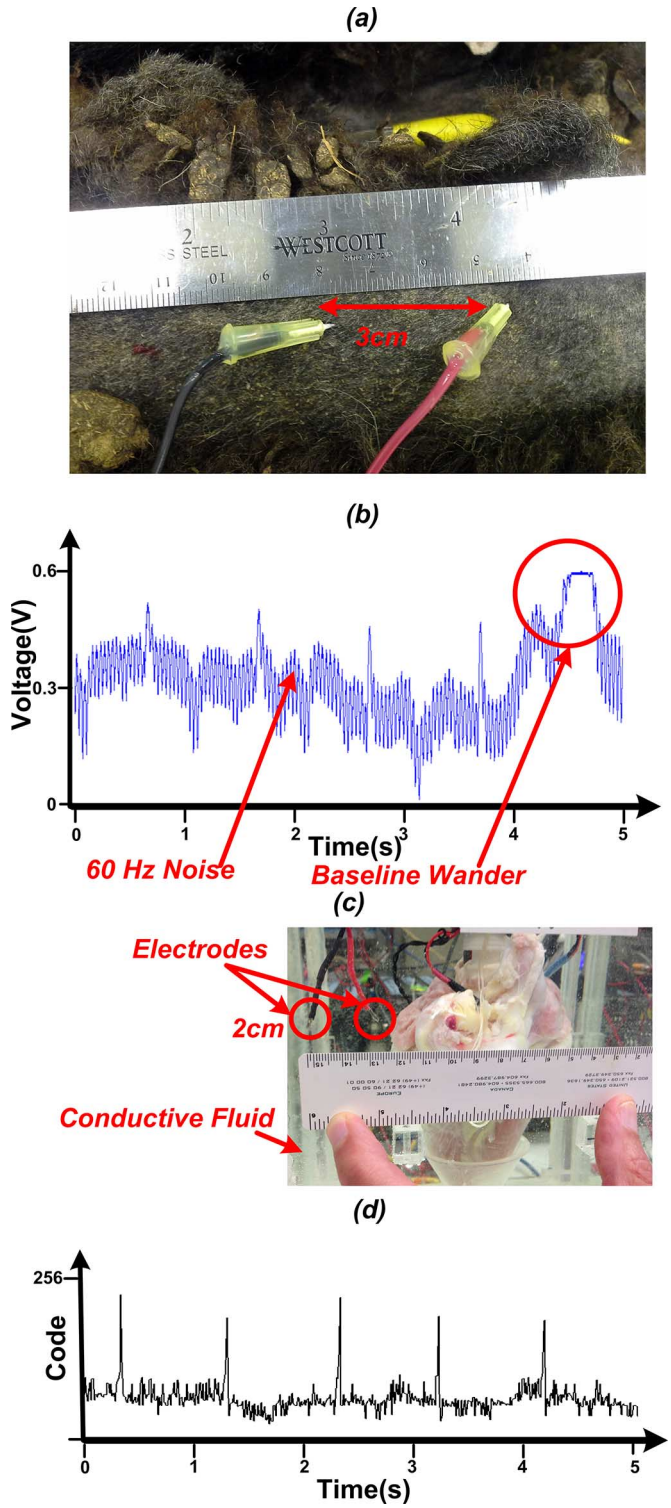

Fig. 22. (a) Test setup of the sheep experiment. (b) Measured waveform of the experiment. (c) Test setup of the isolated sheep heart experiment. (d) Measured waveform of experiment from digital readout buffer (downsampled by 10×).

C. Measurement Result with Peripherals

To build a complete electronics system, several other peripherals are needed including a power management unit and wireless module. The stacked microsystem of [16] includes a radio layer, control layer, and decap layer and is used in system-level testing in this work together with the proposed SoC [Fig. 3(b)].

TABLE IV
COMPARISON TABLE

		This Work	Zhang, JSSC'13[34]	Hsu, VLSI'12[10]	Kim, ISSCC'13 [11]	Liu, ASSCC '13 [12]	Deepu, ASSCC '13 [13]	Long, ISSCC'14[14]
Target Signals		**ECG**	ECG, EMG, EEG	ECG, VCG, PCG	ECG, Bio-Impedance	ECG	ECG	ECG
Technology		**65 nm**	130 nm	90 nm	180 nm	180 nm	350 nm	180 nm
AFE	V_{DD}	**0.6 V**	1.2 V	0.5 V	1.8 V	0.5V	2.4V~3V	1.3V~1.8 V
	Current	**31 nA**	4 μA	20.44 μA (8-Bit, 2kHz Sampling)	-	22.7 nA (Amplifier Not Included)	12.5μA	680nA
	Gain	**51 ~ 96 dB**	40 ~ 78 dB	40 ~ 64 dB	40 ~ 64 dB	-	47 ~ 66 dB	20 ~ 44 dB
	Bandwidth	**250 Hz**	320 Hz	0.5 ~ 1 kHz	0.5 ~ 1 kHz	-	35 ~ 175 Hz	130Hz
	Input Referred Noise	**6.52uVrms**	-	-	200 nV/$\sqrt{Hz}$	-	1.4 μVrms	4.9 μVrms
	ADC Resolution	**8 Bits**	8 Bits	8/12 Bits	9.3 Bits (ENOB)	8.1 Bits (ENOB)	9.3 Bits (ENOB)	7-10 Bits
	ADC Sampling Frequency	**500 Hz**	-	250 Hz ~ 100 kHz	-	3kHz ~ 6kHz	256/512Hz	-
DSP	V_{DD}	**0.4 V**	0.3 ~ 1.2 V	0.5V (1.0V for SRAM)	- (Analog Signal Processing)	0.5V	2.4V~3V	- (Analog Signal Processing)
	Power Consumption	**45 nW**	2.1 μW	-		435nW	0.89 μA	
	Clock Frequency	**10 kHz**	2 kHz ~ 1.7 MHz	25 MHz		250Hz ~ 500Hz	-	
Memory for Waveform Storage		**10x Down sampled waveform in buffer**	Fully stored in processor memory	Fully store in 4kB data memory	Fully store in signal path	Store in full sized output buffer	Stored lossless compressed waveform	Not storing the waveform
System Total Power Consumption		**64 nW**	6.9 μW	22.6 μW	11.3 μW	457nW	32 μW	884 nW
Power Calculation Configuration		**AFE + DSP Arrhythmia Detection (FDM)**	AFE + DSP R-R Extraction	AFE (BSI) + DSP + OSC Arrhythmia Detection	AFE (3ch ECG + RA) + ASP + OSC Arrhythmia Detection	ADC + DSPE + Feature Extraction	AFE + DSPE + Feature Extraction	AFE + ASP + QRS Extraction

The components of [16] consume 11 nW in the default monitoring mode and the wireless module is activated (which consumes 20 μW) only when needed during recharging and data retrieval. After the proposed SoC is programmed through the control layer and radio layer, other layers go into sleep mode and consume 11 nW. When an arrhythmia is generated by the ECG simulator, the proposed SoC sends an interrupt signal to the control layer. The control layer then wakes up to retrieve the waveform and store it into memory. Moreover, the radio layer also wakes up and is able to send out an RF transmit signal at 915 MHz.

The proposed SoC successfully communicates with other chips, including a power management unit and external memory from [16], over a data bus; the complete system configuration is shown in Fig. 21. Measured waveforms are taken by the SoC under different scenarios including an ECG simulator (Fig. 19), a live sheep [Fig. 22(a) and (b)], and an isolated sheep heart [Fig. 22(c) and (d)]. The isolated live sheep heart is immersed in conductive saline fluid to mimic the implantation environment. The electrodes connected to the analog front end are separated by 2 cm and located near the heart. Note the low frequency wandering and 60 Hz noise present in the measured waveform from a live sheep (which represents a patch-based approach as the electrodes are placed on the skin) compared to the isolated heart test. These signals demonstrate the signal quality improvement of a syringe-implantable approach. Table IV provides a comparison table to related prior work.

VI. CONCLUSION

This work presents an ultralow-power syringe-implantable long-term observation and arrhythmia detection ECG SoC fabricated in 65 nm CMOS technology. The design trades off noise and power using analog–digital co-optimization and employs several amplifier techniques, asynchronous SAR logic, and minimum energy digital computation to achieve 64 nW power consumption. The proposed circuit and new algorithm are verified under different scenarios including an ECG simulator, a live sheep, and an isolated sheep heart. The SoC consumes state-of-the-art power compared to all other works with similar functionality.

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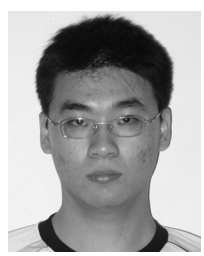

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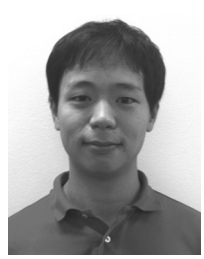

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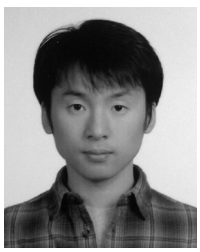

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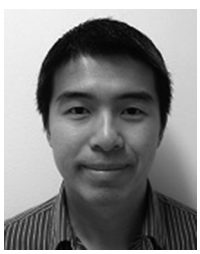
His research interests include subthreshold circuit designs, ultralow-power SRAM, and the design of millimeter-scale computing systems and sensor platforms.



ZhiYoong Foo received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA.

He is currently a Research Fellow in Electrical Engineering with the University of Michigan, Ann Arbor, MI, USA. His research includes low-cost and ultralow-power VLSI circuit systems integration.

Inhee Lee (S'07) received the B.S. and the M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, Korea, in 2006 and 2008, respectively. He is currently working toward the Ph.D. degree at the University of Michigan, Ann Arbor, MI, USA.

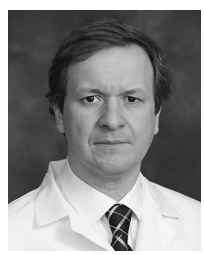
In fall 2012, he held a Research Intern position with Kilby Lab, Texas Instrument, Dallas, TX, USA. His current research includes delta-sigma ADCs, capacitive energy harvesters and power management circuits, battery monitoring circuits and micro-scale wireless sensor nodes.

Nicholas B. Langhals received the B.S.E. degree in bioengineering from Arizona State University, Tempe, AZ, USA, in2001, and the M.S.E. degree in engineering and Ph.D. degree in biomedical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2003 and 2010, respectively. His doctoral work focused on cortical brain-machine interfaces, cortical mapping, direct brain drug delivery, electrode development and characterization, and neural signal analysis.

He currently serves as a Research Assistant Professor with the Plastic Surgery Section, Department of Surgery, and an Assistant Research Scientist of biomedical engineering. He also has affiliate appointments with the University of Michigan Injury Center and the Michigan Center for Integrative Research in Critical Care (MCIRCC). He has worked as a Senior Research Engineer within the Center for Neural Communication Technology and also served as a consultant for Neuronexus Technologies (Ann Arbor, MI, USA) and Biotectix (Ann Arbor). His research efforts are focused around the development of electrode technology and signal processing techniques for neuroprosthetic, cardiac, and other electrophysiological interfaces. He is currently co-director of the Neuromuscular Lab, which is a translational and basic science research lab, housed in the Plastic Surgery Section of the Department of Surgery. His primary efforts are focused around the development of regenerative peripheral nerve interfaces that have the potential to be used for control of replacement robotic appendages in amputees. His secondary efforts are focused around the development of real-time processing strategies for mapping atrial fibrillation from intracardiac electrodes.

Grant H. Kruger received the Ph.D. degree in electrical engineering from the Nelson Mandela Metropolitan University, South Africa, in 2005.

After graduating, he lectured in the Department of Mechatronics before pursuing his postdoctoral research at the University of Michigan in 2007. He is currently an Assistant Research Scientist with the Department of Mechanical Engineering and a Research Investigator with the Anesthesiology Department at the University of Michigan, Ann Arbor, MI, USA. His research and publications cover areas from manufacturing to biomedical engineering. Dr. Kruger's current research focuses on health informatics, specifically the research and development of systems, devices and signal processing based on artificial intelligence technology.



Hakan Oral received the M.D. degree from Hacettepe University;

He completed his internal medicine residency at the Baylor College of Medicine. He then did his fellowship training, first in cardiology, and the in cardiac electrophysiology, at the University of Michigan, Ann Arbor, MI, USA, where he is currently a Professor of internal medicine and the Frederick G.L. Huetwell Research Professor of Cardiovascular Medicine. He also serves as the Director of the Cardiac Arrhythmia Service. He then joined the University of Michigan faculty. His studies have contributed to the understanding the mechanisms of atrial fibrillation and have been instrumental in defining novel techniques for the mapping and ablation of cardiac arrhythmias, particularly atrial fibrillation.

Omer Berenfeld received the Ph.D. degree in medical physics from Tel Aviv University, Tel Aviv, Israel, in 1995.

He completed his postdoctoral training in cardiac electrophysiology at the Upstate Medical University, Syracuse, NY, USA, where he joined the faculty in 2005 and later moved to the University of Michigan, Ann Arbor, MI, USA, in 2008, where he is currently an Associate Professor of internal medicine and biomedical engineering with the Center for Arrhythmia Research. His main interests are in the basic and clinical research of cardiac impulse propagation and arrhythmias. His research employs optical, electrical, and computational approaches to investigate cardia arrhythmias from bench to bedside. In particular, his studies on ventricular and atrial fibrillation have led to groundbreaking understanding of their underlying mechanisms and paved the way for better detection and treatment of those devastating arrhythmias.

Zhengya Zhang (S'02–M'09) received the B.A.Sc. degree in computer engineering from the University of Waterloo, Waterloo, ON, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, CA, USA, in 2005 and 2009, respectively.

Since 2009, he has been on the faculty of the University of Michigan, Ann Arbor, MI, USA, as an Assistant Professor with the Department of Electrical Engineering and Computer Science. His current research interests include low-power and high-performance VLSI circuits and systems for computing, communications and signal processing.

Dr. Zhang was a recipient of the National Science Foundation CAREER Award in 2011, the Intel Early Career Faculty Honor Program Award in 2013, the David J. Sakrison Memorial Prize for outstanding doctoral research in EECS at UC Berkeley, and the Best Student Paper Award at the Symposium on VLSI Circuits. He is an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS.

David Blaauw (M'94–SM'07–F'12) received the B.S. degree in physics and computer science from Duke University, Durham, NC, USA, in 1986, and the Ph.D. degree in computer science from the University of Illinois, Urbana, IL, USA, in 1991.

After his studies, he worked for Motorola, Inc., Austin, TX, USA, where he was the Manager of the High Performance Design Technology group. Since August 2001, he has been on the faculty at the University of Michigan, Ann Arbor, MI, USA, where he is a Professor. He has authored/coauthored over 450 papers and holds 40 patents. His work has focused on VLSI design with particular emphasis on ultralow-power and high-performance design.

Dr. Blaauw was the Technical Program Chair and General Chair for the International Symposium on Low Power Electronic and Design. He was also the Technical Program Co-Chair of the ACM/IEEE Design Automation Conference and a member of the ISSCC Technical Program Committee.

Dennis Sylvester (S'95–M'00–SM'04–F'11) received the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA.

He is a Professor of electrical engineering and computer science with the University of Michigan, Ann Arbor, MI, USA, and Director of the Michigan Integrated Circuits Laboratory (MICL), a group of ten faculty and 70+ graduate students. He has held research staff positions in the Advanced Technology Group of Synopsys, Mountain View, CA, USA, Hewlett-Packard Laboratories, Palo Alto, CA, USA, and visiting professorships with the National University of Singapore and Nanyang Technological University. He has authored/coauthored over 375 articles along with one book and several book chapters. His research interests include the design of millimeter-scale computing systems and energy-efficient near-threshold computing. He holds 20 U.S. patents. He also serves as a consultant and technical advisory board member for electronic design automation and semiconductor firms in these areas. He cofounded Ambiq Micro, a fabless semiconductor company developing ultralow-power mixed-signal solutions for compact wireless devices.

Dr. Sylvester was the recipient of a National Science Foundation CAREER award, the Beatrice Winner Award at ISSCC, an IBM Faculty Award, an SRC Inventor Recognition Award, and eight Best Paper Awards and nominations. He was the recipient of the ACM SIGDA Outstanding New Faculty Award and the University of Michigan Henry Russel Award for distinguished scholarship. He serves on the technical program committee of the IEEE International Solid-State Circuits Conference and previously served on the executive committee of the ACM/IEEE Design Automation Conference. He has served as an associate editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN and the IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS and guest editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS. While at the University of California, his dissertation was recognized with the David J. Sakrison Memorial Prize as the most outstanding research in the UC-Berkeley Electrical Engineering and Computer Science Department.