A 1.5-GHz 6.144T Correlations/s 64 × 64 Cross-Correlator With 128 Integrated ADCs for Real-Time Synthetic Aperture Imaging

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***Abstract*— A 65-nm CMOS, 18-mm^2, 1.5-GHz 64 × 64 cross-correlator with 128 on-chip analog-to-digital converters (ADCs) enables real-time synthetic aperture radiometric imaging. This brief enables high-resolution synthetic aperture radiometry by greatly improving the integration and energy efficiency of the mixed-signal baseband cross-correlator. The design supports analog-in and digital correlation out, removing approximately 5 W of power that would otherwise be needed for I/O between the ADCs and the digital correlation core. The prototype 6.144T correlation/s 1.5 Gsamples/s 64 × 64 correlator is designed for satellite-based radiometric imaging of water in the atmosphere. Massive parallelism together with an optimized correlation scheme leads to a measured energy consumption of only 0.35 pJ/correlation/cycle. A correlation efficiency greater than 90% is achieved for input signal levels greater than −30 dBm.**

***Index Terms*— Circuits, Mixed analog digital integrated circuits, Synthetic aperture radar, System-on-chip.**

I. Introduction

THIS paper enables high-resolution synthetic aperture radiometry by greatly improving the integration and energy efficiency of the mixed-signal baseband cross-correlator. Imaging radiometry over millimeter-wave frequencies (30–300 GHz) has the potential to transform security, health care, and remote sensing. Applications include sensing of concealed weapons [1], detection of skin cancer [2], and mapping of water in the atmosphere [3]. Originally conceived for radio astronomy, synthetic aperture radiometry achieves a high resolution image with a simple frontend and a relatively small number of antenna elements. However, the complexity and processing required from the mixed-signal baseband have hampered use in energy constrained and size constrained applications. We introduce the first large-scale fully integrated high-speed correlator that incorporates both analog-to-digital converters (ADCs) and high-speed digital correlation in a single power-efficient IC. Operating at 1.5 GHz, the prototype achieves 6.144T correlations/s and consumes 3.735 W.

Synthetic aperture radiometry has significant advantages over other imaging radiometry techniques. It is much smaller and more reliable than a mechanical scanned antenna. Compared to a phased array, a synthetic aperture system has a much simpler frontend and more importantly requires far fewer antenna elements to achieve the same resolution, thanks to array thinning [4]. Synthetic aperture radiometry combines the outputs of an array of fixed individual antennas to construct a complete image of a scene. Cross-correlation of the individual antenna outputs generates spatial Fourier terms that represent the scene, so that the image is revealed, simply, by taking an inverse Fourier transform.

This paper presents a low-power IC that both digitizes and cross-correlates 128 elements at up to 1.5 GHz, enabling low-power, low-cost, real-time synthetic aperture imaging radiometry. Despite its advantages, the requirements for high-speed (Gsamples/s) digitization of a large number of element outputs, along with the need to generate a very large number of correlation products (i.e., 10 s of Tcorrelation/s), have hampered the practical realization of synthetic aperture radiometer systems. In [6], a 1-bit 64-channel digital correlator without ADCs was reported [5], but the power-hungry gigahertz + I/Os and signal routing create a huge bottleneck. The prototype 6.144T correlation/s 1.5 Gsamples/s 64 × 64 correlator is designed for satellite-based passive radiometric imaging of water in the atmosphere.

As shown in the system diagram of GeoSTAR [4] (Fig. 1), a geosynchronous satellite based radiometer, millimeter wave signals at 183GHz collected by a fixed 2D array of antennas are mixed-down to baseband. The 128 500 MHz bandwidth baseband signals are digitized and cross-correlated by the correlator IC. The limited available power in the satellite system and the limited capability for heat dissipation greatly constrain power consumption. Integrating the 128 ADCs on the IC saves approximately 5 W, which would otherwise be dissipated by 384 LVDS I/O connections. The 65 nm CMOS prototype, packaged in custom-

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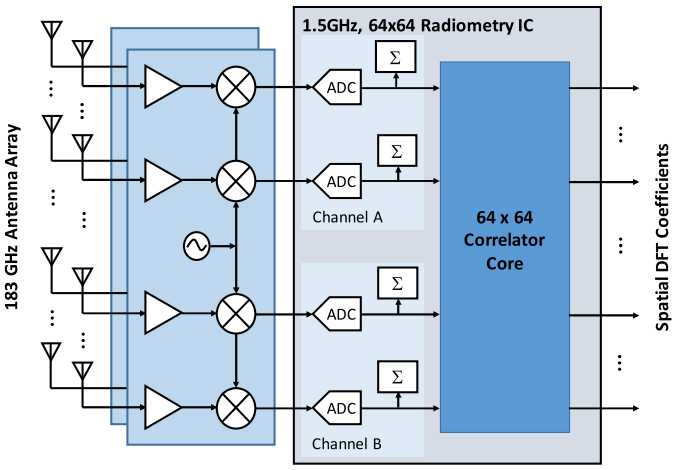


Fig. 1. Top-level block diagram of the 64 × 64 cross-correlator chip integrated with 128 ADCs.

designed 576 pin eight-layer substrate, is radiation tolerant. A massively parallel digital correlation architecture together with a modified correlation scheme leads to a measured energy consumption as low as 0.35 pJ/correlation/cycle.

II. Synthetic Aperture Radiometry and the GeoSTAR System

A. GeoSTAR System

The prototype mixed-signal correlator IC is designed for GeoSTAR, a new type of microwave sounder that can produce 3-D images of tropospheric temperature and humidity profiles of the earth from geostationary orbit (GEO) every 15 to 30 min [3], [4]. GeoSTAR is a 2-D spatial interferometer with a large synthetic aperture capable of providing high spatial resolution from geosynchronous orbit. The antenna elements in this system are arranged in a Y configuration, which achieves a large synthetic aperture with a highly reduced number of antenna elements. The increased temporal resolution provided by the GeoSTAR platform will allow highly dynamic weather phenomena like hurricane genesis and intensification to be better studied, tracked, and predicted.

B. Advantages and Challenges of Synthetic Aperture Radiometry

Adapted from radio astronomy, synthetic aperture radiometry simultaneously captures an entire scene by processing the outputs of an array of antenna elements. As shown in Figs. 1 and 2, a synthetic aperture system works by cross-correlating down-mixed baseband signals from an array of individual antenna elements. This operation is also known as interferometry. The complex correlation between element outputs (i.e., Re{V} and Im{V} in Fig. 2) is referred to as the *visibility function* [7]. Each cross-correlation represents a spatial harmonic of the scene. In this way, the 2-D image is revealed with an inverse Fourier transform of the visibility function. For synthetic aperture radiometry, antennas are nominally placed in a grid spaced at half wavelength intervals. In practice, the array can be *thinned* [4], [7] to dramatically reduce the number of antenna elements with no loss in resolution. A "Y" pattern is especially popular.[1]

[1]Radio telescopes that employ aperture synthesis, such as the very large array, use a Y-shaped array.

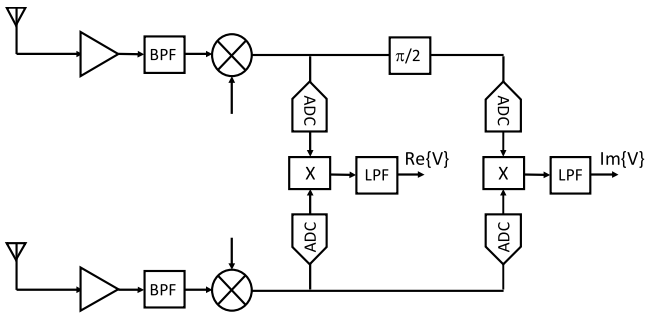


Fig. 2. Cross-correlation between two antenna elements. Re{V} and Im{V} are terms of the visibility function.

The processing for a pair of antenna elements is shown in Fig. 2. After bandpass filtering, the antenna signals are mixed down to baseband. Digitized baseband signals are multiplied together for cross-correlation. Multiplication is best done in the digital domain not only for accuracy but also because this is the only practical way to multiply each antenna signal with many other antenna signals. To obtain the cross-correlation, the products are accumulated, which is equivalent to low pass filtering with an integrator.

Fundamentally, noise in the visibility function (ΔV) is related to the integration time τ, the bandwidth B, and the system noise temperature T_S

$$\Delta V = \frac{T_S}{\sqrt{2B\tau}}. \tag{1}$$

For the GeoSTAR, the goal is to resolve an image of the earth to 0.3 K accuracy within 15 min, and so a 500-MHz bandwidth is chosen. Quantization noise due to finite resolution worsens visibility noise. However, effective cross-correlation of Gaussian random signals requires a surprisingly low word width [8]. With a 2-bit digitization, noise in the visibility function is only 1.14 times larger than with ideal analog multiplication. Therefore, 2-bit ADCs are used with little loss in performance. On the other hand, the accuracy of the thresholds in the 2-bit ADC needs to be far higher than in a conventional 2-bit ADC.

Despite the significant advantages of aperture synthesis, until this work, practical application has been limited by the very significant digitization and digital processing requirements. This is especially the case for energy constrained applications, including deployment in space. To support the 500-MHz bandwidth, each element requires a high speed (i.e., >1Gsamples/s) ADC. Trillions of correlations must be calculated each second. A further challenge is that space-based radiometer must work reliably in a high radiation environment. The radiation environment is especially challenging if the instrument is placed in a GEO.

III. Massively Parallel Mixed-Signal Architecture

A block diagram of the 64 × 64 correlator with 128 on-chip ADCs is shown in Fig. 1. The architecture is designed to minimize the overall power consumption. The digital correlator core generates all cross-correlations between the two sets of 64 digitized signals. At 1.5 GHz, the core performs 6.144T

2-bit cross-correlations/s, consuming 0.61 pJ/correlation/cycle. 128 1.5-Gsamples/s 2-bit resolution radiation-hardened ADCs digitize 128 inputs to an 8-bit equivalent noise level. Integrating ADCs and a digital correlator core on the same die not only reduces system size but also eliminates 5 W of power, which would otherwise be needed for high-speed I/O and signal routing between discrete ADCs and a discrete processor core. The 2-bit ADCs achieve the equivalent of an 8-bit SNR, allowing effective operation with input signals as low as -30 dBm (50 Ω). This small signal level simplifies the IF buffering, saving several watts of system power. The full GeoSTAR system requires crosscorrelation of more than 800 IF signals. A lower signal level allows a lower amplifier supply voltage for an acceptable amount of distortion.

A. High-Speed ADC Design With Adjustable Thresholds

The large number of ADCs and the unique system requirements present challenges for the design of ADC. A high SNR permits a small (-30 dBm) input amplitude, saving considerable system (i.e., IF buffer) power. Although the ADC resolution is nominally 2 bits, the threshold crossings must be very accurate to properly capture the statistics of the signal. Furthermore, these levels need to be tunable to accommodate different input power levels. Other 2-bit radiometry systems use 8- or 10-bit discrete ADCs followed by digital thresholding to three levels [9]. Instead, our ADC uses three low-noise comparators with each comparator reference set by a digital-to-analog converter (DAC) for offset cancellation and amplitude control. These thresholds are adjusted as needed to compensate for both the initial offsets within the ADC and to compensate for the RF receiver and IF amplifier gain changes between ground tests and GEO, due to environmental temperature changes, for example. This eliminates the need for AGCs. The threshold voltages are set to achieve a nominal distribution of approximately 20%, 30%, 30%, and 20% among all four digital outcomes, weighted as -3, -1, $+1$, and $+3$, respectively. On-chip digital totalizers monitor the signal statistics for each ADC.

The 1.5 Gsamples/s ADC architecture is illustrated in Fig. 3. The 2-bit flash architecture is compact and low power, while the 8-bit noise[2] performance and the DAC adjustable references allow the ADC to digitize input signals over a large dynamic range. The comparators are based on a current-mode latch (CML) structure to achieve a short aperture time and eliminate the need for 128 input sample and holds. Each ADC uses three CML comparators with separate offset-correction DACs, differential clock buffers, and a thermometer-to-binary encoder with -3, -1, 1, and 3 binary encoded outputs. Three 5-bit resistor-string DACs in each ADC enable offset correction and variable gain adjustment. Each ADC has its own reference ladder to reduce crosstalk between channels. The resistor-string DACs and the ADC share the same resistor ladder structure. Each complete ADC cell, including DACs, occupies 128 μm $\times$ 350 μm to fit beneath four solder-bumps and consumes 1 mW.

[2]The comparator noise level is equivalent to that of comparators in an 8 bit ADC. This allows the ADC to meet the system noise requirements over a large ADC input range.

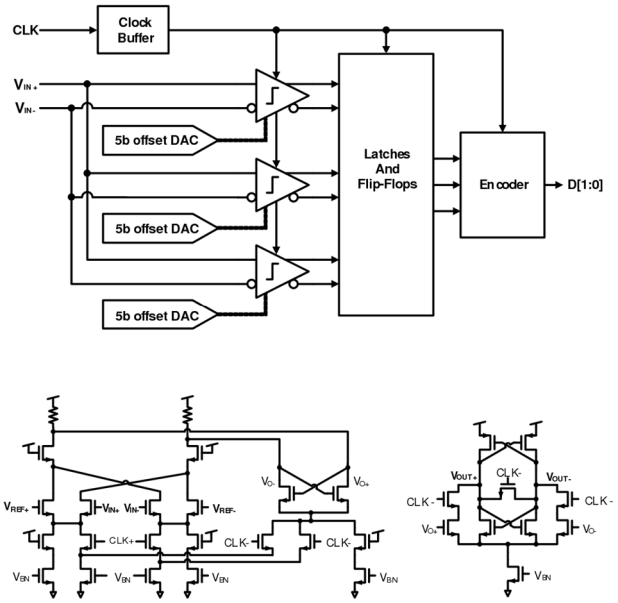


Fig. 3. Top: single ADC channel. Bottom: CML comparator and regenerative analog latch.

To improve the overall comparator gain and reduce the probability of metastability, each CML comparator is followed by three stages of radiation-hardened regenerative latches: the first, a resetting analog latch, and the last two, ratioed digital latches. The first stage accepts fully differential reference and analog inputs. Cascode devices on the load reduce capacitance on the sensitive latching node. Radiation tolerance is enhanced by separating all PMOS and NMOS structures with wide double guard rings and by using dual interlocked storage cell (DICE) latches for the digital latches and encoder.

B. 64 $\times$ 64 Digital Correlator Core

As shown in Fig. 4, the core uses 4096 correlators operating in parallel at 1.5 GHz to compute the cross-correlations between two sets of 64 inputs in every clock cycle. These correlations are accumulated over a 10 ms integration window before they are read out. Supply voltage scaling is a promising approach to reduce power consumption, but the minimum 1 GHz operation imposes a stringent 1 ns clock period that limits the extent of voltage scaling. The requirement for radiation tolerance can further complicate the design, as hardening requires upsizing, redundancy, voltage margin, and timing margin, which inevitably increase power and decrease speed. To overcome these challenges, we designed a specialized correlator arithmetic to reduce complexity and structured the pipelined datapath to enable extended supply voltage scaling.

The specialized correlator arithmetic is illustrated in Fig. 5. A 2-bit digitizer output has four possible levels $\{-3, -1, 1, 3\}$ and the cross-correlation belongs to $\{-9, -3, -1, 1, 3, 9\}$. The literal implementation of the correlator requires a 5-bit integer arithmetic. To reduce the dynamic range, we scale down the correlator output by a factor of 3 to $\{-3, -1, -1/3, 1/3, 1, 3\}$, then round it to $\{-3, -1, 0, 0, 1, 3\}$, and finally add an offset of 3 to $\{0, 2, 3, 3, 4, 6\}$. This manipulation reduces the 5-bit output to 3 bits. The arithmetic is captured in a table, with two 2-bit inputs producing 16 3-bit outputs. The table is

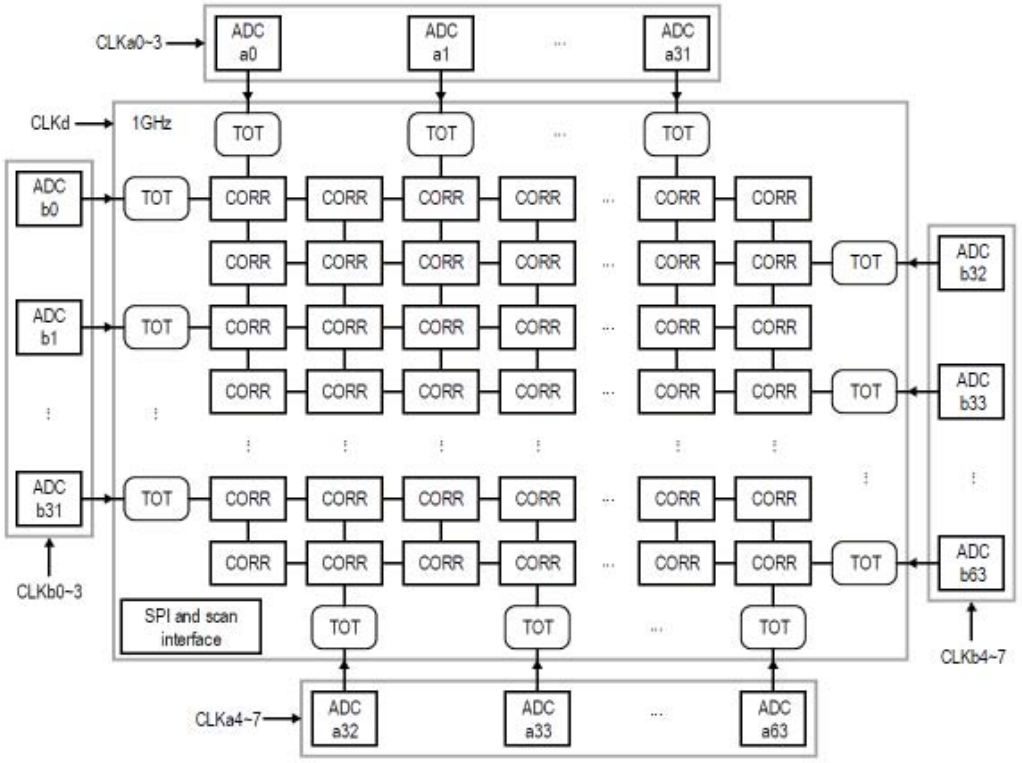


Fig. 4. Top-level block diagram of the 64 × 64 cross-correlator chip integrated with 128 ADCs. (CORR: 2-bit correlator and TOT: 4-bin totalizer).

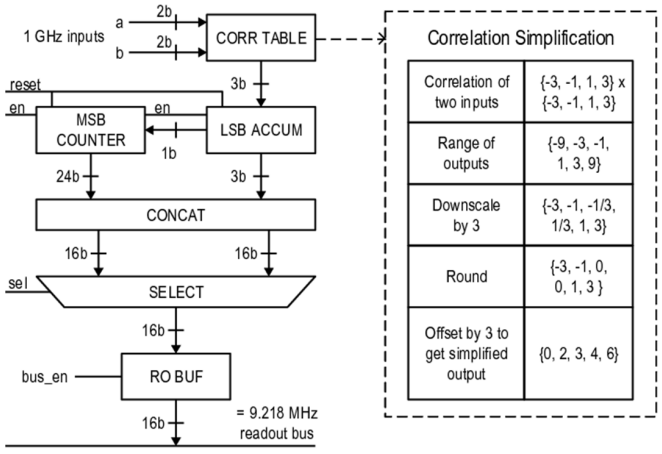


Fig. 5. Correlator design and simplified correlation.

synthesized to combinational logic. This simplification has a major implication on power and silicon area, as the correlator design is replicated 4096 times. The impact on signal-to-noise (SNR) is minor and is compensated by a 2% longer integration window.

The 3-bit correlation outputs are continuously accumulated for a 10 ms integration window. At 1.5 GHz, 10 ms translates into 15 million clock cycles, and thus a 27-bit accumulator is needed. However, an accumulator with a 27-bit adder does not meet the <1 ns timing requirement. Therefore, we designed a two-stage pipelined adder with a 3-bit adder to accumulate 3-bit correlation outputs and a 24-bit adder (counter) to accumulate the MSB, as shown in Fig. 5. The correlation output of each cycle is accumulated by the 3-bit LSB adder that produces a carry as the enable to the 24-bit MSB counter. The 4096 correlators operate independently, but their outputs are all connected to a single 16-bit readout bus. As a result, the capacitive loading of the readout bus is significant, and it becomes challenging to drive the bus at a sufficiently high speed. To reduce the capacitive loading on each correlator, the readout bus is restructured to a three-level hierarchy. At the first level, 16 correlators are connected to a local bus in order to limit the loading seen by each correlator. At the second level, 16 local buses are ORed together to an intermediate bus, thereby isolating each local bus. At the final level, 16 intermediate buses are ORed together to the top-level readout bus. The hierarchical structure limits the loading seen by each correlator and significantly improves the clock frequency.

Readout occurs after each 10 ms integration window, and up to 1 ms is allocated to readout to meet a minimum 90% duty cycle requirement (i.e., to perform correlations for 90% of the time while readout takes only 10% of the time). Given a 1 ms readout time, the hierarchical readout bus operates at a divided clock (with a configurable divide ratio) to reduce the switching power and to allow drivers and buffers to be downsized to save power and area. To capture signal statistics for calibrating the radiometer, 128 totalizers, one for each of the 128 ADCs, record a histogram of each ADC's outputs over the integration window.

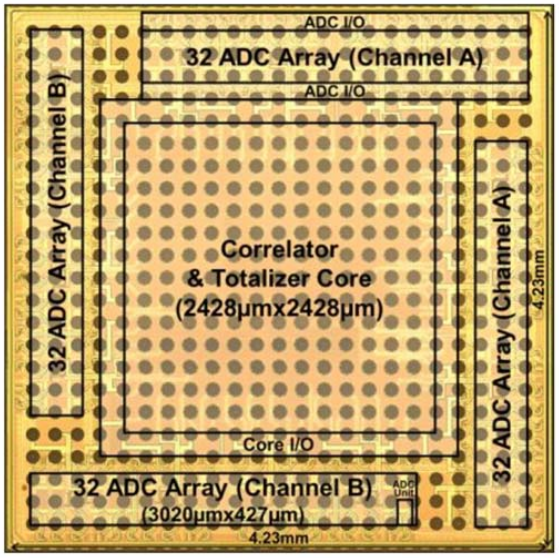


Fig. 6. Chip microphotograph.

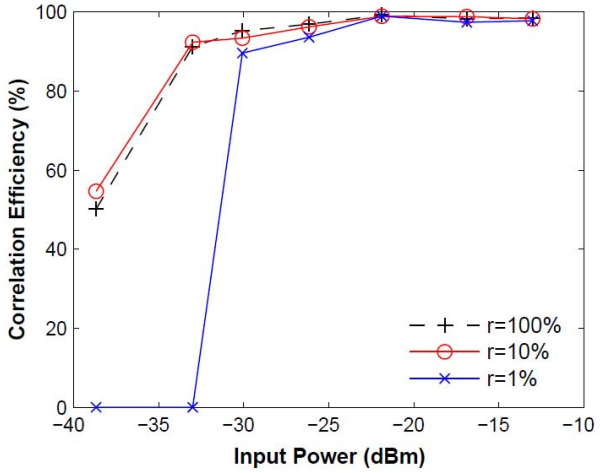


Fig. 7. Measured correlation efficiency of the prototype. ($r = 100\%$ represents when the two channels receive 100% correlated inputs; $r = 10\%$ represents the two channels receive 10% correlated inputs and so on.)

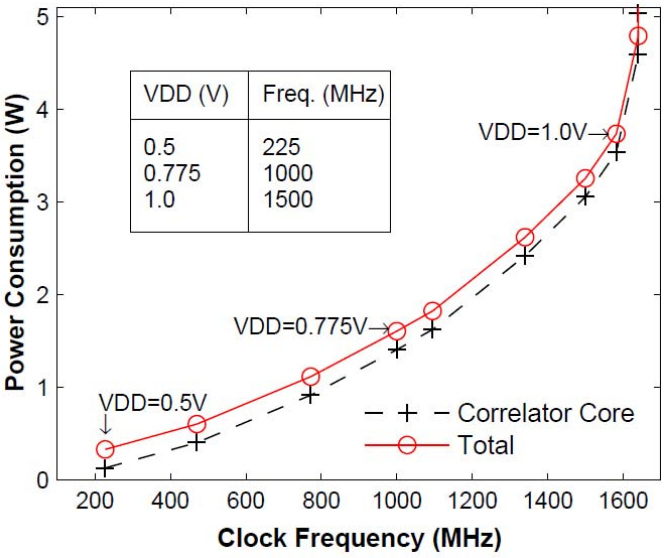


Fig. 8. Measured correlator core and total power consumption of the test chip.

C. Radiation Tolerance

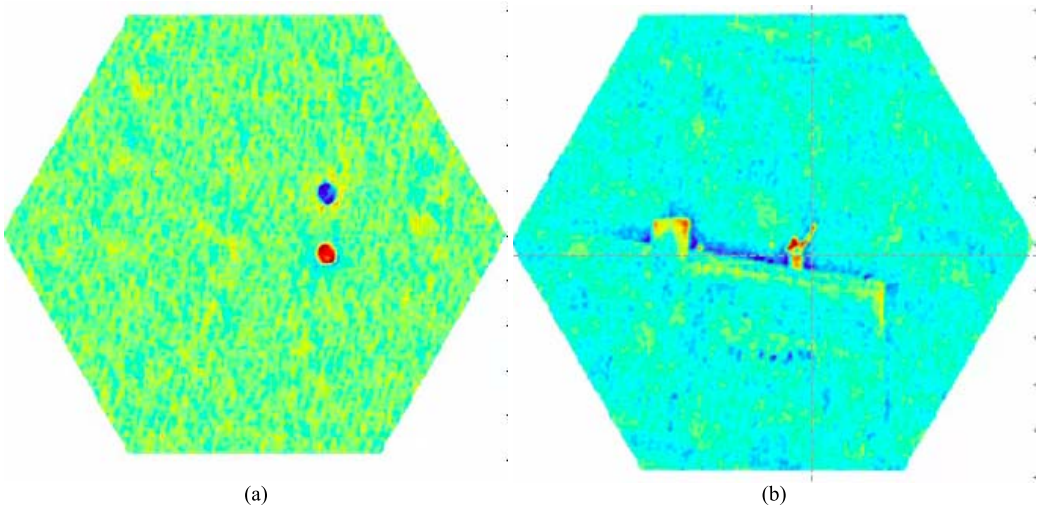
The correlator core design needs to be robust to the abundant high-energy particles in the deep space environment. The 150 Kb of on-chip registers storing correlations and signal histograms are the most vulnerable to soft errors due to single-event effects. However, conventional radiation hardening techniques, such as DICE [10] and triple modular redundancy (TMR), incur significant extra power and area that challenge the viability of the GeoSTAR system. We carried out heavy-ion radiation tests to measure the error sensitivity of a small-scale 5×5 correlator test chip [11] and used the test results with the CREME tool [12] to compute the expected error rate for GEO. Based on the measurement results, we estimate that an unhardened 64×64 correlator core operating in the GEO will experience only 0.163 errors/day, while a hardened version using DICE and TMR will experience 0.0057 errors/day.

For the imaging system, the bit error rate only needs to be low enough to ensure that anomalous images occur at a manageably low rate. For a frame rate of thousands of frames per day, an error even as high as hundred or more bit errors each day is tolerable. In this context, the higher error rate of the unhardened design is still sufficiently low, so we chose an unhardened digital core design to save significant power and silicon area. On the other hand, ADC hardening does not significantly impact power or area, so the ADC was hardened with a small overall increase in power and area. Radiation tests on the full-scale application-specific IC, performed by JPL, confirmed the predicted estimates for radiation hardness. ADC errors were at a level that was too low to detect.

IV. Measurements

The 1 GHz 128-channel correlator IC (Fig. 6) is fabricated in 65-nm CMOS and occupies 18 mm^2. The 6-mm^2 digital core contains the correlators and totalizers. The 128 ADCs are arranged in four sections along the periphery. The device is flip-chip bonded to a custom-designed 576 pin eight-layer substrate. The large pin count supports the large analog I/O requirement for the 128 ADCs and a large number of power and ground pins. To characterize the effectiveness of the correlators, we measure the correlation efficiency [13] as the ratio of correlations obtained from the test chip to ideal correlation values. Fig. 7 shows that the correlation efficiency exceeds 90% for input signals above -30 dBm. Measured adjacent channel isolation is 35 dB, while measured isolation between alternate channels is 45 dB. The frequency response of the correlator is nearly flat with approximately 0.5 dB of ripple over a 500-MHz input bandwidth.

At 1.0 V and 1.5 GHz, the chip digitizes 128 analog inputs with 2-bit ADCs and performs 6.144T 2-bit cross-correlations/s, consuming 3.735 W or 0.61 pJ/correlation/cycle. Each ADC consumes 1 mW. The baseline 1-GHz required operation is reliably achieved with a supply voltage of 775 mV. For this performance, the entire power consumption is 1.443 W, which corresponds to an energy



(a) (b)

Fig. 9. (a) False color image of the moon (red disk) captured with a prototype GeoSTAR instrument. The blue disk is a reference source. (b) Image of a person waving on building rooftop.

of 0.35 pJ/correlation/cycle. The power and frequency measurements are shown in Fig. 8. Compared to [5], this design doubles the number of correlators, doubles the bit width from 1-bit to 2-bit, and integrates ADCs on chip to avoid the need for high speed off-chip I/O. Note that doubling the bit width to 2-bit significantly improves sensitivity and reduces correlation time [14]. By dramatically reducing total power consumption and substantially increasing integration, this brief helps make low-cost real-time synthetic aperture imaging radiometry practical.

Fig. 9(a) shows a false color image of the night sky captured at 183 GHz by a prototype GeoSTAR instrument. This is with a full system with a Y-shaped 183 GHz antenna array, mixers, and filters connected to the prototype 64 × 64 mixed-signal cross-correlator chip. Fig. 9(b) shows an image of a person waving on a rooftop.

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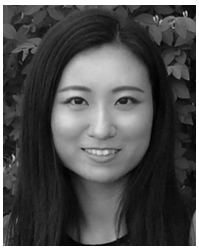

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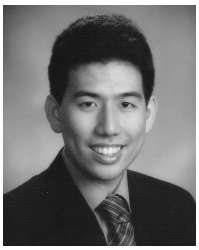

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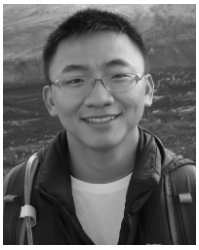
Mr. Chen received the Rackham Merit Fellowship in Intel Corporation. He did an internship with CRL, Intel Corporation, Santa Clara, CA, USA, in 2015.

Jeffrey Fredenburg, photograph and biography not available at the time of publication.



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Aaron Rocca, photograph and biography not available at the time of publication.

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Andres Tamez, photograph and biography not available at the time of publication.

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Michael P. Flynn received the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, USA, in 1995.

From 1988 to 1991, he was with the National Microelectronics Research Center, Cork, Ireland. He was with National Semiconductor, Santa Clara, CA, USA, from 1993 to 1995. From 1995 to 1997, he was a Member of the Technical Staff with Texas Instruments, Dallas, TX, USA. From 1997 to 2001, he was with Parthus Technologies, Cork. In 2001, he joined the University of Michigan Ann Arbor, MI, USA, where he is currently a Professor. His current research interests include RF circuits, data conversion, serial transceivers and biomedical systems.

Dr. Flynn is a 2008 Guggenheim Fellow. He received the 2016 University of Michigan Faculty Achievement Award, the 2011 Education Excellence Award, and the 2010 College of Engineering Ted Kennedy Family Team Excellence Award from the College from Engineering at the University of Michigan. He received the 2005–2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan. He received the NSF Early Career Award in 2004. He was a recipient of the 1992-1993 IEEE Solid-State Circuits Pre-Doctoral Fellowship. He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He served on the Technical Program Committees of the International Solid State Circuits Conference, the Asian Solid-State Circuits Conference and the Symposium on Very Large Scale Integration Circuits. He currently serves on the Technical Program Committee of the European Solid State Circuits Conference. He was the Editor-in-Chief of the IEEE JOURNAL OF SOLID STATE CIRCUITS (JSSC) from 2013 to 2016. He served as an Associate Editor of the IEEE JSSC and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.