Electromagnetic Fast Firing for Ultrashallow Junction Formation

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***Abstract*—The creation of low resistivity, ultrashallow source/drain regions in MOS device structures requires rapid thermal processing (RTP) techniques that restrict diffusion and activate a significant percentage of the implanted dopant species. While current heating techniques depend upon illumination based heating, a new technology, electromagnetic induction heating (EMIH), achieves a rapid heating of the silicon by coupling electromagnetic radiation directly into the silicon wafer. Heating rates of 125 °C/s to temperatures in excess of 1050 °C have been achieved for 75- and 100-mm-diameter wafers at input powers of 1000 and 1300 W, respectively. These ramp rates are suitable for ultrashallow junction formation, and junctions shallower than 30 nm with sheet resistances lower than 600 Ω/square have been achieved. This paper details the application of electromagnetic heating using radiation in the microwave, 2450 MHz, frequency regime. Experimental results, comparing microwave annealed implants to the well documented SEMATECH requirements, and simulations, utilizing a coupled electromagnetic-thermal computer model, of the heating process are discussed.**

***Index Terms*—Activation, anneal, dopant, junction, microwave, radiation, shallow.**

I. Introduction

THE CONTINUATION of Moore's law, as defined by the ITRS roadmap [1], predicts that the DRAM half pitch and physical gate length dimensions will fall to 80 and 32 nm, respectively, by 2005. A major requirement of this scaling plan is the reduction of power losses during device operation, primarily through the elimination of parasitic resistances. A major source of device resistance comes from the junction between the source/drain region and the channel. While the implementation of highly doped extensions in this junction region has helped minimize resistance, meeting the year 2005 requirements necessitates that these extensions have a depth and sheet resistance no greater than 22 nm and 820 Ω/square, respectively. The formation of these ultrashallow junctions, which retain an ever greater percentage of activated dopants (eventually reaching levels that exceed the solid solubility limit) in a much shallower near-surface region (eventually a zero-diffusion anneal), presents a significant obstacle to future device fabrication [1], [2].

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The aforementioned junction requirements have caused the industry to move from conventional furnace annealing (i.e., 30 min at 1000 °C) to rapid thermal processing, RTP, techniques. While the first RTP prototypes were presented in the earlier 1980s, a general loathing of both rapid heating and single wafer processing, coupled with loose processing margins and the entrenched position of large batch furnaces, prevented the acceptance of single wafer RTP until the earlier 1990s. A complete review of the history of RTP can be found in [3]. Once accepted, RTP processes quickly moved from 50 °C/s ramp rates and 60-s soak times to ramp rates as high as 450 °C/s with zero second, or "spike," soak times [4]. These state-of-the-art RTP systems, however, only satisfy the current technology requirements and have not proven adequate for the next generation of device fabrication [5].

Alternative anneal technologies, including laser melt, laser submelt, millisecond FLASH RTP, and solid phase epitaxial (SPE) regrowth, have attempted to fill the looming technology void but have achieved only limited successes to date [5]. Laser melt, which activates the implanted dopant species by literally melting and recrystallizing the implanted surface region on nanosecond time scales, presents significant integration issues since the melt/recrystallization process degrades the entire gate structure. Laser submelt avoids this issue by not exceeding the melting point of silicon. While the overall time at temperature (tens of nanoseconds to reach 1200 °C) has created a no-diffusion anneal process, it is very difficult to achieve high levels of activation on such short time scales. Millisecond RTP, or FLASH, provides results parallel to laser submelt, but the overall power requirements to heat a 300-mm wafer to temperatures greater than 1200 °C in only a few milliseconds raise questions about the commercial viability of this technique. Finally, SPE regrowth at temperatures below 700 °C provides no-diffusion junctions ($X_j \sim 20$ nm) with moderate sheet resistances (Rs $\sim 800\ \Omega/\mathrm{square}$) [5]. The overall post anneal damage, however, is four orders of magnitude larger than the accepted range, creating such high leakage currents that the transistors are virtually inoperable.

Of the many techniques listed in the SEMATECH roadmap [1] for ultrashallow junction formation, rapid microwave annealing has gone virtually untested. A few attempts at heating silicon with gyrotron-generated, millimeter radiation (i.e., 110 GHz, near the upper end of the microwave frequency range) has shown success [6], but the extreme costs and complexity involved with building and maintaining a gyrotron based system

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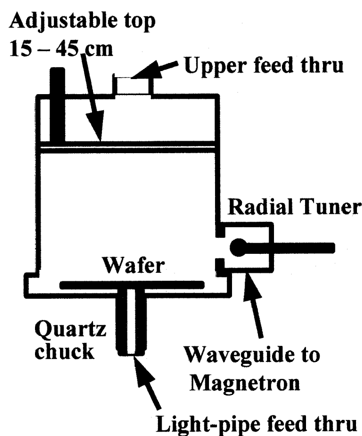


Fig. 1. Resonant cavity used for microwave (2.45 GHz) heating. Silicon wafer is placed at the bottom of the cavity, where the transverse components of the electric field are strongest.

has limited such experiments to the realm of basic research. Recent advances in microwave heating technology [7], however, have allowed silicon wafers to be rapidly heated (>125 °C/s) to temperatures in excess of 1000 °C with electromagnetic radiation ranging from 1 MHz to 10 GHz. These frequencies are well below the gyrotron range and therefore easily accessible at low cost. This paper provides a brief review of the equipment necessary for microwave heating, evaluates the heating efficiency of this technique, compares the anneal results to those achieved using the most prominent flash-lamp rapid thermal processing (RTP) tools [4], [8], provides detailed simulation results of the heating process, and evaluates the overall advantages and limitations of microwave annealing.

II. Experimental Apparatus

The basis for efficient microwave annealing is rooted in a broader technique more commonly referred to as electromagnetic induction heating (EMIH) [9], [10]. This technique rapidly (125 °C/s) and volumetrically heats silicon to temperatures in excess of 1050 °C by coupling electromagnetic radiation, in the millimeter (30 GHz–300 GHz), microwave (300 MHz–30 GHz), or radio (3 MHz–300 MHz) frequency regimes, directly into the silicon wafer. The extremely weak dipole response of silicon [11], [12] makes the coupling of electromagnetic energy into silicon a nontrivial process, and the requirements for efficiently heating silicon with microwave radiation are detailed in a previous publication [7]. Because of the reasons listed in [7], microwave annealing was performed in the resonant cavity shown in Fig. 1. The diameter of the cavity was 17 cm and the height was left adjustable to tune in specific modes. A radial tuning stub helped minimize reflected power and up to 3000 W could be supplied from a fixed frequency (2450 MHz) magnetron source. Although several resonant modes were available, the dominant TM111 and TM011 modes were primarily used. Wafers of 75 and 100 mm diameter were supported by a hollow quartz cylinder positioned 5 mm above the cavity bottom to optimize power transfer to the wafer. Finally, temperature was measured in the center of the wafer with an optical light pipe that fed through the bottom of the cavity.

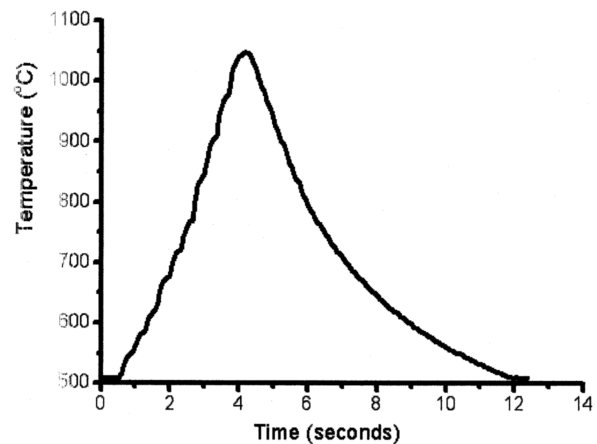


Fig. 2. Typical spike anneal temperature transient for microwave annealing.

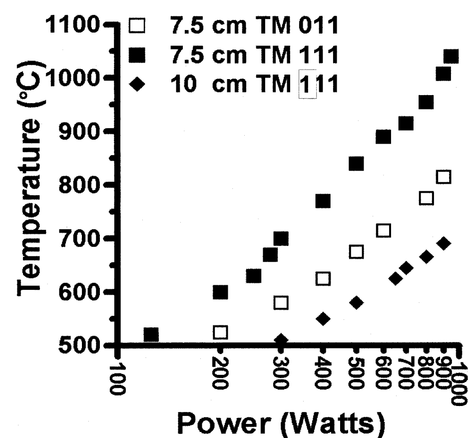


Fig. 3. Semilog plot of temperature and power during microwave annealing.

III. Heating Results

Heating rates of 125 °C/s up to and beyond 1050 °C were achieved. These results are comparable to commercially available lamp based RTP systems [4], [8] and a typical temperature transient is shown in Fig. 2. A semi-log plot of steady-state temperature as a function of power is shown in Fig. 3. The fourth root dependence of temperature on power is apparent, indicating a loss mechanism dominated by radiation, as expected for this temperature regime. The loading effect between 75- and 100-mm wafers is apparent as well as the efficiency of the TM111 mode as compared to the TM011 mode. The difference in efficiency between these two modes is attributed to the significantly larger coverage of the wafer by the transverse electric field during operation in the TM111 mode. This issue will be discussed in detail through the simulations performed.

IV. Simulation Results

Uniformity is critical to any rapid heating process. The dependence of microwave heating on the intensity of the electric and magnetic flux transverse to the wafer makes the heating uniformity highly susceptible to any nonuniformity in the electric/magnetic field pattern. Because these microwave heating experiments were performed in a single mode resonant cavity, a nonuniform dominant mode pattern may dictate a nonuniform

heating profile across the wafer. Finite-difference time-domain (FDTD) simulations were run to examine the electric and magnetic flux intensity spatially within the wafer and to evaluate the subsequent effect on heating uniformity.

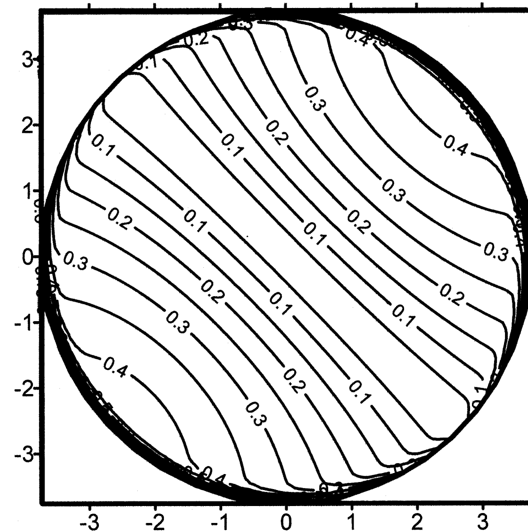
The rationale for utilizing FDTD to simulate the electromagnetic (EM) fields can be found in [13]. The equations derived in [13] break the chamber down into a two-dimensional (2-D) grid and simultaneously solve for the radial, r, axial, z, and azimuthal, ϕ, electric, E, and magnetic, H, field components in each cell of the 2-D radial coordinate system (radial and axial dimensions). The azimuthal component is then obtained by taking advantage of the physical symmetry of the cylinder to assemble the Fourier components around the azimuthal direction, as dictated by the resonant mode. Specific details of this reconstruction process are located in a typical electromagnetics textbook [11].

The simulated electric and magnetic flux intensities determined within the wafer were then inserted into a thermal FDTD simulation, (1), comprised of a grid exactly matching the EM

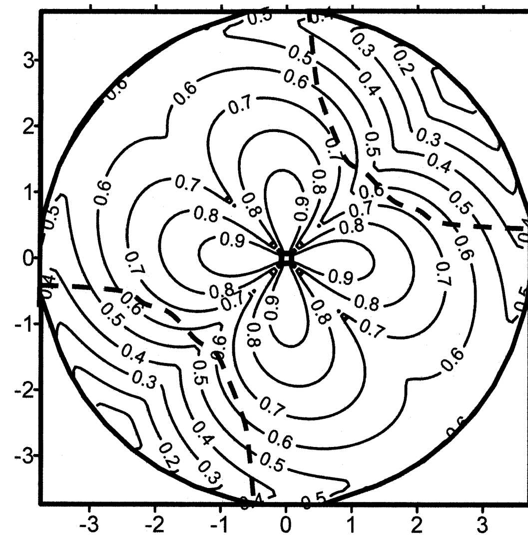
$$\frac{\rho_T C_T}{K_T}\frac{\partial}{\partial T}T = \left[\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial Z^2} + \frac{1}{r^2}\frac{\partial^2 T}{\partial \phi^2}\right] + \frac{P}{K_T} \quad (1)$$

FDTD simulation, so that the temperature evolution could be extracted. In this equation, P is the net power density, defined as absorbed electromagnetic energy minus radiation losses, k_T is the thermal conductivity, c_T is the specific heat of silicon, ρ_T is the density of silicon, r is the radial dimension, ϕ is the azimuthal dimension, Z is the axial dimension, T is the temperature, and t is time. The EM power was stepped into the thermal code in a staircase type fashion that followed the same basic philosophy of similar electromagnetic/thermal code methodologies [14]–[16]. To start, the wafer temperature was set at 500 °C and temperature dependent parameters such as conductivity calculated accordingly. The EM code was then run to steady-state and the absorbed power inserted into the thermal code, which was subsequently run to steady-state as well. The wafer parameters were then updated as a function of temperature, and the process repeated until the maximum or target temperature was reached. Despite the inherent approximations involved in this process, the coupling of these two codes works quite well since the time constant to reach steady state for the EM code is several orders of magnitude faster than for the thermal code, allowing the former to be constantly updated into the latter.

The physical reality of the microwave chamber was adhered to as closely as possible during the simulation. Because the wafer was located 5 mm above the bottom of the chamber, a number of free space grids equaling 5 mm was left between the wafer and the conductive barrier representing the cavity bottom. The quartz chuck upon which the wafer sat was not incorporated into the simulation. The simulated cavity was a perfectly round cylinder of infinite conductivity, but the actual cavity was composed of brass and contained three small view-ports, approximately 2 cm in diameter, which caused small perturbations from the idealized cylindrical symmetry. The EM power in the simulation was introduced through a current source located in the center of the grid, but for practical purposes power was input through a port at the base of the microwave cavity. Finally, wafer rotation during heating was reproduced by averaging the fourier components that were used to assemble the azimuthal components of the 2-D code into the full 3-D wafer representation. This averaging provides perfect azimuthal symmetry, as would be expected from an idealized rotational heating system.



(a)



(b)

Fig. 4. (a). Simulated axial electric field (Ez) intensity for a 7.5-cm-diameter wafer heated in the TM111 mode. The temperature of the wafer is 1050 °C, and the field strength has been normalized. (b) Simulated transverse electric field (parallel to the wafer) intensity for a 7.5-cm-diameter wafer heated in the TM111 mode. The temperature of the wafer is 1050 °C, and the field strength has been normalized. The transverse field is approximately 20 times the intensity of the axial field shown in (a).

Contour maps of the axial (normal to the wafer) and transverse (parallel to the wafer) electric field intensity across the wafer surface for the TM111 mode are shown in Fig. 4(a)–(b). The resulting temperature map is shown in Fig. 5. The axial and transverse electric fields for the TM011 mode, along with the simulated temperature, are shown in Fig. 6. The rotational TM111 mode involves rotating the wafer at a rate of 60 revolutions per minute while heating in the TM111 mode. The axial and transverse electric fields for the rotational TM111 mode, along with the simulated temperature, are shown in Fig. 7.

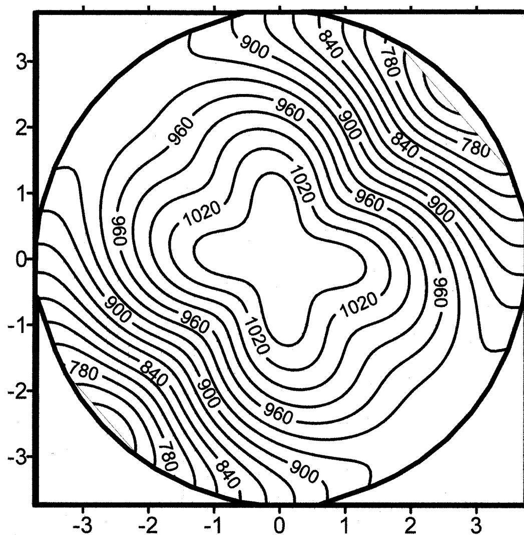


Fig. 5. Simulated steady-state temperature map for a 7.5-cm-diameter wafer heated in the TM111 mode. $\mathrm{Max\ Temp} = 1050\ °\mathrm{C}$, $\mathrm{Min\ Temp} = 740\ °\mathrm{C}$.

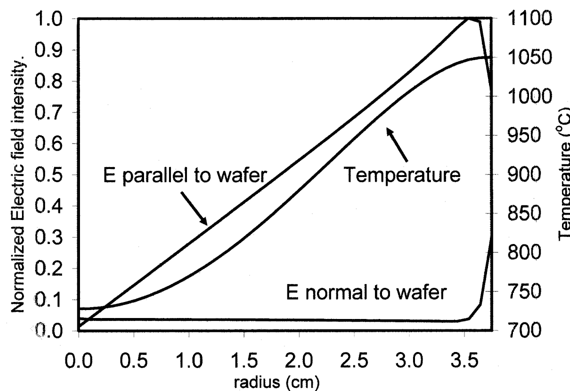


Fig. 6. Simulated electric field intensities for a 7.5-cm-diameter wafer heated in the TM011 mode. Because the field (and therefore temperature) pattern is azimuthally symmetric, a single cut through half the wafer is shown. The maximum temperature of the wafer is 1050 °C .

The temperature was measured experimentally at three point points along the wafer radius and included in Fig. 7. Because the TM011 and TM111 rotational modes are azimuthally symmetric, the electric field and temperature data are represented by a single cut in the radial direction.

The distinct features of each mode pattern are clear. The TM111 mode exhibits an hourglass pattern [see dashed lines in Fig. 4(b)] with the transverse field intensity being strongest within a clover leaf region at the center of the hourglass and the axial field intensity being strongest outside the hourglass. The TM011 mode shows a steep radial gradient with most of the transverse field intensity located at the edge of the wafer while the maximum axial field intensity is focused in the center of the wafer. Note that continuity of the total electric field, within the physical confines of the chamber, means that the transverse and axial electric fields have alternating maximums and minimums. Rotating the wafer averages out, in time, the azimuthal asymmetry of the TM111 mode, eliminating the hour glass pattern effect of the TM111 mode, but a distinct radial gradient (center hot, edge cool) still exists.

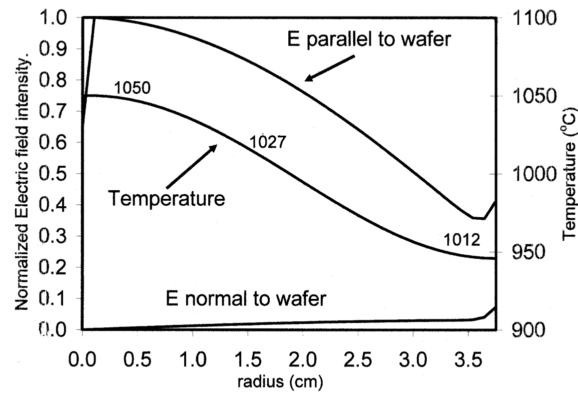


Fig. 7. Simulated electric field intensities for a 7.5-cm-diameter wafer heated in the rotational TM111 mode. Because the field (and, therefore, temperature) pattern is azimuthally symmetric, a single cut through half the wafer is shown. Experimentally measured temperatures are shown as text. The maximum temperature of the wafer is 1050 °C.

The "hot" zones for each mode correspond with the areas of maximum transverse electric field intensity (the approximate complement of the axial electric field), and it is clear that the electric flux intensity transverse to the wafer surface has a dominating impact on the overall temperature pattern. Heating in the TM111 mode results in an empirically determined temperature nonuniformity of 13.6%, and rotating the wafer at 60 rpm reduces the temperature nonuniformity to 3.6%. The overall result is clear: the intensity of the transverse electric field directly affects the final wafer temperature, and any nonuniformity in the transverse electric field intensity across the wafer surface creates a similar nonuniformity in the wafer temperature.

It is apparent that uniformity is the dominant obstacle to microwave annealing in a resonant cavity since commercially available RTP systems are generally expected to provide less than 1% nonuniformity in sheet resistance. This issue, however, can be overcome by constructing a dual mode cavity in which both the TM111 and TM011 modes simultaneously power the cavity. The uniformity could be controlled by adjusting the power of the TM011 mode (edge hot) with respect to the TM111 mode (center hot) until the radial gradient is eliminated. The main drawback to such a system is the requirement of a second microwave power source whose frequency is selected so that both modes are in resonance for a given set of cavity dimensions. This would necessitate a feedback system that adjusted the power of both modes as well as the physical height of the cavity. While complicated and more expensive than the current experimental apparatus, this design is well within the realm of present day technology.

The resonant cavity approach is not the only means by which microwave radiation can be used to rapidly heat silicon wafers. An alternative system involves a multimode cavity whose physical dimensions are many times larger than the free space wavelength of the incident radiation. Because no single mode is resonant, dozens of random and unique modes simultaneously deposit energy into the silicon wafer. The effective mode pattern is an average of all of these modes, with the resultant electric field intensity having excellent spatial uniformity across the wafer surface. One such system [17] has reported temperature ramp rates greater than 150 °C/s with a cross

wafer nonuniformity less than 1%. The main drawback to this design is the increased power and thus cost of the microwave power supply. Because the wavelength of the 2450-MHz radiation used in the resonant cavity is 12.25 cm, a system size greater than 1 m is required to achieve a truly multimode configuration. The power densities needed to obtain the same heating rates as those in a smaller single-mode system require a much greater input microwave power for the larger system. This requirement for a very large, very high-power system can be avoided by going to higher frequencies. At gyrotron frequencies (30 GHz and above), wavelengths of 1 cm or less can be achieved and much smaller multimode cavities are possible, as in [17]. However, the jump from magnetron (currently used for high-power 2450-MHz microwave generation) to gyrotron technology incurs a significant capital investment.

V. USJ Results

The effectiveness of microwave heating for ultrashallow junction formation was evaluated by spike annealing several shallow implanted samples. The implant conditions of the samples shown were BF_2 at 4500 eV, Fig. 4, BF_2 at 2200 eV, Fig. 5, and BF_3P^2LAD at 200 V, Fig. 6. The BF_2 species were beam-line implanted, and pulsed plasma doping [8], [18] was used to implant the BF_3 species. In pulsed plasma doping, the implanted dopant atoms are not accelerated and mass selected as in beam-line ion implantation. Instead, the implant depth is controlled by the voltage applied to the chuck. While this applied voltage is analogous to implant energy, the two terms are not completely interchangeable, as discussed in [18]. As a result, beam line implants are referred to by implant energy, eV, and P^2LAD implants by implant voltage, V. All samples had a dose of $10^{15}/\text{cm}^2$. It has been shown for lamp-based RTP [4], [19] that reducing the concentration of oxygen, $[O_2]$, in the ambient during the anneal process limits the diffusion and enhances the activation of boron with an optimal anneal condition occurring between 33–1000 ppm oxygen in a nitrogen purge. As a consequence, the microwave anneal experiments were split between an uncontrolled ambient, approximately 21% O_2, and an ambient that was purged with N_2 to a controlled $[O_2]$ of 100 ppm.

The 4500-eV anneals, Fig. 8, performed in a 21% O_2 ambient show significant diffusion at 1050 °C. At 950 °C, only moderate diffusion occurs, but instead of becoming "box-shaped" the profile tails out. The "box-shaped" dopant profile is preferred because the total number of dopants contained within the junction depth is maximized, resulting in a significantly lower sheet resistance. The sharper drop off in concentration near the edge of a "box-shaped" profile junction also results in a smaller depletion width, providing superior electrical isolation between the n- and p- type regions. Both of the anneals performed in an ambient with a controlled $[O_2]$ of 100 ppm show a more "box-shaped" profile, and an improved sheet resistances (Rs) as compared to the anneals performed in an uncontrolled ambient. The 2200-eV anneals, Fig. 9, also show considerable diffusion when performed in an uncontrolled ambient. Controlling the $[O_2]$ and reducing the temperature limits this diffusion and improves the Rs. For example, the 950 °C anneal had an Rs of 519 Ω/square and a junction depth of 30 nm, placing this data point within the technology node requirements for 100-nm devices [1].The effect of $[O_2]$ concentration is illustrated yet again during annealing of the 200-V plasma—doped BF_3 samples, Fig. 10. At 1050 °C, the junction depth and Rs are reduced by 50 nm and 828 Ω/square, respectively, when the oxygen concentration of the ambient during the anneal is reduced to 100 ppm. Anneals performed at subsequently lower temperatures result in similar "box–shaped" profiles, slopes of ~6 nm/decade, with

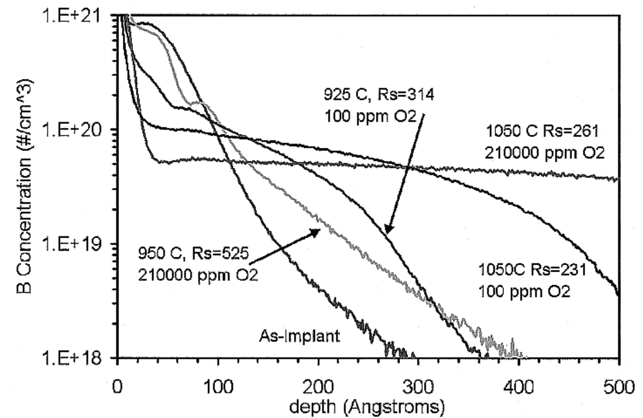


Fig. 8. 4500-eV BF_2 anneal results.

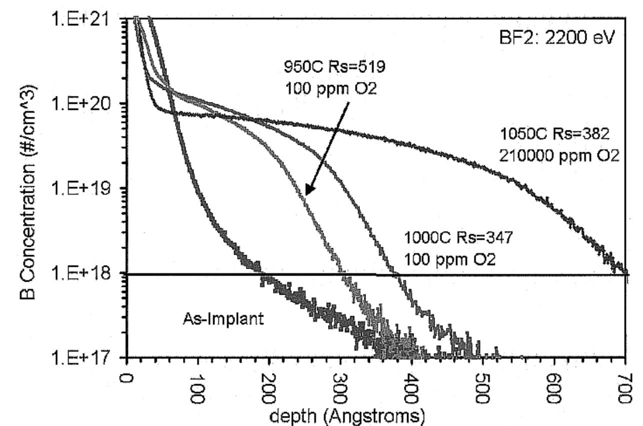


Fig. 9. 2200-eV BF_2 anneal results.

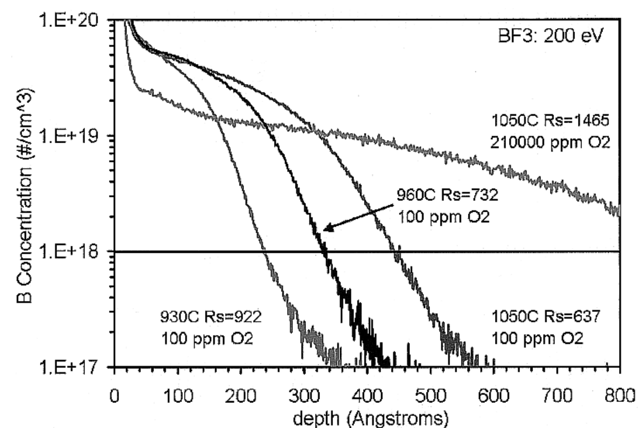


Fig. 10. 200-V BF_3P^2LAD anneal results.

TABLE I
AMOUNT OF BORON DOSE RETAINED IN THE SILICON FOR 2200 eV, $10^{15}/cm^2 BF_2$ IMPLANTS AND 800 V, $5 * 10^{15}/cm^2 P^2$LAD IMPLANTS. ERROR RANGE FOR THE SIMS ANALYSIS IS 5%. THE FINAL MICROWAVE SPIKE ANNEAL TEMPERATURE WAS 1000 °C FOR ALL SAMPLES AND, THE OXYGEN CONCENTRATION OF THE ANNEAL AMBIENT VARIED AS SHOWN

Implant species and energy	$[O_2]$ in the anneal ambient	Retained B dose
2200 V BF_2	100 ppm	1.68*10^{14}
2200 V BF_2	210000 ppm	9.55*10^{13}
800 V BF_3	33 ppm	1.26*10^{14}
800 V BF_3	100 ppm	1.20*10^{14}
800 V BF_3	300 ppm	1.17*10^{14}
800 V BF_3	1000 ppm	9.77*10^{13}
800 V BF_3	210000 ppm	5.75*10^{13}

consistently shallower junction depths and higher sheet resistances. These points also form a curve that satisfies the 100-nm technology node as defined by the ITRS roadmap [1].

The dramatic differences witnessed when annealing in an uncontrolled versus a controlled low ppm O_2 ambient can be partially attributed to the oxidation of the top 30–40 A of silicon during the anneal process. After implantation, the largest fraction of the implanted dose lies in the extreme near surface, top 5 nm, of the silicon, most of which is well above the solid solubility limit for boron in silicon. For superior junctions to form, this dose must diffuse into regions where the boron concentration is below the solid solubility limit, allowing it to become substitutional. When annealing in an oxidizing ambient, it is foreseeable that a sizable fraction of the dose becomes trapped within the thin oxide layer that forms during the high temperature step of the anneal process. This is especially true for impurities like boron, which, unlike phosphorous, are excellent network formers in glasses [20]. The oxide thickness is difficult to gauge since ellipsometric measurement of very thin dielectric films is highly inaccurate when the chemical composition is not precisely known. Nevertheless, the amount of boron dose trapped in the oxide can be indirectly measured by stripping the grown oxide layer before SIMS analysis and calculating the retained dose. This was done for two 2200-eV BF_2 implanted samples (cut from the same wafer after implant) that were microwave spike annealed to 1000 °C in different ambient conditions. The retained doses for the sample annealed in a 21% oxygen ambient and for the sample annealed in an ambient whose $[O_2]$ was limited to 100 ppm were $9.55 * 10^{13}$ B/cm^2 and $1.68 * 10^{14}$ B/cm^2, respectively. These results clearly point to an increased consumption of dose when the anneal process is performed in an oxidizing ambient. A summary of the amount of boron dose retained in the silicon after several of the anneals can be found in Table I.

Because a significant quantity of boron is trapped in the surface oxide, maintaining an $[O_2]$ of 100 ppm in the ambient during the anneal limits the oxide growth, which limits the boron dose loss, leaving the boron free to diffuse into the silicon. When the thermal budget is adequately restricted, the boron will diffuse from the super-saturated near surface region into the next 20 nm of silicon without being driven deep into the wafer. This concentration enhanced diffusion (CED) effect that occurs in highly doped silicon layers facilitates this short range diffusion, thereby enhancing the formation of a "box-shaped" boron concentration profile [21]. CED is a by-product of the relatively immobile nature of substitutional boron, which must overcome an energy barrier associated with detaching itself from the silicon site in which it resides before being free to diffuse, as compared to interstitial boron, which sees no such energy barrier. After a high dose implant, most of the boron within the top few nm of the surface is interstitial and therefore very mobile, while most of the boron at the end of the junction depth (concentration $<10^{18}/cm^3$) is substitutional and, therefore, relatively immobile. As a result, the average mobility of the boron atoms increases with atomic concentration, and impurity atoms in the extreme near surface region will diffuse into the silicon at a disproportionately higher rate than atoms located only a few tens of nanometers deeper in the silicon. Furthermore, as the highly mobile interstitial atoms move into the silicon and find substitutional sites, their mobility decreases, dramatically slowing the diffusion process. The end result is a "box-shaped" diffusion profile, as witnessed in Figs. 8–10. By preventing the loss of this near-surface high boron dose to excessive surface oxide growth, the CED driving force is able to dominate the kinetics over incorporation into the surface oxide. The resultant "box-shaped" profile forms a more abrupt junction and incorporates a higher concentration of active dopant in the junction region.

An additional benefit to annealing in an ambient that has a low $[O_2]$ is the reduction of oxygen enhanced diffusion, OED, effects [4], [19]. OED first attracted attention over forty years ago when unacceptably high levels of oxygen became incorporated in the silicon as it was being pulled from the melt. The ensuing studies of this poor quality silicon [22], [23] revealed a stable oxygen-atom-Si-vacancy pair association that prohibited the interstitial boron atoms from moving onto the now partially occupied silicon sites. The result was a larger concentration of mobile boron, driving faster diffusion, and a lower concentration of activated boron within the junction region, forcing a higher sheet resistance. As the quality of silicon wafer processing improved, OED became less of an issue. With the advent of ultrashallow implants, however, the incorporation of oxygen from the anneal ambient into the highly doped, near-surface region became a prime source for oxygen enhanced diffusion. Previous studies [19] show that even moderate concentrations of oxygen prohibit the activation of boron atoms, and SIMS results of the samples annealed for this study show that oxygen incorporation falls by 65% when the $[O_2]$ in the anneal ambient is reduced from 21% to 100 ppm during spike anneals to 1000 °C. These results, along with the consumption of dose by the oxide growth, are believed to explain the combined observations of higher sheet resistances and enhanced diffusion, especially in the tail ($10^{17}/cm^3$ to $10^{18}/cm^{18}$) of the profile, when the samples were annealed in an uncontrolled, oxygen-rich ambient.

The effect of $[O_2]$ on junction formation during microwave annealing was further studied by spike annealing (125 °C/s to 1000 °C) samples, implanted with $10^{15}/cm^2 BF_2$ ions at an energy of 4500 eV, at various $[O_2]$ in the ambient. The results, Fig. 11, indicate shallower junctions as the $[O_2]$ in the ambient, and subsequently, oxygen-enhanced diffusion,

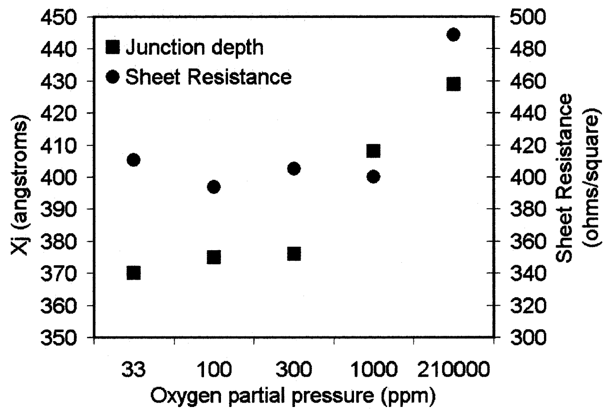


Fig. 11. 4500 eV, $10^{15}/cm^2 BF_2$ implant samples spike annealed to 1000 °C at different background oxygen concentrations to illustrate the effect of oxygen when ultrashallow junctions are formed using microwave annealing.

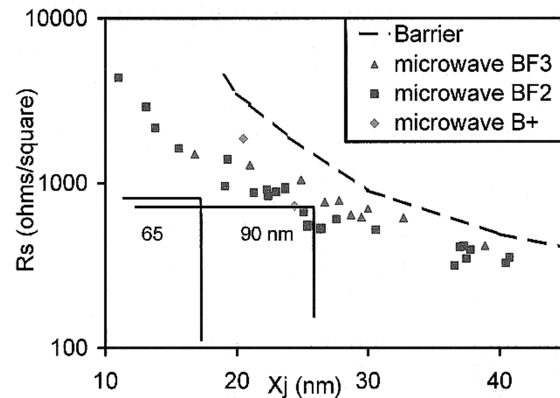


Fig. 12. $Rs - X_j$ curve showing microwave anneal results. The 65- and 90-nm technology node boxes are shown. The BF_2 implants clearly satisfy the 90-nm node.

is reduced. While the sheet resistance initially decreases as the $[O_2]$ is reduced, it flattens out below 1000 ppm. This has been seen in lamp-based RTP studies of both B+ and BF_2 implanted species [19] and is attributed to the saturation of active dopant concentration. Because sheet resistance—for ideal "box-shaped" junctions—is defined as resistivity (Ω·cm) divided by junction depth (cm), and because the resistivity depends upon the total number of activated dopant atoms per unit volume of silicon, a value that saturates at a physically determined maximum, the sheet resistance is expected to reach a natural minimum value as the junction depth is reduced. The optimal ambient for microwave annealing of 4500 eV BF_2 implants falls between 33–1000 ppm oxygen in a nitrogen purge. It is reasonable to assume that this same range in $[O_2]$ would be suitable for lower BF_2 implant energies (e.g., $\sim$300–2000 V). It may be further speculated that the optimal oxygen concentration should decrease with even lower BF_2 implant energies since a larger fraction of the implanted dose is contained within the ultra near-surface region most exposed to oxygen incorporation from the ambient. These results agree with the profile engineering illustrated in Figs. 8–10, and it is possible that these results could be improved upon once the "best" anneal ambient is determined.

Plotting sheet resistance and junction depth together, Fig. 12, gives an overall summary of the results. The labeled boxes indicate the technology nodes as determined by the ITRS roadmap [1]. It is clear that microwave annealing satisfies the 90-nm node and with further optimization may satisfy the 65-nm node, making these results comparable to the best results reported to date using flash-lamp anneal technology [4], [24]. It should further be noted that the optimal temperature for microwave annealing BF_2 implants is 950 °C while for lamp-based RTP, it is 1070 °C [24]. The ramp rates used in these experiments, 125 °C/s, are lower than the 450 °C/s used in the best lamp-based processes [4]. Future experiments utilizing more rapid ramp rates should further restrict any diffusion of the boron in the tail region of the profile.

The temperature of the wafer during microwave annealing was monitored with a light pipe. Great lengths were taken to ensure the accuracy of the temperature measurement as detailed in a previous publication [25]. First, thermally reactive paints, which liquefy once a certain temperature is reached, were used and the results compared favorably to the light pipe data. Next, the light-pipe was calibrated by measuring the temperature of a silicon wafer while it was heated in a conventional furnace, whose temperature was controlled by a thermocouple. Finally, a rigorous chemistry-based calibration study was conducted. Solid-state reaction mechanisms were monitored and used to correlate the temperature as measured by the light-pipe to the temperature extracted from the solid-state reactions [25]. Note that in the microwave-annealing system, all surfaces are cold except for the heated silicon wafer. The light-pipe sensor *only* measures the temperature of the hot wafer, and is not influenced by other potential sources of light contamination from hot objects (either surface or lamps) that exist in other RTP systems.

The difference in optimal anneal temperature may indicate the presence of an additional driving force, driven by the high frequency electric fields, which stimulates the diffusion of the implanted dopants. It has been shown experimentally for non-silicon materials that microwave ponderomotive forces drive the diffusion of certain species of atoms at rates that are several orders of magnitude greater than thermal driving forces alone [26], [27]. It has been further illustrated theoretically [28], [29] that high frequency electric fields can give rise to these same ponderomotive forces in silicon. A possible conclusion along these lines may be that these ponderomotive forces stimulate the diffusion of boron from the ultra-near surface of the wafer into the shallow junction region. This mechanism does not seem to specifically enhance the activation of boron but rather to create a more "box-shaped" dopant profile at a lower anneal temperature. As a result, this stimulated diffusion lowers the sheet resistance achieved for a given spike anneal temperature by increasing the total number of activated boron atoms within the junction region. It further appears that the lower temperature at which the anneal occurs restricts the diffusion in the tail region of the profile.

Other mechanisms, not directly related to the high frequency electric fields present during microwave annealing, may be responsible for this moderate increase in surface diffusion. Seebauer *et al.*, have shown experimentally [30], [31], that high intensity radiation in the optical spectrum affects the surface diffusion of impurity species in silicon during high temperature

thermal processing. While this high intensity optical radiation is present during lamp-based annealing, the microwave chamber is “dark,” and no optical radiation is present. The results presented in [30] and [31] do show enhanced surface diffusion for boron when no optical radiation is present. There are, however, several important differences. The experiments performed by Seebauer *et al.* were in an ultrahigh vacuum, for long durations of time (approximately 1 h), and the implanted species was boron. The optimized anneals shown here were performed in 100 ppm oxygen in a nitrogen purge, the time scale was very short (several seconds) and the boron was co-implanted with fluorine using either a BF_2 source gas or through the BF_3P^2LAD process. Downey *et al.*, have shown the importance of the anneal ambient on diffusion [19], as also discussed in this paper, and several authors [32], [33] discuss the role that fluorine plays on the diffusion of boron in silicon. R.B. Fair especially discusses the role of both fluorine and optical illumination on the diffusion of boron in SiO_2 [34], although not specifically in silicon. Because of these important differences, it is difficult to draw definitive conclusions on the role that optical radiation (or the lack thereof) plays during microwave annealing. This is an area of further study, and experiments are being planned to determine more specifically how the phenomena uncovered by Seebauer affects the diffusion of boron during microwave RTP.

VI. Conclusion

Microwave annealing, a novel RTP technique, is similar in many ways to the more conventional lamp-based RTP systems. Both techniques show the same oxygen enhanced diffusion trends for BF_2 implants, and both techniques satisfy the 90-nm technology node. There are, however, several differences that warrant further study. From a commercial standpoint, the greatest obstacle to the implementation of microwave annealing as a practical RTP technology is the uniformity of the electric field intensity across the wafer surface. This issue may be overcome through careful cavity design utilizing either a dual or multimode system or wafer rotation and long wavelength sources and cavities. From a basic physics viewpoint, evaluating the kinetics of diffusion and activation in the presence of high frequency electric fields and high intensity optical radiation—with and without the co-implantation of fluorine, and in a controlled, low ppm O_2 ambient versus an uncontrolled ambient—presents a framework for future research.

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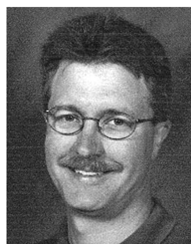

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