Batch Mode Micro-Electro-Discharge Machining

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***Abstract*—This paper describes a micro-electro-discharge machining (micro-EDM) technique that uses electrode arrays to achieve high parallelism and throughput in the machining. It explores constraints in the fabrication and usage of high aspect ratio LIGA-fabricated electrode arrays, as well as the limits imposed by the pulse discharge circuits on machining rates. An array of 400 Cu electrodes with 20 μm diameter was used to machine perforations in 50-μm-thick stainless steel. To increase the spatial and temporal multiplicity of discharge pulses, arrays of electrodes with lithographically fabricated interconnect and block-wise independent pulse control resistance–capacitance (*RC*) circuits are used, resulting in $>100\times$ improvement in throughput compared to single electrodes. However, it was found to compromise surface smoothness. A modified pulse generation scheme that exploits the parasitic capacitance of the interconnect offers similarly high machining rates and is more amenable to integration. Stainless steel workpieces of 100 μm thickness were machined by 100 μm $\times$ 100 μm square cross-section electrodes using in 85 s using an 80-V power supply. Surface smoothness was unaffected by electrode multiplicity. Using electrode arrays with four circuits, batch production of 36 WC-Co gears with 300 μm outside diameter and 70 μm thickness in 15 min is demonstrated. [692]**

***Index Terms*—Electro-discharge machining (EDM), high aspect ratio, LIGA, metal microstructures.**

I. Introduction

MICRO-ELECTRO-DISCHARGE machining (micro-EDM) is an attractive microfabrication technique that can be used to cut any electrically conductive material, including steel, graphite, silicon [1], and magnetic materials [2], [3], including permanent magnets [4]. It involves the sequential discharge of electrical pulses between a microscopic electrode and the workpiece while both are immersed in a dielectric oil [5]. The pulse discharge timing is controlled by a simple resistance–capacitance (*RC*) circuit. The electrode is conventionally a cylindrical metal element which is 5–300 μm in diameter. Although it has been commercially used for applications such as ink-jet nozzle fabrication, traditional micro-EDM is limited in throughput because it is a serial process. The use of a single electrode limits not only the throughput but also precision because the electrodes themselves are individually shaped by using a micro-EDM technique, wire electro-discharge grinding (WEDG) [6], and variation may occur in the electrode shape.

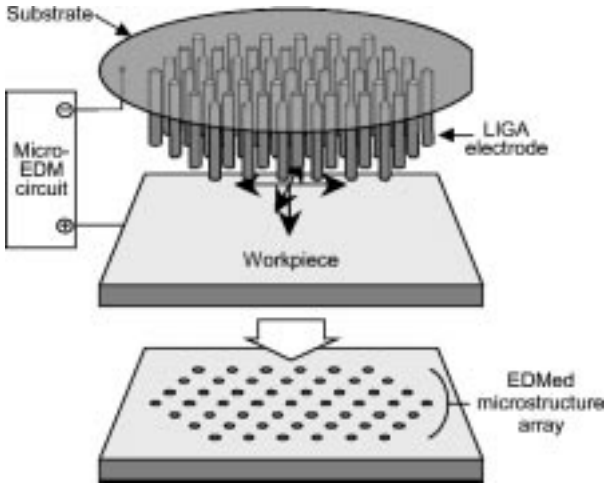

Fig. 1. Concept of batch mode micro-EDM. This diagram shows a basic scheme that all electrodes are connected to one pulse generating circuit through electroplating base on substrate.

To overcome these throughput and material issues that exist in these technologies, batch mode micro-EDM that uses LIGA-fabricated electrodes has been investigated (see Fig. 1). The LIGA process uses X-ray lithography to form high aspect ratio molds for electroplated structures [7]–[10]. In past efforts, it was demonstrated that electroplated Cu electrodes provide acceptable wear resistance [11]. It was also shown a parallel machining for perforations in stainless steel by using 3×4 arrayed electrodes with 100 μm diameter and 500 μm pitch could be achieved. Sequential application with electrode arrays was subsequently demonstrated to produce a 1-mm long WC-Co super hard alloy mechanical processing tool [12]. This paper presents new electrode and circuit configuration that improve the throughput by $>100\times$.[1] Section II describes the fabrication and wear of the electrode arrays; Section III presents an advanced approach to accelerate machining rate by using electrically partitioned electrode arrays that intend to achieve independent discharge pulses timing; whereas Section IV presents the impact of parasitic capacitance upon surface roughness. A thyristor based model for the electro-discharge is used to predict scaling trends. A new circuit configuration that can not only solve the problems but also make the approach more practical is discussed.

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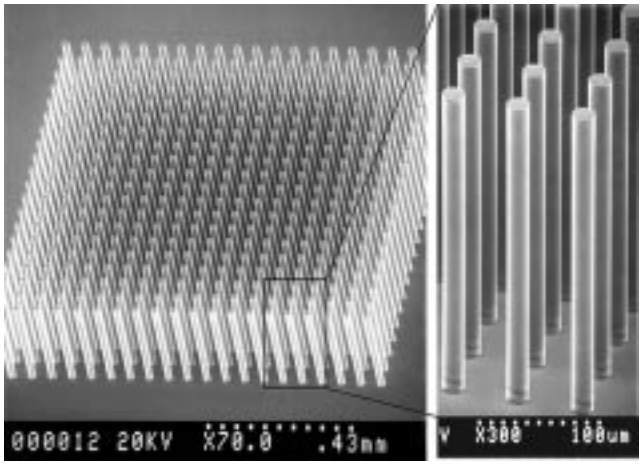


Fig. 2. A 20 × 20 array of LIGA fabricated Cu electrodes with 20 μm diameter and 300 μm height.

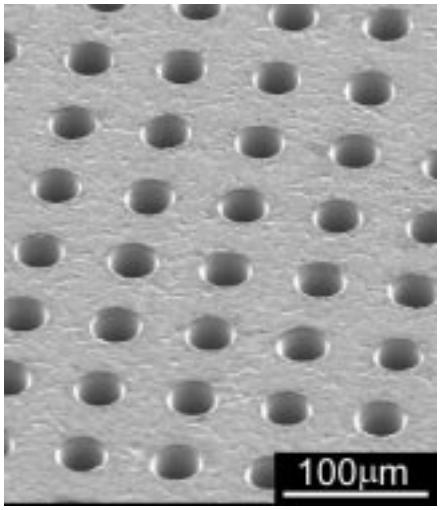
II. Electrode Fabrication and Usage

Several different arrays were fabricated by the LIGA technology to examine scaling effect this time. Fig. 2 shows a 20×20 array of electrodes with 20 μm diameter and 60 μm pitch. The electrodes have 300 μm structural height were formed from electroplated Cu on a Ti/Cu electroplating base deposited on a Si substrate. This array represents a 30× increase in electrode count and 70× increase in spatial density over past efforts [11]. In conventional micro-EDM, the workpiece is held stationary in a horizontal position, while a single cylindrical electrode is scanned across its surface. The electrode is simultaneously rotated at 3000 rpm in order to increase uniformity and prevent local welding to the workpiece. This rotation is clearly not possible when using arrayed electrodes. Instead, the electrodes are placed on a vibrator that dithers them along the axis of approach. The workpiece is scanned across the probe array in this arrangement.

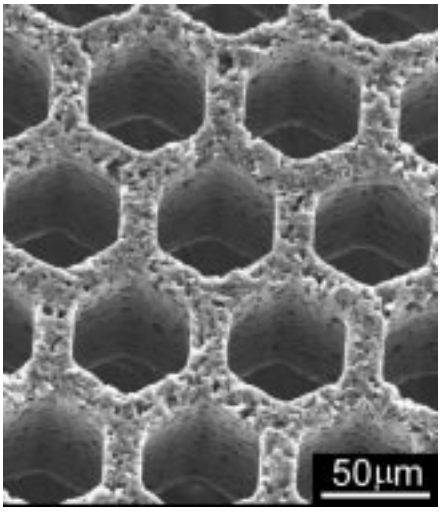
Using the electrodes shown in Fig. 2, an array of 400 perforations was successfully produced in 50 μm thick stainless steel by experimental apparatus based on the Panasonic MG-ED72W micro-EDM machine [see Fig. 3(a)]. A single *RC* pulse timing circuit with 1 KΩ and 100 pF respectively was used for this setup. The machining time was $\approx$5 min., which is 20×–30× less than that required for serial machining by a single electrode. Fig. 3(b) shows a honeycomb structure fabricated in 125 μm thick graphite sheet by using arrayed electrodes with hexagonal pattern shape. The pitch of hexagonal cells is 70 μm and wall thickness is 16 μm (a texture of lateral surface is from original graphite sample, not from machining). Since graphite has high thermal conductivity, such structures may be suitable for heat exchange applications.

Fig. 4 shows the variation of perforation diameters along a diagonal of the 20×20 array. The difference between the typical perforation diameter of 30–32 μm and the electrode diameter of 20 μm suggests that the lateral discharge gap is 5–6 μm. This is relatively large compared to the 2–3 μm gap that can be achieved by rotating single electrodes under comparable operating conditions. The enlargement of the hole is believed to be caused by debris from the discharge process, which includes particles removed from the workpiece and electrode as well as carbon residue from the dielectric oil. The debris are flushed away more effectively by rotating the electrode than by dithering it. The secondary discharges that occur between charged debris and workpiece are likely to enlarge the discharge gap. Fig. 4 shows that the holes in the center of the array are larger than those at the periphery.

A distribution of electrode wear across the array is shown in Fig. 5. The height of individual electrodes in the array was measured by detecting discharge to a sharp single-wire probe. It



(a)



(b)

Fig. 3. (a) Perforations of stainless steel using electrode array of Fig. 2. (b) Graphite honeycomb structure formed by array of hexagonal electrodes.

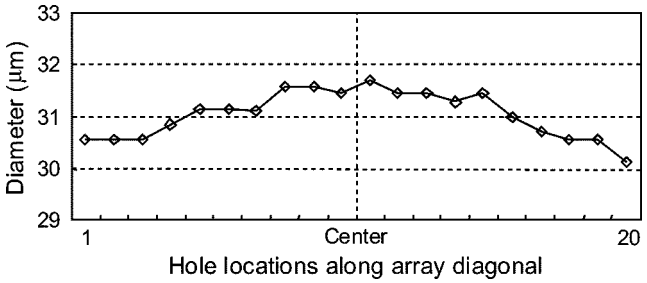


Fig. 4. Variation of perforation diameter in an array of Fig. 3(a). Diameter in the center of array is 1–1.5 μm wider than that at periphery.

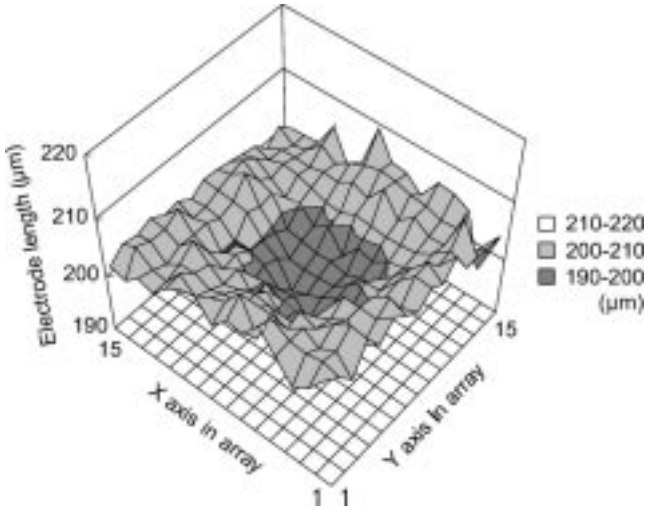


Fig. 5. Distribution of electrode wear in a 15 × 15 array of electrodes with 300 μm initial height, 30 μm diameter, and 90 μm pitch after uses in machining. Peak-valley difference in height is 16.8 μm.

is found that electrodes in the center are shorter than those at the periphery as similar tendency as the variation of hole diameter has. These both results are consistent with the hypothesis of debris removal.

The scaling limits for batch mode micro-EDM are related to both electrode fabrication and the micro-EDM process. The lower limit on electrode diameter is constrained by the plating process because of the height of the electrodes and the relatively small footprint. Void formation and adhesion problems can be encountered in fabricating very tall and narrow electrodes. Such electrodes may also delaminate from the substrate during the micro-EDM process.

Other problems observed in using high aspect ratio, densely packed electrode arrays include the following. The debris produced during the machining process gradually form lumps that tend to clog dense arrays or complex shapes. This problem is exacerbated in the context of lithographically fabricated electrode arrays because the debris are trapped between the workpiece and the electrode substrate. Trapped debris increase the likelihood of irregular arcing that disrupts regular discharge pulses. They may also deform the electrodes. Another concern is that arrays of narrow electrodes have an increased potential for damage from local pressure fluctuations (shock waves) that will be created in the dielectric oil as it is heated by discharge pulses.

III. Parallel Discharge

As the number of electrodes in an array increases, in order to obtain the highest machining rate it is necessary to sustain the discharge pulse frequency as well as to permit independence in the pulse timing at each electrode. For high-throughput machining with high precision, very small and well-controlled discharges should be generated by individual circuits connected to electrically isolated electrodes. This section evaluates the use of hybrid and monolithic implementations of partitioned arrays to achieve this goal.

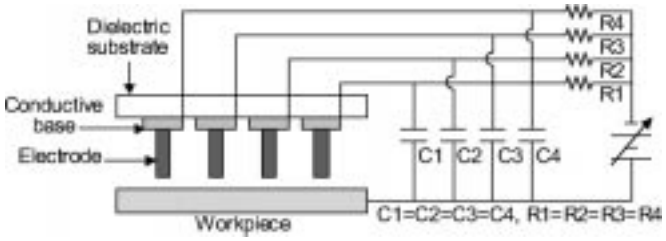


Fig. 6. Experimental setup for generating parallel discharge.

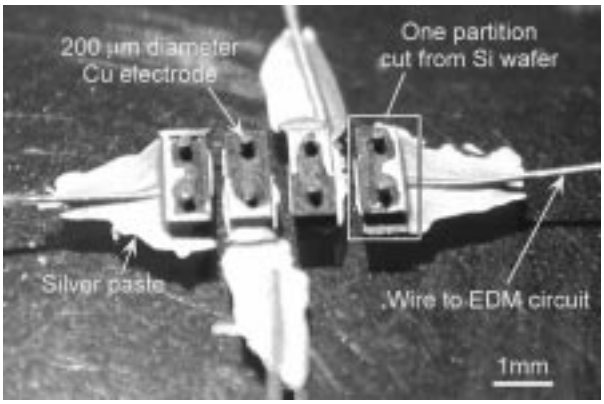


Fig. 7. Hybrid four-partition electrode array assembled on glass substrate.

A. Hybrid Partitioned Array

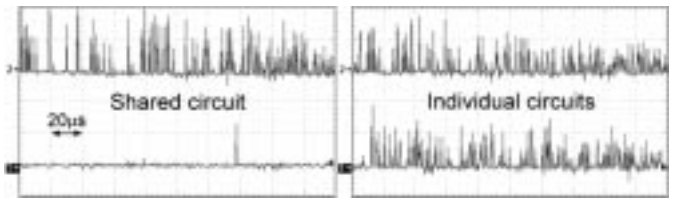
As a first step, to observe the effect of the parallel discharge mode, the electrode arrays were partitioned into four sections that were connected to separate *RC* pulse timing circuits as shown in Fig. 6. These partitions were assembled on a glass substrate and each had two 200 μm diameter electrodes connected to one circuit through the plating base (see Fig. 7). Each *RC* pair consists of a 1 KΩ resistance and 100 pF capacitance. The stainless steel workpiece served as a common anode, whereas the separated electrodes served as cathodes. The supply voltage was 80 V.

The effect of changing the partitioning of *RC* circuits was studied by its impact on the time required to machine a fixed depth. In order to sustain discharges with a fixed gap between the workpiece surface and the electrode tips, the electrodes must be advanced along the axis of approach as the workpiece and electrodes are eroded. If the electrodes are advanced with a rate that exceeds the erosion rate, they will come into contact with the workpiece, leading to a short circuit that can be detected by the apparatus. The equipment is designed to automatically retract the electrodes if this occurs. Consequently, the user-programmed value of the electrode advance rate should not significantly affect the actual machining rate as long as it exceeds the maximum machining rate achievable by the other operating conditions. This was experimentally verified by dithered operation using single and arrayed electrodes. A programmed value of 8 μm/s, which satisfied this lower bound, was used in the following experiments.

The electrodes of Fig. 7 were advanced up to 100 μm depth in stainless steel workpieces under three different configurations of the *RC* circuit. Table I shows a comparison of machining times required for the depth in each case: "1 circuit" denotes the connection of a single *RC* pair (with the values provided above)

TABLE I
MACHINING TIME FOR 100 μm DEPTH IN STAINLESS STEEL USING THE ELECTRODES OF Fig. 7 WITH 1, 2, AND 4 *RC* PAIRS

	1 circuit	2 circuits	4 circuits
Machining time (s)	1670	1117	814
Ratio to "1 circuit"	1	0.67	0.49



(a) (b)

Fig. 8. Timing diagram showing discharge pulses for two electrode partitions (a) sharing one *RC* circuit and (b) with separate *RC* circuits.

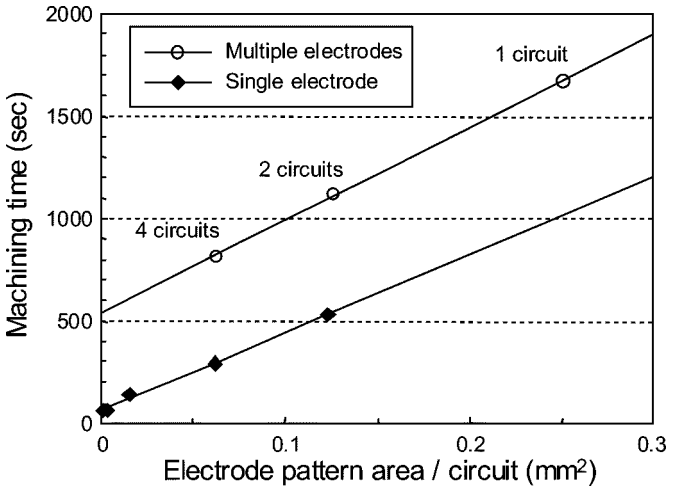


Fig. 9. Variation of machining time for 100 μm depth as electrode area per *RC* circuit is increased.

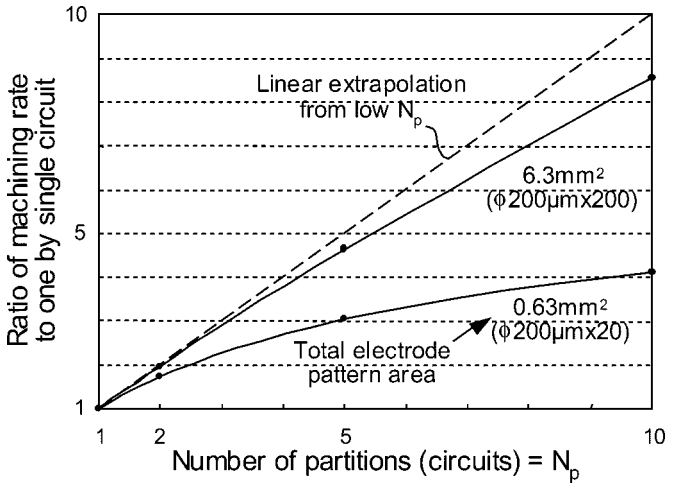


Fig. 10. Projected increase in machining rate as number of partitions is increased.

to all four electrode partitions in parallel; "2 circuits" denotes two *RC* pairs, each to two partitions in parallel; and "4 circuits" denotes the use of a separate *RC* pair for each partition. It was found that the machining time for the last was less than half that of the first.

Fig. 8 shows the timing diagram for the discharge pulses of two partitioned electrodes. The measurements were taken with current probes, which have a minimal loading on the discharge circuits. It is evident that when an *RC* pair is shared between two electrodes, only one electrode may fire at any given moment. The electrode which is closer to the workpiece surface will tend to dominate, effectively alternating the operation between the shared partitions. In contrast, when individual *RC* pairs are used for each partition, both can be firing all the time, resulting in a faster machining rate.

In Table I, the time savings are shown to be not in direct proportion to the number of *RC* pairs used. Since the RC pair determines the total power available through the electrode for a given supply voltage, it is worthwhile to evaluate the impact of electrode area served by one *RC* pair on the machining rate. Fig. 9 compares the machining times for 100 μm depth in a stainless steel workpiece using single electrodes of varying cross-sectional area served by a single *RC* pair with the data of Table I. Similar machining conditions were used in both cases. It is evident that for both single and arrayed electrodes, there is a linear dependence between the machining time and the electrode area served by an *RC* circuit pair. However, the latter results in a time-axis intercept of about 500 s, suggesting that for arrayed electrodes, there is a point of diminishing returns beyond which the machining rate may not be increased by adding *RC* pairs to the discharge circuit. This effect is further analyzed in Fig. 10. Two hypothetical cases are evaluated in this figure, using the trend shown for arrayed electrodes in Fig. 9, and assuming that it will be sustained as the net electrode area is increased. In one case, the array consists of 200 electrodes of 200 μm diameter, whereas in the other case only 20 electrodes are present, resulting in $10\times$ smaller area. The plots show the machining rate (normalized to that achieved with a single *RC* pair) increases with the number on *RC* partitions more effectively for large areas. The result suggests a path of investigation for further increases in throughput.

B. Monolithic Partitioned Array

To increase both of spatial density of partitions and temporal density, the use of lithographically patterned thin film interconnect underneath LIGA-fabricated electrode array in conjunction with multiple pulse generation circuits is explored (see Fig. 11). Such electrodes can be fabricated by using a two-mask sequence similar to sacrificial LIGA process [15]. The interconnect pattern is formed on 0.5 μm thick oxide on a Si substrate by etching an $\approx$1 μm thick Ti/Cu electroplating base. Fig. 12 shows Cu electrodes of 10 μm wall thickness and 300 μm height intended for cutting gears. The connection to pulse timing circuits is made by wire bonding to contact pads along the array perimeter. Using these electrodes, 70 μm thick WC-Co gear clusters were successfully produced (see Fig. 13). The upper scanning electron micrograph (SEM) image in Fig. 13 shows a sample of 36 gears that were cut in parallel in 15 min using four circuits. The lower image shows gears that took about 50 min. under similar conditions because of the larger surface area. Even so, this represents

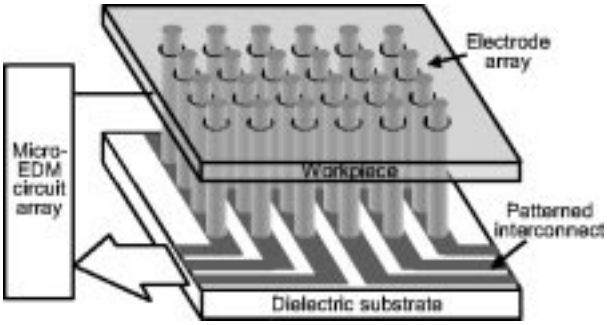


Fig. 11. Conceptual diagram of accelerated batch mode micro-EDM by means of generating parallel discharges with partitioned electrode arrays that are connected to individual micro-EDM circuit.

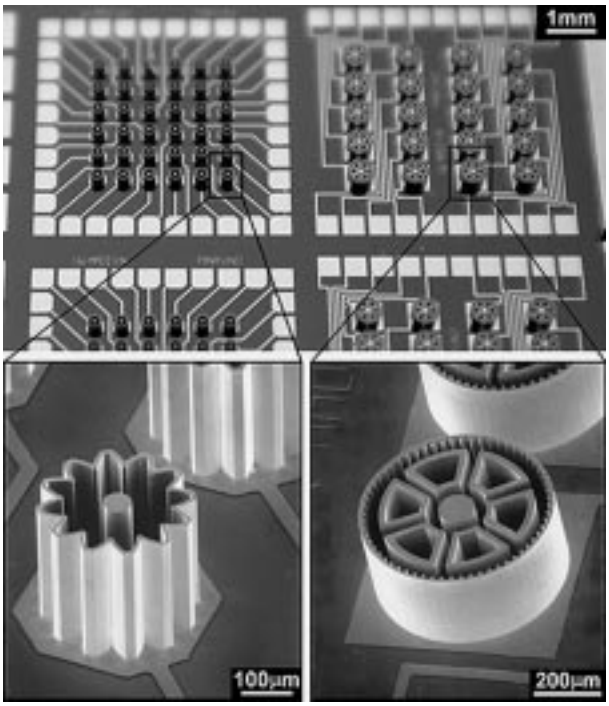
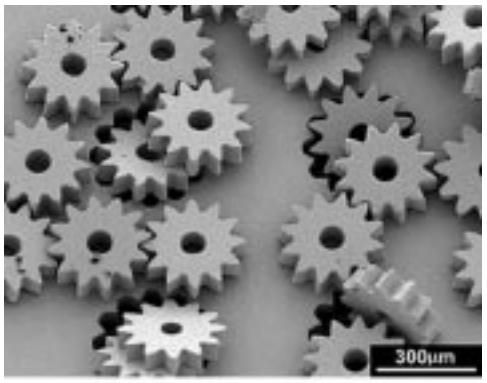


Fig. 12. Cu electrode arrays with patterned interconnect fabricated by using LIGA technique with two-mask alignment sequence.

$>100\times$ improvement in throughput compared to single electrodes.

IV. Circuit Optimization

Although the use of multiple *RC* pairs increased throughput, it was found to have a deleterious effect on the roughness of the machined surface when lithographically fabricated electrode arrays with patterned interconnect were used. Fig. 14 compares two surfaces of stainless steel machined by an array of eight electrodes with 100 μm $\times$ 100 μm square cross section with individual leads: one using eight *RC* pairs and the other with a single *RC* pair. The same values for *RC* were used for every pair. A single power supply of 80 V was used in both cases. It is clear that the former is substantially rougher. Fig. 14 also shows the trace of a single current pulse triggered by the discharge measured at the workpiece where it connects to the external lead. The increase in pulse amplitude and duration with the number of *RC* pairs used in this scheme increases the net energy per discharge to a level that compromises surface quality, and consequently, precision.



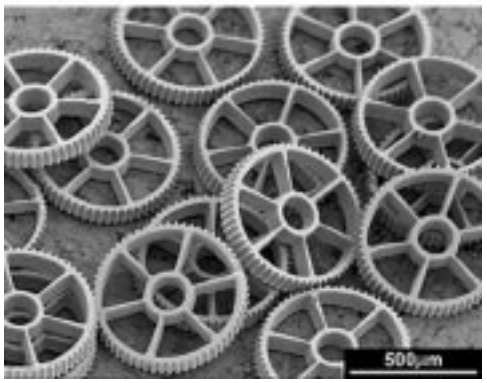


Fig. 13. WC-Co super hard alloy gears cut from a 70-μm-thick workpiece using electrode arrays of Fig. 12.

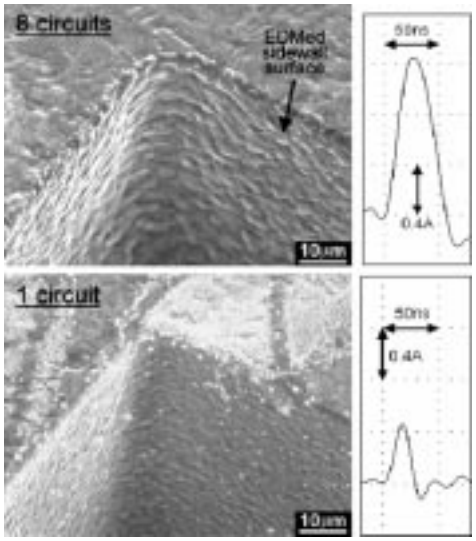


Fig. 14. Comparison of the roughness of machined surface and associated discharge pulse currents when using eight circuits (upper) and one circuit (lower).

A. Impact of Parasitic Capacitance

The increase in pulse discharge energy can be largely attributed to the parasitic capacitance associated with the thin-film patterned interconnect. As shown in Fig. 15(a), C_{p1a}, the capacitance between this metal layer and the Si substrate exists essentially in parallel with the external capacitance C_e,

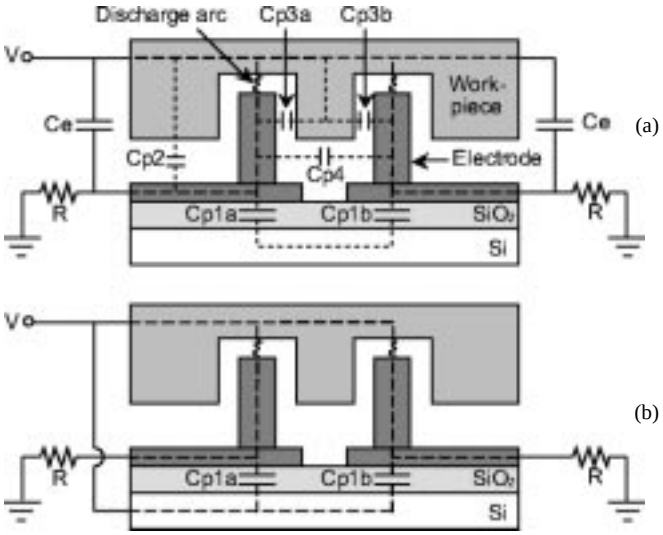


Fig. 15. (a) Conventional pulse generation circuit showing parasitic capacitances. (b) New circuit that uses parasitic capacitances instead of C_e.

which, together with the external resistance R, is intended to control the pulse timing. Other parasitic components that occur between the workpiece and various facets of the electrode are typically 10^2–10^4 smaller than C_{p1a}. Furthermore, the Si substrate, which is electrically floating in the conventional micro-EDM scheme, connects all the C_{p1} elements together, and provides a path for cross-talk between the electrodes that can affect pulse timing. For example, in Fig. 15(a), a discharge arc may raise the potential of one electrode, but capacitive coupling through the series combination of C_{p1a} and C_{p1b} may also elevate the voltage of the neighboring electrode, temporarily suppressing a discharge there. In the eight electrode experiment described above, the measured value of this series combination is 95 pF, which means that a single C_{p1a} is 190 pF because every segmented interconnect and contact pad in the setup has the same area. This is in excellent agreement with the theoretical estimate for the 3 mm^2 pad area for each electrode.

B. Simulation Analysis

The impact of C_{p1} was examined by circuit simulation using SPICE™ [16]. To model a discharge gap, the following simplified steps in typical electrical breakdown phenomena were considered: 1) a breakdown is triggered when the voltage between an electrode and the workpiece exceeds a threshold; 2) once it is triggered, the voltage instantly drops to a constant arc voltage sustained during the discharge; 3) the arc ends when a current supplied from a capacitor diminishes. This behavior can be modeled by a thyristor or silicon controlled rectifier (SCR) [17]. The thyristor is used essentially as a two-terminal device that triggers at a threshold voltage. Since the steady-state operating voltage of the thyristor is typically small, a series connected Zener diode is used to match the steady-state arc voltage. The breakdown of the thyristor is then set at the difference between the overall breakdown voltage desired and the Zener breakdown voltage. A resistor and inductor are also connected in series to the thyristor with the Zener diode to shape the simulated current pulse to the measured transient current during the discharge. Fig. 16 shows an equivalent circuit for the four-partition arrangement of Fig. 15(a). It is used to analyze pulse frequency as well as pulse waveform.

In Fig. 16, the elements R_p and L_p can be interpreted as the parasitic resistance and inductance, respectively, in a discharge circuit loop that consists of a capacitor and a discharge gap connected in parallel. Although their direct measurement is difficult, they can be estimated from a single-electrode discharge circuit by using measured values of peak current and pulse duration τ_p. This model that replaces a discharge gap with a constant dc voltage source E_g to express the constant arc voltage is good to see a transient behavior of a single pulse (see Fig. 17). The following differential equation can be derived from the circuit [18]:

$$L_pC_e\frac{d^2i}{d^2t}+\left(R_pC_e+\frac{L_p}{R}\right)\frac{di}{dt}+\left(1+\frac{R_p}{R}\right)i=\frac{E-E_g}{R} \tag{1}$$

where i is a current that flows in the discharge circuit loop, R is a resistance in a charge circuit loop, C_e is a capacitance and E is a dc voltage source. A general solution of (1) is

$$i=e^{-Dt}(c_1\sin\omega t+c_2\cos\omega t)+\frac{E-E_g}{R+R_p} \tag{2}$$

where c_1 and $c_2=$ constant, $D=(1/2)((R_p/L_p)+(1/RC_e))$ and $\omega=\sqrt{(1/L_pC_e)(1+(R_p/R))-D^2}$. With the initial conditions of $i=0$ and voltage of capacitance $C_e=E$ when $t=0$, c_1 and c_2 can be fixed to $c_1=((E-E_g)/\omega)((1/L_p)-(D/(R+R_p))$ and $c_2=-((E-E_g)/(R+R_p))$, respectively, and (2) is transformed to

$$i(t)=\frac{E-E_g}{R+R_p}\cdot \left[e^{-Dt}\left(\frac{R+R_p-L_pD}{\omega L_p}\sin\omega t-\cos\omega t\right)+1\right]. \tag{3}$$

The time at which the current peak can be found by setting $di/dt=0$. This value is $T=(1/\omega)\arctan(c_1\omega-c_2D)/(c_1D+c_2\omega)$. The peak current is found by evaluating (3) at this time. Typical measured values of peak current and pulse duration were 0.45 A and 40 ns respectively when a single electrode was used (and others in the array were left floating). These values were similar to those in the experiment of Fig. 7, because the parasitic capacitance between electrode partitions was negligible. In particular, the measured value was 100–1000× smaller than the external C of 100 pF in Fig. 7. Therefore

$$i(R_p,L_p)|_{t=T}=0.45\ \text{amp}. \tag{4}$$

The pulse duration, τ_p is determined by the zero-crossing of the current waveform. Thus,

$$i(R_p,L_p)|_{t=\tau_p=40\ \text{ns}}=0\ \text{amp}. \tag{5}$$

In the experiments, R, C_e and E are 1 KΩ, 100 pF and 80 V respectively, and E_g was measured as ≈20 V. Using (4) and (5) with the values, a pair of R_p and L_p was obtained numerically.

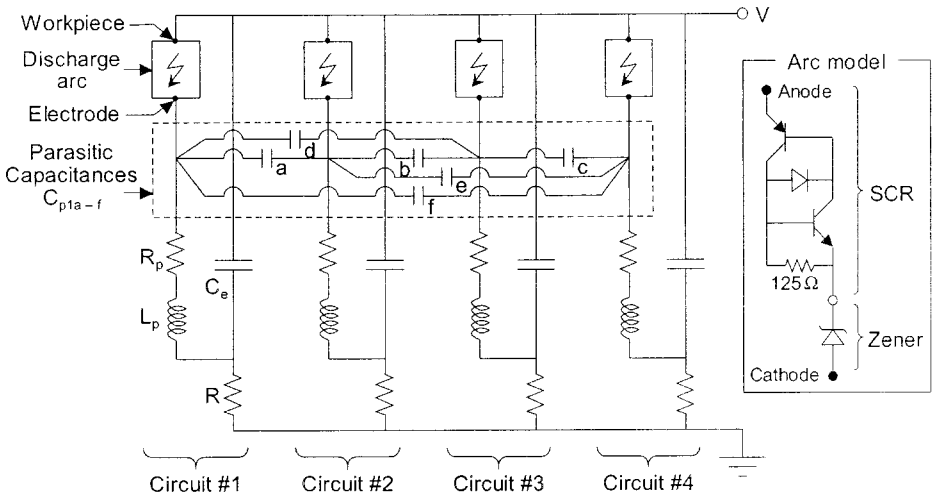


Fig. 16. Four-partition circuit model for SPICE simulation that uses thyristor (SCR) with Zener diode for modeling discharge gap. Each circuit consists of the same element with the same value. L_p, R_p, R, C_e, C_{p1}, and V are 1.3 μH, 26 Ω, 1 KΩ, 100 pF, 95 pF, and 80 V, respectively. Breakdown voltages of thyristor and Zener diode are 50 V and 20 V, respectively.

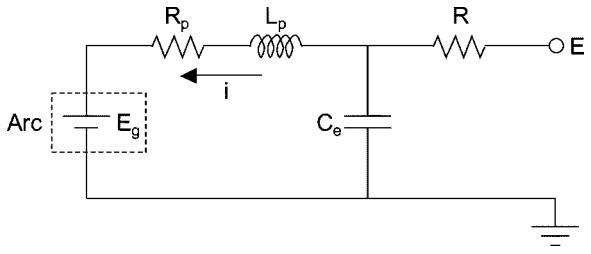


Fig. 17. Single charge/discharge circuit model that is used to estimate R_p and L_p by calculation with measured pulse duration and peak value of current i. E_g represents constant arc voltage.

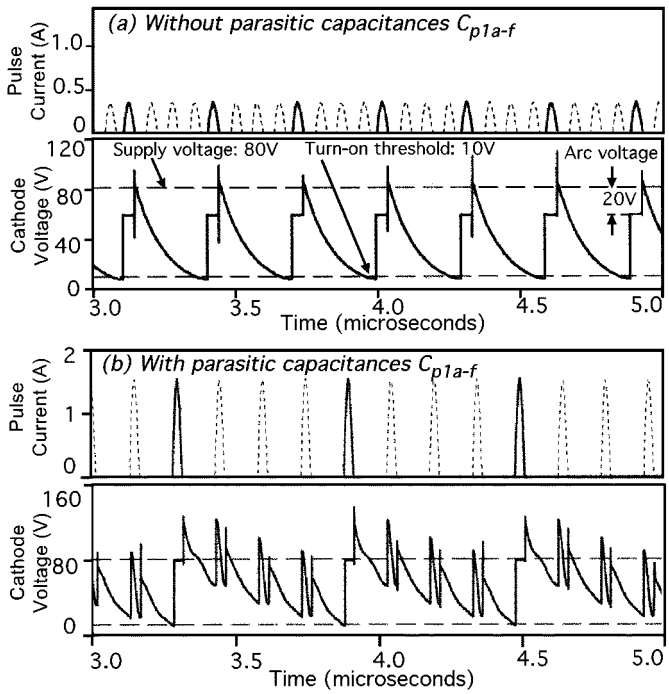


Fig. 18. SPICE simulation results for 4-partiton circuits (A) without and (B) with parasitic capacitances C_{p1a-f} in Fig. 16. In each result, pulse current (upper) and voltage (lower) at one electrode are plotted by thick line. Dashed thin lines in each of current diagrams show currents at the other three electrodes. Different initial timing is used for each partition.

Although two solutions were obtained, only one (26 Ω, 1.3 μH) provides a fit to the measured waveform.

The role of the parasitic capacitances C_{p1} in shaping the pulse waveform is shown by the simulation results in Fig. 18. Fig. 18(a) shows the waveform obtained when C_{p1} is negligibly small, such as the hybrid arrangement of Fig. 7, whereas Fig. 18(b) shows the case for the monolithic implementation illustrated in Fig. 11. In both Fig. 18(a) and (b), the upper diagram shows the current that flows through the thyristor as an arc current represented by a solid line (with currents in other three thyristors are seen as dashed lines), while the lower diagram is the voltage at its cathode. Since the breakdown voltage was estimated at 70 V and the steady-state arc voltage was measured at 20 V, in the arc model, the Zener breakdown was set at 20 V and the thyristor breakdown was set at 50 V. In the absence of parasitic capacitance the pulses are clean and there is no evidence of cross-talk between electrodes. The simulated peak current and duration of a pulse are 395 mA and 42 ns respectively, which agree well with typical measured values described above. In the presence of C_{p1}, however, the cathode voltage of the observed thyristor is affected by pulses at other thyristors, which results less frequent firing and predicts a lower machining rate. The pulse frequency at each electrode in Fig. 18(b) is 1.79 MHz, which is nearly a half of 3.37 MHz achieved in Fig. 18(a). In addition, the peak current is increased almost tripled. This means that the volume removed by each pulse is increased, which makes machined surfaces rougher. These results explain experimental results very well.

C. New Circuit Scheme

Despite the adverse effects discussed above, the presence of C_{p1} offers an opportunity to eliminate C_e and simplify the discharge circuit for the monolithic implementation. The revised circuit is shown in Fig. 15(b). The primary changes are that the

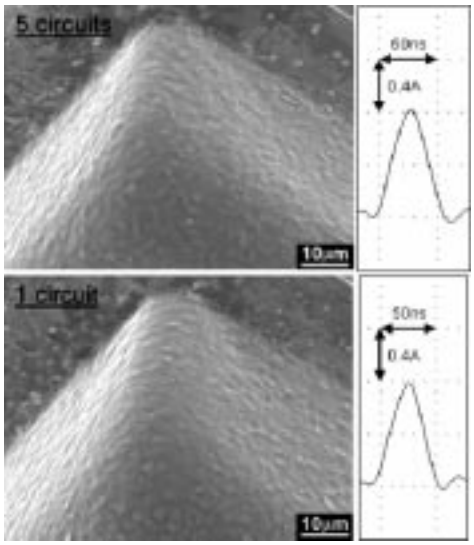


Fig. 19. Comparison of roughness of machined surfaces and associated discharge pulse currents when using five circuits (upper) and one circuit (lower) in setup of Fig. 15(b).

TABLE II
MEASURED WIDTHS OF HOLES MACHINED BY ONE 100 μm $\times$ 100 μm ELECTRODE (IN AN ARRAY OF 5) USING VARIOUS CIRCUITS

Fig. 15(a) w/ 5 circuits	Fig. 15(a) w/ 1 circuit	Fig. 15(b) w/ 5 circuits	Fig. 15(b) w/ 1 circuit
109 μm	106 μm	105 μm	105 μm

external capacitors have been dropped and the electrode substrate is tied to the positive supply terminal. This configuration reduces cross-talk due to C_{p1} between electrodes.

The performance of new circuit was experimentally evaluated using an array of five Cu electrodes with 100 μm $\times$ 100 μm square cross section. In a stainless steel workpiece, using an 80 V supply, 50 μm machined depth was achieved in 38 s at an average rate of 1.32 μm/s, whereas 100 μm depth was achieved in 86 s, at an average rate of 1.16 μm/s. The machining rates were the same whether a single electrode was connected to a single external resistor/circuit or all five electrodes were connected to five separate resistors. (In this experiment, only one electrode was permitted to touch the workpiece.) As shown in Fig. 19, the smoothness of the machined surfaces in both the single electrode/single circuit case and the five electrode/five circuit case was visually comparable to the best smoothness achieved by the conventional pulse generator. The current pulses shown in Fig. 19 were of intermediate amplitude compared to those in Fig. 14.

A measure of precision in micro-EDM is the tolerance between an electrode and a hole machined by it. In Table II, this parameter is compared for four different cases. It is notable that the conventional circuit configuration in which all electrodes are connected in parallel to a single *RC* pair, provides the most modest tolerance, with a 9 μm mismatch between the electrode dimensions and the hole, whereas the configuration which uses the built-in parasitic capacitance provides the best performance with a 5 μm mismatch.

V. CONCLUSION

The batch mode micro-EDM that uses LIGA-fabricated electrode arrays has been investigated. This effort has explored scaling issues in the fabrication and use of the electrodes. Arrays of up to 400 electrode elements with 20 μm diameter and 300 μm height were fabricated from plated Cu. The fabricated arrays were used to machine stainless steel and graphite samples. The variation of hole diameter and electrode wear across the array was studied. The impact of partitioning the array and using separate discharge timing circuits for each partition was also examined. The results obtained clearly demonstrate that using arrayed electrodes with separate pulse control circuits (*RC* pairs) for each array partition can vastly increase the machining rate. The rate increased linearly with the number of *RC* pairs used. However, scaling predictions based on measured results suggest that the benefits to machining rate diminish as the electrode area per *RC* pair decreases. The experimental results were extrapolated to project the potential improvement in machining rate afforded by increasing the number of partitions. The results suggest that the machining rate can be increased by a factor of 4–8 if 10 partitions are used in electrodes of 0.6–6 mm^2 area.

Electrode arrays with lithographically fabricated interconnect were explored for the purpose of increasing spatial and temporal density of discharge pulses. Examination of machined surfaces and the pulse waveforms revealed that as the number of *RC* pairs increases, the pulse energy and the surface roughness both increase. These may be attributed to the role of the parasitic capacitance between the patterned interconnect and the Si substrate, which increases the total effective capacitance and also permits crosstalk between electrodes. SPICE simulation for the discharge circuit agreed with the presumption.

A new circuit configuration that uses the on-chip parasitic capacitance of 190 pF per electrode instead of external capacitors was demonstrated. This arrangement is highly amenable to large size arrays because all the pulse control circuit elements can be integrated. In addition, it offers accelerated machining rates, and tighter tolerance than conventional schemes. Stainless steel workpieces of 100 μm thickness were machined by 100 μm $\times$ 100 μm square cross section electrodes in only 86 s using an 80-V power supply. The machined holes were only 5 μm wider than the electrodes, while the surfaces were smooth and did not exhibit any degradation with increased electrode or circuit multiplicity. These results demonstrate that highly integrated electrodes and circuits will be practical to use for high-yield and high throughput production. Using electrode arrays with four circuits, batch production of 36 WC-Co gears with 300 μm outside diameter and 70 μm thickness in 15 min. was demonstrated.

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