Batch-Fabricated High-Power RF Microrelays With Direct On-PCB Packages

Fatih M. Ozkeskin, Member, IEEE, Sangjo Choi, Student Member, IEEE, Kamal Sarabandi, Fellow, IEEE, and Yogesh B. Gianchandani, Fellow, IEEE

Abstract—This paper describes a process for batch manufacturing, assembly, and packaging of metal alloy microrelays directly on printed circuit board (PCB) substrates for high-power radio frequency (RF) applications. Stainless steel cantilevers with Pt-Rh tips are mounted on Rogers 4003 PCB substrates to demonstrate the approach. A multilayer PCB design allows for the use of subsurface metal layers to transmit the RF signal into and out of the sealed encapsulation. The electrostatically actuated microrelays with 8.4-mm² footprints have 78-V pull-in voltage and 1.1-Ω ON-state resistance. Packaged microrelays exhibit down-state insertion loss and up-state isolation better than −0.25 and −15 dB, respectively, for frequencies up to 5 GHz. Packaged devices remain functional up to 20-W RF power under hot switching conditions. The high power lifetime of the microrelays is 10,913 cycles for 1-W incident RF power in 1-s pulses and 84,144 cycles for 10-W incident RF power in 0.1-s pulses. The impact of device encapsulation and multilayer PCB substrate on device performance is addressed.

Index Terms—Batch fabrication, high power, package, printed circuit board (PCB), radio frequency (RF) microrelay.

I. INTRODUCTION

RECENT advances in radio frequency (RF) microrelays and micromachined switches have shown the possibility of very low insertion loss, high isolation, and near-zero power consumption in comparison with conventional technologies such as p-i-n diodes and FET switches [1]–[7]. Although many types of microrelays have been reported, less attention has been focused on integration with various other functional components, which is necessary to implement complete systems, and many challenges remain [8]–[11]. The RF micromechanical switches that are fabricated on Si, GaAs, quartz, and alumina [12]–[14] require attachment to the printed circuit boards (PCBs) where other components are located.

PCBs are commonly used for RF applications, including phase shifters and antennas [19]–[21]. PCBs offer several advantages such as a wide range of substrate thickness and dielectric constants, and low loss tangent which is highly desired in reducing losses and mismatches. These properties make PCB a good substrate candidate for direct microrelay fabrication and integration to other RF front-end system components. Wire bonding is one of the most widely used interconnection techniques for IC and MEMS packaging; however, at high frequencies, bonding wires are known to introduce parasitic effects and impedance mismatching [15], [16]. These effects and mismatch exhibit undesired signal losses on the RF components which deteriorate device performance. Other interconnection techniques such as flip chip are used to achieve system level integration [17], [18]; however, these are still susceptible to RF performance degradation due to the aforementioned effects. Past efforts on RF MEMS switch fabrication on PCB substrates [22]–[25] focused on applications limited to very low power and did not consider device packaging, which is essential for environmental protection and increasing device reliability.

This paper describes a process to batch fabricate and assemble electrostatically actuated microrelays with stainless steel cantilevers and Pt-Rh tips on PCB substrates for high-power RF applications. In addition, a direct on-PCB device encapsulation process without notable RF performance compromise is introduced. Section II describes the microrelay design. Section III provides details for the batch fabrication and assembly of the device and packaging. Section IV presents the experimental evaluation and results. These include the characterization of electrical performance in dc, small-signal and high-power RF, device lifetime, and package testing. Section V provides the discussion and conclusions.

II. DESIGN

The packaged batch microrelays are designed in 4 × 1 array structures (Fig. 1). Individual platinum-rhodium (Pt-Rh) contact bridges, detailed later in this section, are located on a Parylene-coated 50-μm-thick stainless steel (SS304) cantilever frame which carries four cantilevers. Four gold posts (1-mm height and 500-μm diameter each) align and firmly hold the cantilever frame over cantilever frame support traces on a multilayer PCB.

The individual microrelay, which is singulated from 4 × 1 array structures, is shown in Fig. 2(a). The device footprint,
defined by the footprint of the cantilever, is 8.4 mm$^2$. The cantilever has three distinct regions which are shown in Fig. 3(a). The first region includes a slot (1 mm × 250 μm) located on the anchor region which facilitates the attachment of the cantilever on the PCB. The second region constitutes a recess of 2.23-mm$^2$ area and 4-μm depth in the middle of the cantilever for the actuation gap. The third region has a recess of 28-μm depth at the distal end for the placement of the Pt-Rh contact bridge. Parylene is used to electrically isolate the cantilever from the RF path because of its excellent insulation properties [26]. A Parylene coating of 3-μm thickness enveloping the cantilever allows for a dielectric breakdown voltage of 820 V. A Parylene-free opening is located on the cantilever for the electrical connection.

Pt-Rh was chosen as the contact metal due to its high RF power handling capability [27]. A 25-μm-thick rectangular Pt-Rh contact bridge is located inside the 28-μm-deep recess below the tip of the cantilever for the electrical contact. The Parylene coating on the cantilever isolates the contact bridge from the dc path. The contact bridge has a through hole of 300-μm diameter in the center to permit epoxy application during the assembly. Four contact dimples of 40-μm diameter are defined on the contact bridge to electrically short the open ends of the transmission line underneath it. The height of the dimples is designed to be 10 μm to reduce the capacitance between the transmission line and the contact bridge, hence increasing the isolation in the up-state. The bottom of the contact bridge levels with the cantilever and allows for a 3-μm contact gap as per the Parylene thickness [Fig. 2(b)].

The cantilever–contact bridge assembly is positioned on a multilayer PCB, orthogonal to the transmission line. The PCB
uses a 600-μm-thick Rogers 4003 substrate which accommodates a reduced loss at microwave frequencies. The substrate is composed of three layers (each 200 μm thick) to accommodate multilayer traces. The Cu traces (70 μm thick) provide the bias electrodes, the transmission line segments, and vias. A 4-μm-thick Ni is used as an adhesion layer on the Cu base, and a 0.15-μm-thick outer gold layer provides high-conductivity electrical contacts. The PCB layout can be divided into four regions. The first region includes two transmission line segments with 50-Ω characteristic impedance and provides input and output paths for the RF signal. At the end of open lines, the terminals fork out to accommodate regions for contact dimples (150 μm × 150 μm each). The transmission line segments are located on two layers: the top layer and the layer-2 which is at 200-μm depth from the substrate surface [Fig. 3(b)]. This design approach is used to enable the location of a package lid on top of the device which would directly sit on the PCB substrate. Blind vias of 150-μm diameter connect the top layer with the layer-2 transmission line.

The second region includes the dc ground electrode, which is designed on the top metal layer in the PCB. Blind vias of 250-μm diameter transfer the dc signal onto the layer-2, whereas through vias of 250-μm diameter shunt the dc ground to the RF ground plane at the bottom layer.

The third region includes the pull-in electrode which is used to electrostatically actuate the cantilever. It is also located on both the top layer and the layer-2 to allow for the placement of the package lid. The fourth region includes an L-shaped electrode which allows for the placement of a dc-blocking capacitor and also acts as a shield to minimize RF signal coupling from the transmission line. In this design, the multilayer structure of the transmission line is one of the main reasons for increased RF signal reflection and return loss. The current transmission line design is obtained through an iterative optimization study to enhance RF switching performance. The simulations are described toward the end of this section.

A 1-mm-tall package lid (Stratedge Corp.) with 0.5-mm wall thickness is used to encapsulate the device. Liquid crystal polymer (LCP)-based Vectra A130 is used because its low loss tangent of 0.002 and very high electrical resistivity of 10^{15} Ω·cm minimize RF coupling [28]. Nitrogen is chosen as the encapsulated gas. The open edges of the lid contain an epoxy preform with a wavy surface profile, allowing the gas intake prior to curing, after which it levels with the substrate and seals the device. Fig. 3(c) shows the dimensions of the package lid.

ANSYS Workbench finite-element analysis (FEA) was used to perform the electrostatic modeling for the RF microrelay.
Fig. 3. (a) Dimensions for the cantilever and the contact bridge. Three distinct regions are shown on the cantilever. First region is for anchoring the cantilever on the PCB and has the anchor slot to apply epoxy. Second region has a 4-μm shallow recess to define the 7-μm actuation gap with 3-μm Parylene thickness. Third region has a 28-μm deep recess for the placement of the contact bridge. The contact bridge has four contact dimples with 40-μm diameter and 10-μm height each. (b) DC and RF lines shown in separation from the PCB substrate. All the vias are plated with Cu/Ni/Au traces. Through vias connect the top layer to the bottom layer where RF ground is defined whereas blind vias connect the top layer to the layer-2. (c) Package lid dimensions. Wavy epoxy preform allows gas intake prior to thermal curing.

The displacement and the stress distribution are shown in Fig. 4(a) and (b), respectively. The model consisted only of the microrelay and partial transmission line. All other components were neglected. The “fixed geometry” boundary condition was applied around the anchor slot on the cantilever. The Parylene coating was modeled as a 3-μm-thick solid body enveloping the cantilever. The “bonded contact” boundary conditions were used between the cantilever and the contact bridge, and the transmission line. The simulated pull-in voltage for 3-μm tip displacement was 72 V. The displacement above the ground electrode was less than 2 μm. This suggested that inadvertent contact at this location would be avoided. The stiffness of the microrelay, including the Parylene-coated cantilever and the contact bridge, was 110 N/m. Fig. 4(b) shows the same stress distribution over four contact dimples. The contact force per contact region was 0.55 mN (with 2.2 mN evenly distributed over four contact regions) for an increased actuation voltage of 100 V. The simulated turn-on time from dynamic analysis was 9 ms for 72-V actuation voltage.

The multilayer transmission line was optimized to reduce the fringing and the RF coupling effects. The geometric optimization assumed only the through-line for the signal: All the traces on the PCB, as well as the package, were included in the model; however, the cantilever and the contact bridge were excluded. Iterative RF simulations were performed in high-frequency structure simulator (HFSS), and return loss ($S_{11}$) was evaluated. A total of five transmission line configurations were studied [Fig. 5(a)]. All the lines were matched to 50-Ω characteristic impedance. Geometric considerations for LC tuning included mainly design limitations imposed by the PCB manufacturing process. The two main limitations were the minimum via diameter of 125 μm and the minimum layer thickness of 100 μm which defined the minimum via height. Table I summarizes via dimensions and configurations. Configuration-1 used a single-point connection between the top layer and the layer-2 through a single via with 400-μm diameter. The length of the line segment on the layer-2 was 4.2 mm to match the line segment on the top layer. Configuration-2 employed
Fig. 5. (a) Geometric configurations for the through transmission lines used in RF optimization study. (b) Full-wave HFSS simulation results showing $S_{11}$ for five configurations. The cantilever and the contact bridge were discarded in simulations. Configuration-5 provides the lowest return loss with nearly $-28$ dB at 10 GHz.

III. Fabrication and Assembly

Microelectrodischarge machining (μEDM) is a lithography-compatible electrothermal machining technique applicable to any conductor and semiconductor material. Feature sizes as small as 5 μm can be achieved using μEDM both in serial mode (using a cylindrical wire-tip electrode) and in batch mode (using a lithographically patterned and electroplated chip as a “cookie cutter”) [29].

The contact bridges were serially fabricated using μEDM in 80:20 Pt-Rh (Alfa Aesar Corp., 99.99% purity). The thickness of the stock metal foils was 25 μm. Initially, a through hole of 300-μm diameter was created in the center of the structure. This was followed by 10-μm recesses to define the height of the contact dimples with 40-μm diameter. Since the height of the dimples was not further modified, the surface roughness of the contact dimples was the same as the surface roughness of the virgin stock foil. The roughness was measured using Zygo NewView 5000 interferometer. Average roughness $R_{a}$ was approximately 26 nm.

The cantilever frame was photochemically etched from 50-μm-thick SS304 foil (Kemac Technology Inc., CA). Perforations of 500-μm diameter were located on the four corners of the frame for batch assembly onto the PCB. In addition, slots of 250-μm diameter and 1-mm width were located on the individual cantilevers for the assembly over the PCB.

The etched cantilever frames were then serially machined using μEDM to create recesses of 4 and 28 μm in the middle and at the tip of the cantilevers, respectively. The lowest available discharge energy of 18 nJ was used to minimize the residual stress and achieve flat cantilevers. After machining, the cantilever frames were cleaned in an ultrasonic tank with kerosene-based EDM oil, acetone, IPA, and deionized water. Following this, the cantilever frames were coated with 3-μm-thick C-type Parylene. All the individual components, including cantilever frames, package lids, and the PCB (Circuit Express, AZ), are shown in Fig. 6(a).

For the device assembly, the contact bridges were placed inside the recessed regions at the tip of the cantilevers and fixed by applying high-temperature epoxy (Cotronics Duralco 4703, 645 K maximum temperature) around the through hole [Fig. 6(b)].

To batch assemble the cantilever frame and the PCB, alignment posts were fabricated using μEDM from 500-μm diameter gold wire and tightly fitted into the vias on the PCB. The cantilever frame with mounted contact bridges was assembled over the posts [Fig. 6(c)], and epoxy was applied around the posts to fix the frame. In addition, epoxy was applied on the cantilever frame support traces for added mechanical strength during the device singulation process. The individual cantilevers were fixed onto the PCB by applying electrically conductive epoxy (Creative Materials, volume resistivity: 300 $\mu\Omega \cdot$ cm) around the slots. Cutting lines for the device singulation are shown in the inset in Fig. 6(c).

For device packaging, Vectra A130 lids were aligned onto the singulated devices and fitted using a mini spring clamp with 4.5-N pressing force. The devices were then placed in a vacuum oven. The pressure inside the oven was first reduced to approximately 5 Pa at room temperature. Following this, the
vacuum was choked, and the nitrogen was reintroduced up to atmospheric pressure. The oven temperature was then adjusted to 160 °C, and the package lids were cured for 1 h. Following the curing, the spring clamps were removed. Fig. 6(d) shows singulated and packaged devices.

A total of five devices were fabricated and assembled. The distribution of those devices is as follows: two devices for dc ON-state resistance characterization, hysteresis study, and small-signal characterization with and without the package; one device for high-power testing; and two devices for the lifetime characterization at 1- and 10-W RF powers.

### IV. Experimental Evaluation

Electrical testing of the batch-fabricated microrelay included dc and RF performance evaluation at both small-signal and high-power levels. The testing circuitry and the actuation concept are shown in Fig. 7(a). The small-signal RF input and output were provided from a network analyzer through SMA-type coaxial connectors. The small-signal power was 32 μW. For electrostatic actuation, an actuation voltage \( V_G \) was applied on the pull-in electrode. A dc ground voltage was applied to the ground electrode through a 20-kΩ resistor. For a four-probe contact resistance characterization, a line current was monitored in the down-state and in the up-state of the relay, with the contact bridge resistance, and other parasitics. Fig. 8(b) shows the RF performance for the unpackaged and packaged devices, respectively. For the unpackaged microrelay, the down-state insertion loss was better than −0.2 and −0.65 dB for up to 5 and 10 GHz, respectively [Fig. 9(a)]. In the up-state, the isolation was better than −18 and −12 dB for up to 5 and 10 GHz, respectively [Fig. 9(b)]. For the packaged microrelay, the down-state insertion loss was better than −0.25 dB at 5 GHz and about −0.7 dB at 10 GHz [Fig. 10(a)]. The up-state isolation was better than −15 dB at 5 GHz and −12 dB at 10 GHz [Fig. 10(b)]. For both unpackaged and packaged devices, experimental data overall agreed well with the simulations.

The setup for the high-power handling test is shown in Fig. 7(b). A discrete power sweep was performed through 12 gain levels from 1 up to 30 W of RF power at 3 GHz, which was the testing setup limit (Amplifier Research 30W1000B). Only \( S_{21} \) was monitored in the down-state and in the up-state because of the nonreciprocal configuration of the power amplifier. Tests were performed on packaged microrelays. Hot switching conditions were used with continuous RF power and 1-s ON-state times of the switch, repeated every 2 s. The actuation voltage was set to 120 V to provide a low ON-state insertion loss. Fig. 11 shows the experimental results. In the down-state, the insertion loss was better than −0.2 dB for up to 5 W of RF power. Past this point, insertion loss deteriorated progressively down to −0.9 dB, and the microrelay failed due to contact microwelding at 20 W. The up-state isolation was approximately constant at −21 dB over the power sweep range. The maximum variation in isolation was below 1 dB; self-actuation was not observed.

The output power can be estimated using the input power and \( S \)-parameters following the relationship [30]

\[
P_{\text{OUT}}(W) = 10 \frac{P_{\text{in}}(\text{dBm})}{10} \times 0.001 \\
P_{\text{in}}(\text{W}) = 10 \log_{10} \left( \frac{P_{\text{out}}}{10} \right) \\
P_{\text{dBm}} = 10 \log_{10} \left( \frac{P_{\text{out}}}{10} \right) \\
+ 2 \times S_{21}(\text{dB}). \tag{1}
\]

### TABLE I

**VIA DIMENSIONS AND ARRANGEMENTS FOR FIVE CONFIGURATIONS USED IN THE OPTIMIZATION STUDY**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Via count</th>
<th>Via diameter (μm)</th>
<th>Via height (μm)</th>
<th>Via arrangement</th>
<th>Layer-2 line length (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>400</td>
<td>150</td>
<td>Single via</td>
<td>4.2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>250</td>
<td>150</td>
<td>4×1 inline</td>
<td>3.8</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>225</td>
<td>100</td>
<td>3×2</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>200</td>
<td>150</td>
<td>2×1</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>175</td>
<td>200</td>
<td>2×1</td>
<td>1.1</td>
</tr>
</tbody>
</table>

\[ R_{\text{ON}} \text{ was reduced sharply and saturated around 1.1 } \Omega \text{ for 115 V. Past this voltage, no significant change was observed. Measured turn-on and turn-off times were both approximately 10 ms for 78-V actuation and 40-V turn-off voltages, respectively.} \]
Here, $S_{21}$ and $S_{11}$ are the down-state insertion loss at high power and return loss at small signal, respectively. The equation considers a nonreflection case where the constant $S_{11}$ value of $-22.7$ dB at 3 GHz was used from the small-signal analysis.

Fig. 7. (a) Testing circuitry for batch-fabricated RF microrelay. Actuation voltage $V_G$ was used for the electrostatic actuation. $V_{SOI}$ was monitored to detect any leakage with a 1-MΩ resistor. ON-state resistance $R_{ON}$ included the contact resistance, the bridge resistance, and the parasitics. A 10-pF surface-mount capacitor was used for dc blocking. (b) High-power RF test setup (limited to 30 W at 3 GHz).

since the high-power test only included $S_{21}$ characterization at different power levels. It should be noted that the $S_{11}$ contribution to the output power has only a minor effect when compared to $S_{21}$, which is strongly related to contact degradation at high power levels. Fig. 12 shows the input–output power relation. The output power was relatively linear with the input power of up to 13 W. Beyond this power level, output power was reduced due to the degraded down-state insertion loss close to the point of failure.

A. Lifetime Testing

Lifetime tests were performed on microrelays packaged in nitrogen at atmospheric pressure. Two sets of experiments were conducted under hot switching conditions. The first set of experiments used 1-W RF power supplied at 3 GHz. The relay was switched at 0.5-Hz frequency with 50% duty cycle, providing 1-s on and 1-s off times. The second set of experiments used 10-W RF power supplied at 3 GHz, with a switching frequency of 0.2 Hz and 2% duty cycle, resulting in 0.1-s on and 4.9-s off times. The actuation voltage was kept at 120 V for both experiments similar to the conditions used for the high-power tests. Fig. 13 shows the $S_{21}$ for the up-state and the down-state in both sets of experiments. For 1-W power, the device failed at the $10^9$th cycle in the down-state where insertion loss was below $-0.9$ dB. The up-state isolation remained within $\pm 3$ dB of $-21$ dB throughout the test [Fig. 13(a)]. For 10-W power, the device failed after 8414 cycles in the down-state with similar insertion loss and isolation values to the 1-W case [Fig. 13(b)].
Fig. 8. (a) Displacement hysteresis for the microrelay. Actuation voltage was swept 0 V–120 V–0 V. Device pull-in and turn-off voltages were 78 and 40 V, respectively. Combined stiffness of Parylene-coated cantilever and the contact bridge was 125 N/m, as derived from these measurement results. (b) Experimental results showing the change of total series ON-state resistance with increasing actuation voltage. Test was run on packaged devices with nitrogen at atmospheric pressure. ON-state resistance at pull-in was 15 Ω. Further increase of actuation voltage resulted in a lower resistance due to larger contact forces. ON-state resistance saturated past 115 V and was approximately 1.1 Ω.

B. Package Testing

Package testing for the devices followed MIL-STD-883G hermeticity standards (Polaris Electronics Corp., KS). A total of nine empty packages—filled with nitrogen at atmospheric pressure—were tested. The testing involved He bombing of packages at 60-lb/in² pressure for 1 h. The packages were then removed from bombing chamber and placed in a vacuum chamber at 1 Pa for He detection. The packages were tested at three different time intervals to allow for any He residue that might be trapped in the epoxy to be released. The He detection was performed immediately after the bombing, 30 min after the bombing, and 60 min after the bombing, and it was repeated for a subset of the packages. The testing scheme and results are summarized in Table II. The pass/fail threshold for this standard is $5 \times 10^{-8}$ atm cc/s. The packages 1–3 narrowly failed when tested immediately after the bombing, potentially due to trapped He still present on the epoxy. Package 2 passed the test when retested after 60 min of bombing, and package 3 passed when retested after both 60 and 30 min of bombing. Packages 5 and 6, and 8 and 9 also passed the test similarly after 30 and
Fig. 11. High-power handling test for the packaged RF microrelay (nitrogen in atmospheric pressure). Tests were performed at 3 GHz and up to 30 W of RF power (test setup limit), at 120-V actuation voltage, and 1-s ON-state time. Insertion loss in the down-state was below $-0.2$ dB for up to 5 W and decayed down to $-0.9$ dB at 20 W where the device failed due to microwelding. The up-state isolation was approximately $-21$ dB over the 12 gain steps, and self-actuation was not observed.

Fig. 12. Output power estimated from the input power, down-state small-signal $S_{11}$, and down-state high power $S_{21}$. Output power exhibited a relatively linear relationship with the input power up to approximately 13 W, beyond which the linearity was distorted due to dominant effect of down-state $S_{21}$ which degrades significantly at the point of failure at 20 W. The red-dotted line represents linear reference between input and output powers.

60 min of bombing, respectively. After testing, the packages were examined under an optical microscope for any cracks or deformation that might result from high-pressure He bombing and lead to misinterpretation of the results. No such deformations were observed for any of the nine packages (Fig. 14).

V. DISCUSSION AND CONCLUSION

In summary, the assembly and packaging of microrelays directly onto the PCB showed promising results. Stainless steel cantilevers with Pt-Rh contact elements were fabricated and tested; the singulated microrelays had a footprint of 8.4 mm$^2$. The pull-in voltage was 78 V; ON-state resistances as low as 1.1 $\Omega$ were observed for an increased actuation voltage of 115 V. At low power levels, the down-state insertion loss and up-state isolation were better than $-0.25$ and $-15$ dB for up to 5 GHz, respectively. Because of the insulation properties and very low loss tangent of the LCP package lid used, the packages introduced minimal degradation in RF performance. Overall, the experimental data were in good agreement with HFSS simulation results. Maximum deviations for the down-state and up-state were 0.1 and 5 dB, respectively. The reason for such deviation was the resonance possibly induced due to the assembly imperfections.

High-power tests were performed on the packaged devices operating in nitrogen at atmospheric pressure for power levels as high as 30 W at 3 GHz. The power and the frequency limits were due to the amplifier used in this study. For 1-s ON-state times, the devices failed in the down-state at 20 W and exhibited
an $S_{21}$ of $-0.9$ dB. The failure was due to the microwelding of the contacts under extreme local heating. Up-state isolation was nearly constant at approximately $-21$ dB, and no self-
actuation was observed. A packaged microrelay operating in nitrogen at atmospheric pressure had a lifetime of 10 913 cycles under the hot switching conditions for 1 W of RF power with 1-s on and off times. Another packaged microrelay operating at 10-W RF power with 0.1-s on and 4.9-s off times operated for 8414 cycles.

Future provisions to further increase the power handling include the following: 1) dissipating the heat generated at the contacts more effectively by using different substrates with high thermal conductivity such as multilayer low-temperature cofired ceramics [31], [32]; 2) customization of the metal on the PCB for better contact performance; and 3) increase of RF impedance to 75 $\Omega$ for reduced rms current which leads to temperature increase at the contacts. Fig. 15 benchmarks this device and compares the maximum RF power handling and footprint with state-of-the-art micromachined relays. Hot and cold switching conditions are shown in the parentheses.

Fig. 14. Device packages were observed under optical microscope after testing for any deformation or crack formation in the cured epoxy as a possible reason for high-pressure He bombing. No such formations were observed for any of the nine packages.

Fig. 15. Device benchmarking. The maximum RF power handling and footprint of this work are compared with state-of-the-art microrelays. Hot and cold switching conditions are shown in the parentheses.

REFERENCES


Fatih M. Ozkeskin (S’11–M’11) received the B.S. degree in mechatronics engineering from Sabanci University, Istanbul, Turkey, in 2006, the M.S. degree in mechanical engineering from Texas A&M University, College Station, in 2008, and the Ph.D. degree in mechanical engineering from the University of Michigan, Ann Arbor, in 2011.

He is currently a Process Engineer with Apple Materials, Inc., Santa Clara, CA. His research interests include MEMS switches and micro/nano manufacturing.

Sangjo Choi (S’09) received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1980, and the M.S. degree in electrical engineering in 1986 and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering in 1989 from the University of Michigan, Ann Arbor.

He is currently a Graduate Research Assistant with the Radiation Laboratory, University of Michigan.

Kamal Sarabandi (S’87–M’90–SM’92–F’00) received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1980, and the M.S. degree in electrical engineering in 1986 and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering in 1989 from the University of Michigan, Ann Arbor.

He is currently the Director of the Radiation Laboratory and the Rufus S. Teeddale Professor of Engineering in the Department of Electrical Engineering and Computer Science, University of Michigan. His research areas of interest include microwave and millimeter-wave radar remote sensing, meta-materials, electronic wave propagation, and antenna miniaturization. He has 25 years of experience with wave propagation in random media, communication channel modeling, microwave sensors, and radar systems and leads a large research group including two research scientists and 14 Ph.D. students. He has graduated 37 Ph.D. and supervised numerous postdoctoral students. He has served as the Principal Investigator on many projects sponsored by the National Aeronautics and Space Administration (NASA), Jet Propulsion Laboratory, Army Research Office, Office of Naval Research, Army Research Laboratory, National Science Foundation, Defense Advanced Research Projects Agency, and a large number of industries. Currently, he is leading the Center for Microelectronics and Sensors funded by the Army Research Laboratory under the Micro-Autonomous Systems and Technology (MAST) Collaborative Technology Alliance (CTA) program. He has published many book chapters and more than 180 papers in refereed journals on miniaturized and on-chip antennas, meta-materials, electromagnetic scattering, wireless channel modeling, random media modeling, microwave measurement techniques, radar calibration, inverse scattering problems, and microwave sensors. He also has received more than 420 papers and invited presentations in many national and international conferences and symposia on similar subjects.

Dr. Sarabandi served as a member of the NASA Advisory Council appointed by the NASA Administrator in two consecutive terms from 2006 to 2010. He serves as the Vice President of the IEEE Geoscience and Remote Sensing Society (GRSS) and is a member of the Editorial Board of the PROCEEDINGS OF THE IEEE. He was an Associate Editor of the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION and the IEEE SENSORS JOURNAL. He is a member of Commissions F and D of URSI and is listed in American Men and Women of Science, Who’s Who in America, and Who’s Who in Science and Engineering. He was the recipient of the Henry Russel Award from the Regent of the University of Michigan. In 1999, he received a GAAC Distinguished Lecturer Award from the German Federal Ministry for Education, Science, and Technology. He was the recipient of the 1996 EEECS Department Teaching Excellence Award and the 2004 College of Engineering Research Excellence Award. In 2005, he received the IEEE GRSS Distinguished Achievement Award and the University of Michigan Faculty Recognition Award. He also received the Best Paper Award at the 2006 Army Science Conference. In 2008, he was awarded a Humboldt Research Award from the Alexander von Humboldt Foundation of Germany and received the Best Paper Award at the IEEE Geoscience and Remote Sensing Symposium. He was also awarded the 2010 Distinguished Faculty Achievement Award from the University of Michigan. The IEEE Board of Directors announced him as the recipient of the 2011 IEEE Judith A. Resnik Medal. In the past several years, joint papers presented by his students at a number of international symposia (IEEE APS’95,’97, ’00,’01,’03,’05,’06,’07; IEEE IGRASS’99,’02,’07,’11; IEEE IMS’01; USNC URSI’04,’05,’06,’10; AMTA ’06; URSI GA 2008) have received Best Paper Awards.
Yogesh B. Gianchandani (S’86–M’86–SM’05–F’10) received the B.S. degree from the University of California, Irvine, in 1984, the M.S. degree from the University of California, Los Angeles, in 1986, and the Ph.D. Degree from the University of Michigan, Ann Arbor, in 1994, all in electrical engineering.

He is currently a Professor at the University of Michigan, Ann Arbor, with a primary appointment in the Department of Electrical Engineering and Computer Science and a courtesy appointment in the Department of Mechanical Engineering. He also serves as the Director of the Center for Wireless Integrated MicroSensing and Systems (WIMS²). His research interests include all aspects of design, fabrication, and packaging of micromachined sensors and actuators and their interface circuits. He has published more than 250 papers in journals and conference proceedings and has about 35 U.S. patents issued or pending. He was a Chief Coeditor of Comprehensive Microsystems: Fundamentals, Technology, and Applications, published in 2008.

Dr. Gianchandani serves several journals as an Editor or a Member of the Editorial Board. He served as General Cochair for the IEEE/ASME International Conference on Micro Electro Mechanical Systems (MEMS) in 2002. From 2007 to 2009, he also served at the National Science Foundation as the Program Director for Micro and Nano Systems within the Electrical, Communication, and Cyber Systems Division (ECCS).