PARALLEL DISCHARGE WITH PARTITIONED ELECTRODE ARRAYS FOR ACCELERATED BATCH MODE MICRO-EDM

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ABSTRACT

This paper reports on advances in the throughput of micro-electro-discharge machining (micro-EDM) technology by increasing the spatial and temporal multiplicity of discharge pulses. Lithographically fabricated electrode arrays are used in conjunction with various pulse generation schemes, resulting in $>10^2$× improvement in throughput compared to single electrodes. Increasing the number of pulse generation circuits distributed across electrode arrays increases the machining rate several fold, but compromises surface smoothness. A modified pulse generation scheme that exploits the parasitic capacitance of the interconnect offers similarly high machining rates and is more amenable to integration. Stainless steel workpieces of 100 µm thickness were machined by 100 µm x 100 µm square cross section electrodes using in 85 s using an 80 V power supply. Surface smoothness was unaffected by electrode multiplicity. Using electrode arrays with four circuits, batch production of 36 WC-Co gears with 300 µm outside diameter and 70 µm thickness in 15 min. is demonstrated.

Keywords: electro-discharge-machining, LIGA, high-aspect ratio

I. INTRODUCTION

Micro-electro-discharge machining (micro-EDM) is an attractive microfabrication technique that can be used to cut any electrically conductive material, including steel, graphite, silicon, and even permanent magnets. It involves the sequential discharge of electrical pulses between a microscopic electrode and the workpiece while both are immersed in a dielectric oil [1]. The pulse discharge timing is controlled by a simple RC circuit. Although micro-EDM has been commercially used for applications such as ink-jet nozzle fabrication, traditional micro-EDM is limited in throughput because it is a serial process that uses a single electrode with a simple cylindrical shape. To overcome this limitation, in recent efforts single electrodes have been replaced by LIGA fabricated electrode arrays in order to achieve parallelism and increase throughput [2-4].

In [4], it was shown that although the presence of multiple electrodes can increase spatial parallelism, temporal parallelism is not achieved if a single pulse discharge circuit is used because only one electrode fires at a time. Further gains in throughput can be achieved by partitioning the electrode array into segments, each of which is controlled by a separate RC circuit. An array of eight electrodes comprised of four segments was assembled on a glass substrate. The machining rate achieved when separate pulse control circuit was connected to each electrode was more than twice that with a single shared RC circuit. These results suggest a path of investigation for further increases in throughput.

This effort explores the use of lithographically patterned thin film interconnect underneath LIGA fabricated electrode arrays (Fig. 1) in conjunction with multiple pulse generation circuits. Both spatial density of the electrodes and temporal density of the pulse discharges are increased. The impact of parasitic capacitance between the interconnect and the substrate on surface roughness is investigated. A modified pulse timing circuit which exploits the parasitic capacitance and demonstrates improved surface smoothness is presented.

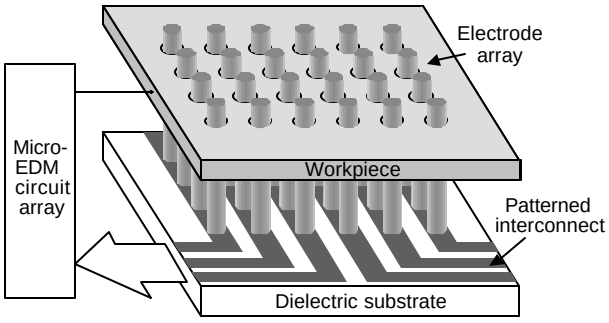

Fig. 1: Conceptual diagram of accelerated batch mode micro-EDM with partitioned electrode arrays

II. FABRICATION & ASSEMBLY

Arrayed electrodes can be fabricated on thin film interconnect metal using a two-mask sequence similar to sacrificial LIGA process [5]. The interconnect pattern is formed on 0.5 µm thick oxide on a Si substrate by etching an 1 µm thick Ti/Cu electroplating base. Figure 2 shows Cu electrodes of 10 µm wall thickness and 300 µm height intended for cutting gears. The connection to pulse timing circuits is made by wire bonding to contact pads along the array perimeter. Using these electrodes, 70 µm thick WC-Co gear clusters were successfully produced (Fig. 3). The upper

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SEM image in Fig. 3 shows a sample of 36 gears that were cut in parallel in 15 min. using four circuits. The lower image shows gears that took about 50 min. under similar conditions because of the larger surface area. Even so, this represents $>10^2$X improvement in throughput compared to single electrodes.

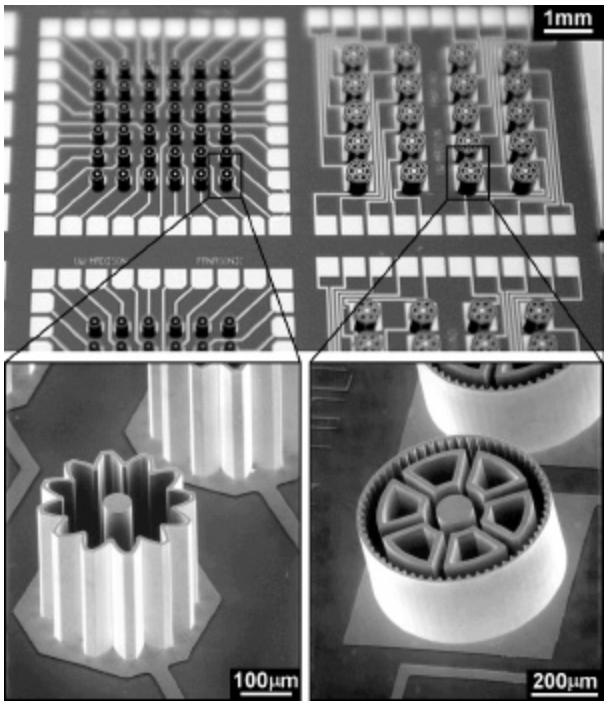

Fig. 2: Cu electrode arrays with patterned interconnect.

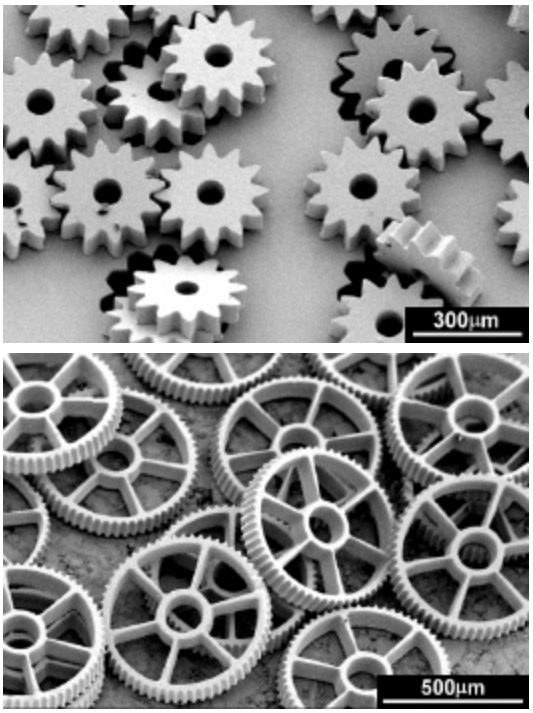

Fig. 3: WC-Co super hard alloy gears cut from a 70 µm thick workpiece using electrode arrays of Fig. 2.

III. MACHINING CHARACTERISTICS

In order to systematically evaluate the characteristics of partitioned electrode arrays with lithographically patterned interconnect, eight Cu electrodes with 100µm x 100µm square cross section and individual leads were connected to varying numbers RC timing circuits in different groups. Figure 4 illustrates the setup.

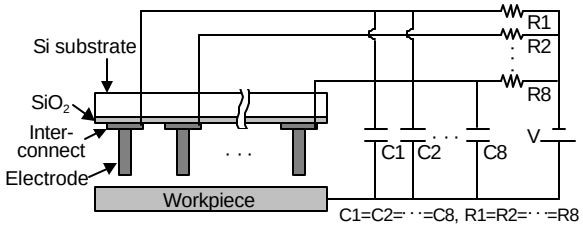

Fig. 4: Circuit setup for 8 electrode array.

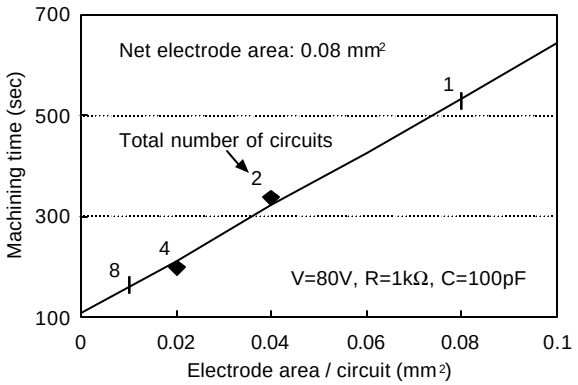

Fig. 5: Machining times for 100 µm depth into stainless steel with different numbers of RC circuits.

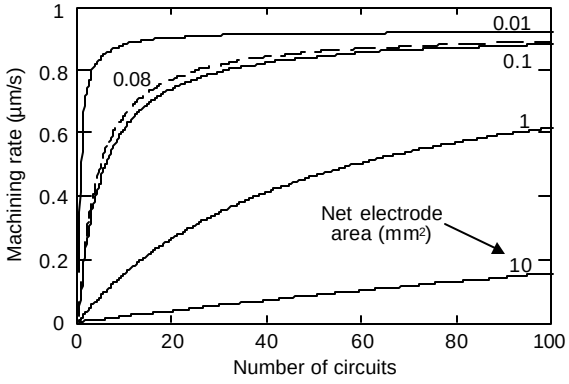

Fig. 6: Projected machining rates for various electrode areas as a function of RC pair multiplicity.

Figure 5 shows the machining times for 100 µm depth into stainless steel samples as a function of electrode cross-sectional area per circuit. For each datum, the eight electrodes were equally distributed between the number of RC pairs indicated in the figure. In each case, *R* was 1 KΩ, *C* was 100 pF, and the supply

voltage was 80 V. It is evident that the machining time increases linearly with electrode area per circuit. Using eight RC pairs provides a machining rate >200% higher than a single RC pair. Based on these measurements, machining rates can be projected for further increases in the number of RC pairs used. These calculations are presented in Fig. 6 using net electrode area as a variable parameter. The results suggest that the benefit of increasing RC pairs diminish as the electrode area per circuit drops below about 0.01 mm^2.

Although the use of multiple RC pairs increases throughput, it can have a deleterious effect on the roughness of the machined surface. Figure 7 compares two surfaces machined by the 8 electrode array: one using eight RC pairs and the other with a single RC pair. It is clear that the former is substantially rougher. A single power supply was used in both cases. Figure 7 also shows the trace of a single current pulse triggered by the discharge measured at the workpiece where it connects to the external lead. The increase in pulse amplitude and duration with the number of RC pairs used in this scheme increases the net energy per discharge to a level that compromises surface quality, and consequently, precision.

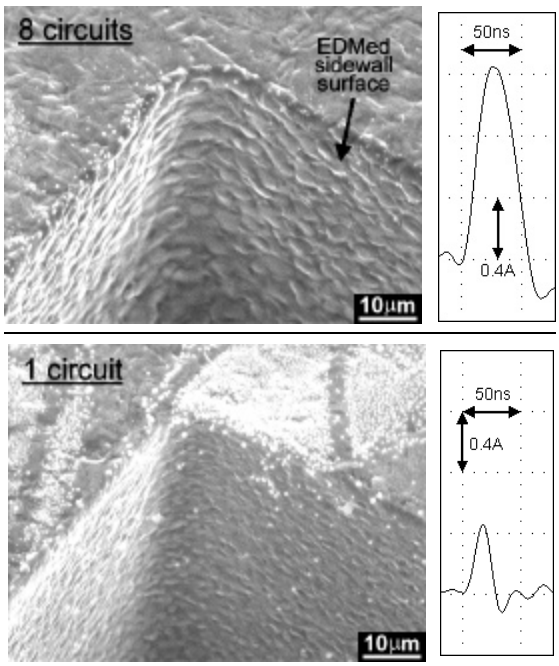

Fig. 7: Comparison of the roughness of machined surfaces and associated discharge pulse currents when using 8 circuits (upper) and 1 circuit (lower).

The increase in pulse discharge energy can be largely attributed to the parasitic capacitance associated with the thin film patterned interconnect. As shown in Fig. 8(a), C_{p1a}, the capacitance between this metal layer and the Si substrate exists essentially in parallel with the external capacitance C_e, which, together with the external resistance R, is intended to control the pulse timing. Other parasitic components that occur between the workpiece and various facets of the electrode are typically 10^2-10^4 smaller than C_{p1a}. Furthermore, the Si substrate, which is electrically floating in the conventional micro-EDM scheme, connects all the C_{p1} elements together, and provides a path for cross-talk between the electrodes that can affect pulse timing. For example, in Fig. 8(a), a discharge arc may raise the potential of one electrode, but capacitive coupling through the series combination of C_{p1a} and C_{p1b} may also elevate the voltage of the neighboring electrode, temporarily suppressing a discharge there. In the eight electrode experiment described above, the measured value of this series combination is 95 pF, which means that a single C_{p1a} is 190 pF because every segmented interconnect and contact pad in the setup has the same area. This is in excellent agreement with the theoretical estimate for the 3 mm^2 pad area for each electrode. Despite its adverse effects, C_{p1} offers an opportunity to eliminate C_e and simplify distributed micro-EDM.

IV. CIRCUIT OPTIMIZATION

A pulse discharge timing circuit that uses C_{p1} instead of C_e is shown in Fig. 8(b). The primary changes are that the external capacitors have been dropped and the electrode substrate is tied to the positive supply terminal. This configuration reduces cross-talk due to C_{p1} between electrodes.

The performance of new circuit was evaluated using an array of five Cu electrodes with 100µm x 100µm square cross section and individual leads. In a stainless steel workpiece, using an 80 V supply, 50 µm machined depth was achieved in 38 s at an average rate of 1.32 µm/s, whereas 100 µm depth was achieved in 86 s, at an average rate of 1.16 µm/s. The machining rates were the same whether a single electrode was connected to a single external resistor/circuit or all five electrodes were connected to five separate resistors. (In this experiment only one electrode was permitted to touch the workpiece.) As shown in Fig. 9, the smoothness of the machined surfaces in both the single electrode/single circuit case and the five electrode/five circuit case was visually comparable to the best smoothness achieved by the conventional pulse generator. The current pulses shown in Fig. 9 were of intermediate amplitude compared to those in Fig. 7.

A measure of precision in micro-EDM is the tolerance between an electrode and a hole machined by it. In Table I, this parameter is compared for four different cases. It is notable that the conventional circuit configuration in which all electrodes are connected in parallel to a single RC pair, provides the most modest tolerance, with a 9 µm mismatch between the electrode dimensions and the hole, whereas the configuration which uses the built-in parasitic capacitance provides the best performance with a 5 µm mismatch.

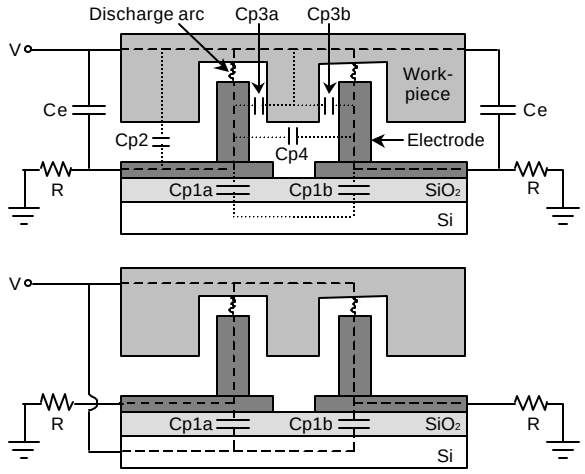

Fig. 8: (a-upper) The conventional pulse generation circuit showing parasitic capacitances; (b-lower) new circuit that uses parasitic capacitances instead of C_e.

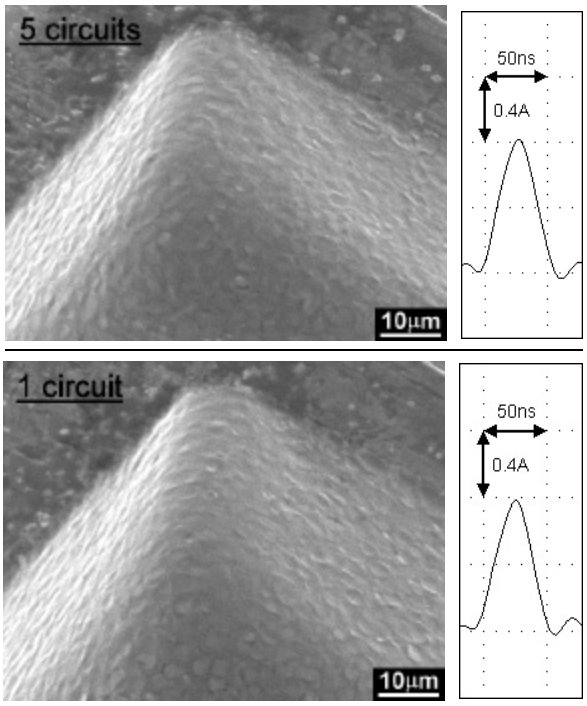

Fig. 9: Comparison of roughness of machined surfaces and associated discharge pulse currents when using 5 circuits (upper) and 1 circuit (lower) in setup of Fig. 8b.

Table I: Measured widths of holes machined by one 100µm x 100 µm electrode (in an array of 5) using various circuits.

Fig. 8a w/ 5 circuits	Fig. 8a w/ 1 circuit	Fig. 8b w/ 5 circuits	Fig. 8b w/ 1 circuit
109 µm	106 µm	105 µm	105 µm

V. CONCLUSION

The results obtained clearly demonstrate that using arrayed electrodes with separate pulse control circuits (RC pairs) for each array partition can vastly increase the machining rate. The rate increased linearly with the number of RC pairs used. However, scaling predictions based on measured results suggest that the benefits to machining rate diminish as the electrode area per RC pair decreases. Examination of machined surfaces and the discharge pulse waveforms revealed that as the number of RC pairs increases, the pulse energy and the surface roughness both increase. These may be attributed to the role of the parasitic capacitance between the patterned interconnect and the Si substrate, which increases the total effective capacitance and also permits cross-talk between electrodes.

A new circuit configuration that uses the on-chip parasitic capacitance of 190 pF per electrode instead of external capacitors was demonstrated. This arrangement is highly amenable to large size arrays because all the pulse control circuits elements can be integrated. In addition, it offers accelerated machining rates, and tighter tolerance than conventional schemes. Stainless steel workpieces of 100 µm thickness were machined by 100 µm x 100 µm square cross section electrodes in only 86 s using an 80 V power supply. The machined holes were only 5 µm wider than the electrodes, while the surfaces were smooth and did not exhibit any degradation with increased electrode or circuit multiplicity. These results demonstrate that highly integrated electrodes and circuits will be practical to use for high-yield and high throughput production. Using electrode arrays with four circuits, batch production of 36 WC-Co gears with 300 µm outside diameter and 70 µm thickness in 15 min. was demonstrated.

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