A CMOS DISSOLVED WAFER PROCESS FOR INTEGRATED P++ MICROELECTROMECHANICAL SYSTEMS

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ABSTRACT

This paper presents a fabrication technology for the integration of p++ microstructures with on-chip circuitry without restrictions upon device shape and size. It is a dissolved wafer technique that combines an electro-chemical etch-stop for the circuitry with an impurity-based etch-stop for the microstructures, both of which are defined in an n-epi layer on a p-type Si wafer. A CMOS op. amp. has been integrated with p++ accelerometers using this process. It has a gain of 68 dB and an output swing within 0.2 V of its power supplies, unaffected by the wafer dissolution. The accelerometers have 3 μm thick suspension beams and 15 μm thick proof masses. The structural and electrical integrity of the fabricated devices demonstrates the success of the fabrication process.

INTRODUCTION

In recent years the boron impurity-based dissolved wafer process has been repeatedly demonstrated as a powerful tool for forming microstructures in the thickness range of 2-20 μm. A few of the devices that have been fabricated with this technique include pressure sensors, tactile imagers, and neural probes [1]. Many of these devices incorporate silicon microstructures that are bonded to an insulating glass substrate. It is also possible to incorporate circuitry in lightly doped regions in the vicinity of these p++ Si microstructures by either surrounding it with a p++ ring and timing the etch, or by patterning the backside of the wafer to terminate the etch on (111) planes outside circuit region. Although these methods have been used in the past [2, 3], they are inherently wasteful of area and impose many restrictions upon the shape and size of the circuit blocks. There exists a need, from both cost and performance considerations, to develop a nonrestrictive and efficient technology to combine circuitry with p++ microstructures for next generation integrated systems.

This paper reports on a new fabrication technology to unify p++ microstructures with on-chip circuitry. This technology, henceforth referred to as the *active* dissolved wafer process (ADWP), has been used to integrate p++ micro-accelerometers with a CMOS operational amplifier intended for a switched capacitor readout. The circuit and the microstructure are both defined in the n-epi region of a p-type silicon substrate. The patterned Si surface is then electrostatically bonded to a glass wafer, and immersed in EDP (ethylene diamine pyrocatechol) until the p-type region dissolves away. The microstructures are formed by virtue of the boron impurity etch-stop, and the circuitry is protected by the application of an anodic bias to achieve an electro-chemical etch stop. Some electrical elements such as resistors or diodes may be integrated into each die to assist in electro-chemical etch-stop [4]. Figure 1 shows a schematic cross section of the finished device. We believe that in addition to integrating circuitry with p++ microstructures, it is possible to fabricate MEMS from lightly doped Si using this technology, obviating concerns of doping-induced stress effects.

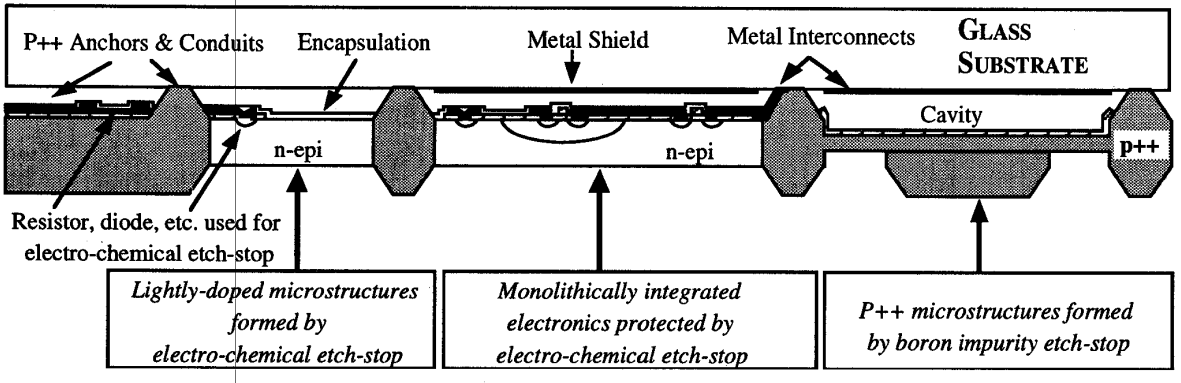

Fig. 1 A device cross section representing the capabilities of the active dissolved wafer process (ADWP).

The key challenges for the ADWP include: (a) the transfer of leads between the Si microstructure, the circuit, and the glass substrate; (b) the incorporation of an effective electro-chemical etch-stop to terminate the wafer dissolution at the n-epi junction; (c) the protection of the circuit during the electrostatic bonding and the wafer dissolution. The basic fabrication technique that has been developed and the results that have been obtained are discussed in the next two sections, followed by additional refinements that broaden the scope of the technology.

FABRICATION

The particular process sequence described here is used to integrate p++ Si microstructures with p-well CMOS in an n-epi wafer. It should be noted, however, that many variations are possible and that the technological approach can be generalized. The fabrication sequence requires a minimum of 13 masks, and uses one glass wafer for the substrate and one silicon wafer for the circuit and the microstructure. (Stacked, multi-level microstructures may be fabricated by using an additional Si wafer and a minimum of 2 masks for each additional level [5].)

The process begins by using one mask to inlay metal interconnect onto the glass substrate, which is then partially grooved along the scribe lines and kept aside while the silicon wafer is processed [5]. The silicon wafer is recessed in all areas except at the anchor points which will be used to attach it to the glass substrate. Following a p-well implant an oxide-masked deep boron diffusion is performed to define the thickest regions of the microstructures, such as the proof masses of accelerometers [3]. It also allows a front side electrical contact to the p-type silicon underlying the n-epi layer, which can be useful to some electro-chemical etch-stop methods [4]. The deep boron diffusion uses solid sources at 1175 °C for 16 hr., and it concurrently drives in the p-well. If the p-well formed in this manner is perceived as being too deep, one may reverse the order of these two steps, performing a 10 hr. deep boron diffusion before implanting the p-well, and then simultaneously driving in both for an additional 6 hr. The field implant and the field oxidation are performed next, defining the active regions in the p-well and n-epi areas where the NMOS and PMOS transistors will be formed respectively. The deep boron doped areas are included in the active region, since the growth of a thick field oxide here would deplete the boron concentration at the surface. The field oxidation has a high thermal budget, which is why it precedes the shallow boron diffusion that defines the suspension beams for the proof mass. It should be noted that the typical etch-stop thickness for the shallow and deep boron diffusions is 3 μm and 15 μm respectively. Following the shallow boron diffusion the sequence is similar to a standard CMOS process. An implant is performed to adjust the threshold voltages; the gate polysilicon is deposited, doped, and patterned; a 750 Å thick layer of capacitor oxide is grown thermally; and the second polysilicon layer is deposited, doped and patterned. The source/drain regions are then implanted, and a 7000 Å thick layer of CVD oxide is deposited. After this the contacts are patterned and 6000 Å of Al is deposited, followed by a layer of low temperature oxide (LTO). The LTO plays an important role in ADWP: as will be explained later, it is the final line of defense between the circuitry and the silicon etchant in the wafer dissolution process. Thus it is patterned to cover the circuit but expose the microstructures. Small areas of it may be retained, however, to serve as bushings that help in reducing stiction in the wet release process.

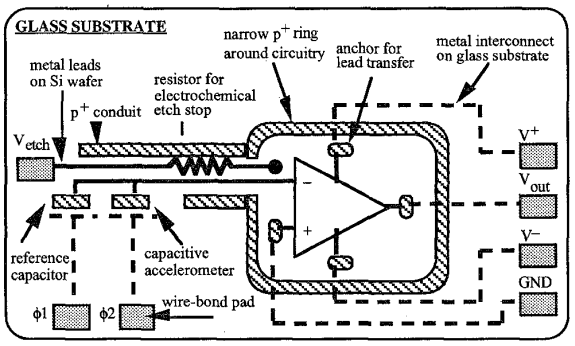

Fig. 2 A schematic of device showing the sensor, the detection circuit and the resistor used to terminate the etch electro-chemically.

At this point the silicon and glass wafers are electrostatically bonded together face-to-face. A metal ground plane on the glass substrate shields the circuitry from the high electric fields associated with this step. Lead transfer of signals between the microstructure and the circuit is accomplished by allowing the Si anchors to partially overlap metal interconnect on the glass [6]. Other leads from the electro-chemical etch control elements on each die run, via wires routed within conduits on the silicon surface, to the edge of the silicon wafer where connections can be made to external apparatus. The conduits are defined by deep boron diffusion and sealed to the glass by anchors that border them [4]. The circuitry is also similarly sealed off by a p++ anchor ring to reduce the access of the etchant into this area (Fig. 2). The glass-silicon sandwich is then immersed in the etchant to dissolve the p-type silicon wafer. Although a simple 2-terminal etch-stop may be adequate to protect the n-epi regions, the preferred approach is to use CECES [4], which provides automatic passivation on a die-by-die basis when the p-substrate is etched through. Its implementation is facilitated by a single resistor integrated onto each die, as illustrated in Fig. 2. At the beginning of the etch the circuitry is completely sealed off from the etchant by an anchor ring that encircles the wafer and by individual anchor rings that surround the circuit on each die. Toward the end of the etch, however, when the p++ microstructures have been etched through, some etchant is able to get through the individual rings because they have holes in them to permit lead transfer. We find that the LTO provides adequate protection against the etchant for this short duration of time. In addition, the flow of the fresh etchant and reaction by-products is so heavily constrained in this region that the risk of damage is further

reduced. If multi-level microstructures are desired, the next Si wafer is bonded to the glass substrate and re-immersed in the etchant at this point. Otherwise, the dice are separated along the grooves in the glass substrate in preparation for wire bonding, etc.

EXPERIMENTAL RESULTS

Figure 3 shows a photomicrograph of the fabricated device with several microaccelerometers and a circuit region which is in the bottom right corner of the die. A front view of the circuitry is presented in Fig. 4. The lead transfer points shown are junction isolated p++ anchors within the n-epi regions, each of which has a contact to one signal on the integrated circuit and also partially overlaps an inlaid metal line on the glass substrate (Fig. 2). Figure 5 shows a view of the junction between the n-epi region and the p++ ring surrounding it after the completion of the final etch. The dissolution of these two regions is prevented by electro-chemical and impurity-based etch-stops respectively.

The various microaccelerometers included on this mask set had differently designed suspensions. For all of the designs the suspension beams were 3 μm thick and the proof masses were 15 μm thick. The proof masses were perforated to reduce the squeeze film damping. The pick-off scheme was capacitive, with one electrode being the conductive silicon that constitutes the proof mass and the other electrode being metal inlaid on the glass substrate beneath it. The dimensions and characteristics of a typical design are listed in Table 1.

A two-stage CMOS op. amp. intended for use in a switched-capacitor readout was integrated with the accelerometers, along with some individual test transistors. The circuitry was characterized before the high voltage step of silicon-glass bonding, and once again after the dissolution of the silicon wafer. As shown in Table 2, the NMOS and PMOS threshold voltages changed by only about 20 mV, and the op. amp. gain changed by less than 2 dB as a result of these process steps. Figure 5 shows that the op. amp. frequency response is also basically unaffected by the bonding and dissolution.

PROCESS REFINEMENTS

As mentioned before, one of the key challenges for the ADWP is the transfer of leads between the circuitry, the MEMS, and the glass substrate. The approach presented above is to transfer the signal through p++ anchors in the n-epi region, as shown in Fig. 2. Unfortunately, since the anchors are junction isolated there is a large parasitic capacitance associated with this method, which can be very detrimental to some capacitive sensing schemes. An alternative approach, illustrated in Fig. 7, allows the signal to remain electrically isolated from the anchor even though lead transfer takes place at the same location. Sensitive signals between the circuitry and the MEMS may also be transferred using an air bridge. The air bridge is implemented by simply routing the metal line on the silicon surface from the circuitry (which is ringed by p++ anchors) to the p++ MEMS over unprotected n-epi region that will be dissolved away [6]. The metal bridge is chemically protected and mechanically supported by a layer of LTO above it and the CVD oxide below it. It should be noted that neither of these two new lead transfer techniques require any additional masks.

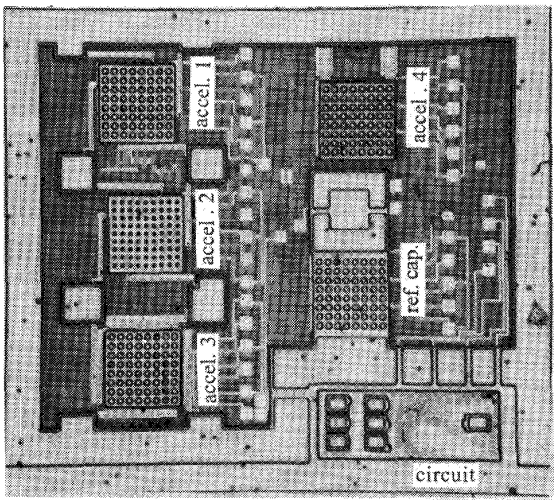

Fig. 3 Photomicrograph of a fabricated die, showing the backside of the circuit and several micro-accelerometers on a glass substrate. The die size is approximately 3 mm x 4 mm.

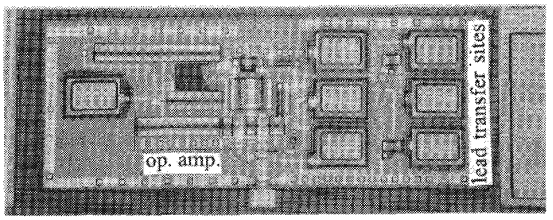

Fig. 4 The front side of the on-chip circuitry, showing the CMOS op. amp., some discrete devices, and the lead-transfer anchors.

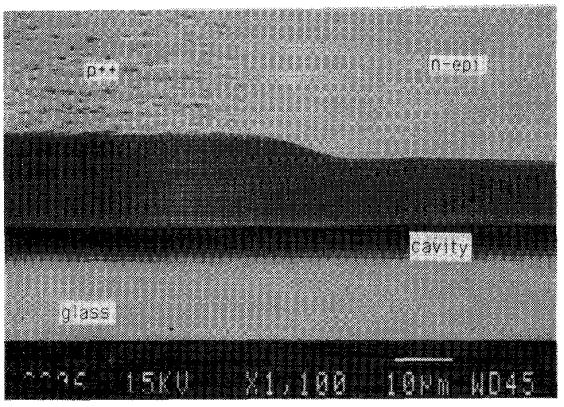

Fig. 5 An SEM of adjacent n-epi and p++ regions after the dissolution of the silicon substrate. The two regions were protected by the electro-chemical and boron impurity etch-stops respectively.

The MEMS fabricated by the process described above are defined purely by selective deep and shallow boron diffusions. As a result the beams and proof masses have curved sidewalls that are characteristic of the diffusion profiles. Straight sidewalls that are necessary for lateral sensing and drive can defined by selectively performing a dry anisotropic etch (RIE) that traverses through the entire thickness of the deep boron diffusion [5]. This step requires an extra mask, and is performed on the silicon wafer after all the other patterning steps are completed, i.e., just before it is bonded to the glass wafer.

CONCLUSIONS

We have proposed an active dissolved wafer process (ADWP) to integrate circuitry with p++ MEMS, and used it to fabricate p++ Si microaccelerometers with an on-chip CMOS op. amp. The microaccelerometers have 15 μm thick proof masses with 3 μm thick suspension beams, whereas the op. amp. has a low frequency gain of 68 dB and an output swing within 0.2 V of the rails. Its performance and those of some test transistors in its vicinity was characterized before electrostatic bonding to the glass substrate and after the dissolution of the Si wafer. The threshold voltages of the transistors were changed by only 20 mV as a result of these steps. It is clear from the structural and electrical integrity of the fabricated devices that the ADWP is an effective technique for integrating circuitry with p++ MEMS. By circumventing the shape and size restrictions imposed on the circuit regions by integration methods that have been explored in the past, it widens the range of possible applications. On-chip circuitry may be the key to higher performance and lower costs for many sensors and actuators in the future, and we expect that the ADWP will make important contributions in this arena.

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Table 1: Accelerometer specifications and measured performance characteristics.

mass dimensions (μm)	690 x 690 x 14.7
beam dimensions (per fold)	700 x 24 x 2.8 μm
mass	14.3 μgm
capacitor gap	1.47 μm
C_O	1.68 pF
Sensitivity	1.2 %/g
Bandwidth	75 Hz

Table 2: CMOS op. amp. specifications before and after the dissolution of the p-substrate.

Parameter	Before Etch	After Etch
V_{Tn}	0.93 V	0.94 V
V_{Tp}	-0.69 V	-0.71 V
A_O	69.8 dB	68.2 dB
output range	-4.73 to 4.80	-4.77 to 4.83
offset voltage	32 mV	27 mV

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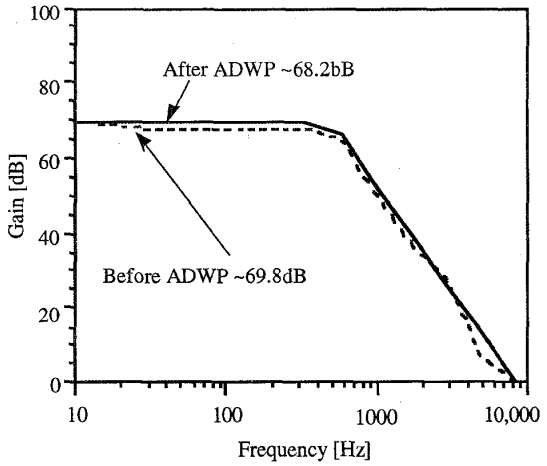

Fig. 6 Open loop gain of the CMOS op. amp. before and after the dissolution of the p-substrate.

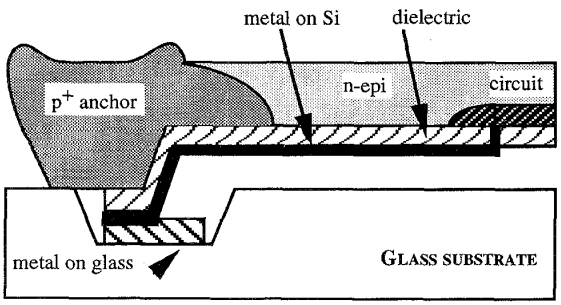

Fig. 7 An illustration of the low capacitance metal-to-metal lead transfer scheme.