

## Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions

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High performance Esaki tunnel diodes [L. Esaki, *Phys. Rev.* 109, 603 (1958)] based on small-diameter Ge/Si core/shell nanowires vertically grown on Si substrates are demonstrated. The devices exhibit pronounced negative differential resistance with peak-to-valley current ratio of 2.75, high peak current density of 2.4 kA/cm<sup>2</sup>, and high tunneling current density of 237 kA/cm<sup>2</sup> at 1 V reverse bias, all obtained at room temperature. The peak current is found to increase with temperature and the data can be well explained with a band-to-band tunneling model. These results suggest that Si-Ge heterojunction with low defect density can be obtained for device applications such as tunnel diodes and tunnel field-effect transistors. © 2011 American Institute of Physics. [doi:10.1063/1.3633347]

There is rising interest in devices based on quantum mechanical tunneling, such as the tunnel field-effect transistor (TFET)<sup>1,2</sup> and the Esaki diode,<sup>3</sup> as transistor scaling faces significant obstacles due to leakage and power consumption issues. Esaki diodes have been proposed in applications in neuromorphic circuits,<sup>4,5</sup> solar cells,<sup>6</sup> and microwave amplifiers,<sup>7</sup> and TFETs have been shown to be a leading candidate for low-power, high-performance electronics. However, tunneling currents in silicon-based devices are normally low due to its large band gap. Germanium offers high hole mobility and can enable higher tunneling currents owing to its smaller band gap.<sup>8</sup> However, heterogeneous integration of Ge-based devices on a Si substrate has remained challenging due to lattice mismatch during thin film growth. To this end, the nanowire geometry allows for radial strain relaxation<sup>9–11</sup> and the growth of heterojunctions with low defect density and sharp interfaces. Thus, the hybrid integration of bottom-up nanowire-based devices with traditional Si substrates offers possibilities to circumvent problems associated with conventional thin-film-based heterogeneous integration approaches. Such devices, based on epitaxially grown, vertical nanowire structures, also offer the potential to be integrated vertically on top of CMOS devices, thus further increasing the device density with 3-dimensional architectures.<sup>12</sup>

In this letter, we demonstrate the fabrication and the electrical characterization of heterojunction Esaki tunnel diodes based on small-diameter (~20 nm) Ge/Si core/shell nanowires grown vertically on a Si substrate. The heterojunction device exhibits a peak-to-valley current ratio (PVR) of 2.75 at room temperature, peak current density of 2.4 kA/cm<sup>2</sup>, and tunneling current density of 237 kA/cm<sup>2</sup>. Besides the practical applications of Esaki diodes listed above, this device structure is also useful for studying and evaluating the tunnel junction itself for other applications such as the TFET.

The device fabrication began with a Si (111) wafer degenerately doped with As to a resistivity of about 0.002 Ω-cm, which corresponds to an n-type doping level of  $\sim 4 \times 10^{19}$  cm<sup>-3</sup>.<sup>13</sup> 20 nm Au catalyst nanoparticles (Ted Pella, Inc.) were dispersed onto the substrate and vertical Ge nanowires were grown epitaxially using the vapor-liquid-

solid mechanism.<sup>14,15</sup> Nanowire nucleation took place at 380 °C for 1 min, followed by elongation at 300 °C for 45 min at a total pressure of 30 Torr (0.9% GeH<sub>4</sub> in H<sub>2</sub>). Fig. 1(a) shows a scanning electron microscopy (SEM) image of a representative vertical Ge nanowire, which is 20 nm in diameter and 1–2 μm in length. The sample was immediately transferred to an atomic layer deposition chamber where a 25 nm-thick conformal layer of Al<sub>2</sub>O<sub>3</sub> was deposited at 150 °C. Next, the Al<sub>2</sub>O<sub>3</sub> film was selectively removed from the nanowires by masking the substrate with a 30 nm-thick layer of spin-on-glass (semiconductor grade 700B from Filmtronics, Inc.), followed by wet etching in a temperature-controlled bath of 85% H<sub>3</sub>PO<sub>4</sub> for ~15 min. After a de-ionized (DI) water rinse and critical point drying, the sample was loaded into a tube furnace where a ~2 nm-thick Si shell was grown around the nanowires at 465 °C and 5 Torr with a flow of 20 sccm SiH<sub>4</sub>. The bottom portion of the core/shell nanowire was then encapsulated in a 250 nm-thick layer of spin-on-glass and cured at 300 °C for 45 min. To make electrical contact to the exposed upper portion, the sample was dipped briefly in buffered hydrogen-fluoride, rinsed in DI water, and immediately transferred to an evaporator where 100 nm Ni was deposited at an angle of 30°–45° to ensure sufficient contact area between metal and nanowire. A drive-in anneal was performed using rapid thermal annealing at 320 °C for 30 s in 5% H<sub>2</sub>/N<sub>2</sub> to form contact to the Ge core. The spin-on glass and Al<sub>2</sub>O<sub>3</sub> layers served to limit leakage current between the top and bottom contacts outside the nanowire contact window. Care was taken to ensure that the selected device under study contained only one nanowire. A schematic of the cross section of the completed device structure is shown in Fig. 1(b).

Several studies have shown that a Si shell can induce a hole gas in the Ge nanowire core and cause the Ge nanowire core to be degenerately p-type doped.<sup>16,17</sup> Thus, the band diagram of the junction between the Si substrate and the Ge nanowire core is that of an Esaki tunnel diode as shown in Fig. 1(c), where both sides have degenerate carrier densities. The devices were measured using a Keithley 4200 semiconductor analyzer with the bias applied to the Ni top contact while keeping the Si substrate grounded. Several devices were measured and showed similar characteristics. Data

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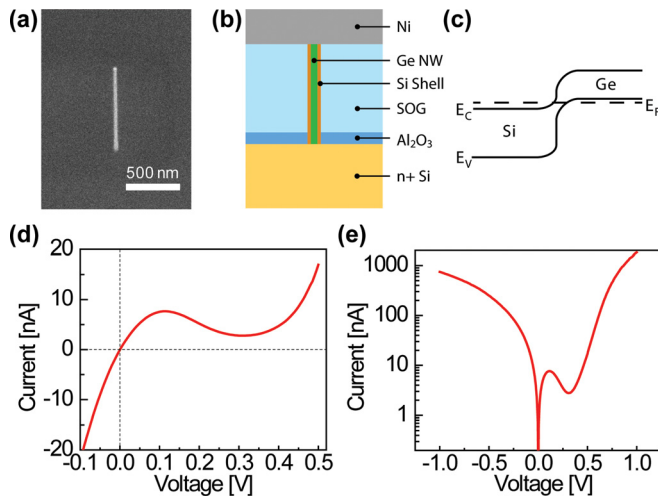


FIG. 1. (Color online) (a) SEM image of a vertical Ge nanowire (20 nm in diameter) epitaxially grown on a Si substrate, taken at a 45° viewing angle. (b) Schematic of the cross section of the completed vertical Esaki diode structure. (c) Equilibrium band diagram of the Si-Ge heterojunction. (d) Current-voltage characteristic of the selected device showing a PVR of 2.75 at room temperature. (e) Expanded semi-logarithmic plot of the voltage sweep shown in (d).

from the most representative device are shown here. Fig. 1(d) shows a current-voltage ( $I$ - $V$ ) plot taken at room temperature (294 K) showing pronounced negative differential resistance (NDR) with a PVR of 2.75, the signature behavior of an Esaki diode and confirming the band diagram of Fig. 1(c). The peak current density is estimated to be 2.4 kA/cm<sup>2</sup>, which is among the highest values reported for nanowire- or Si-based Esaki diodes.<sup>6,18</sup> Fig. 1(e) shows a semi-logarithmic plot taken from the same voltage sweep showing a larger voltage range at both forward and reverse bias. The reverse tunneling current density of 237 kA/cm<sup>2</sup> at 1 V reverse bias is also among the highest reported for nanowire-based devices<sup>6,19</sup> and confirms the potential of the Ge/Si nanowire-based tunneling devices.

Detailed temperature-dependence measurements were performed to elucidate the physical mechanisms of the observed current-voltage characteristics. Fig. 2 shows several representative  $I$ - $V$  curves at both forward and reverse bias taken at various temperatures. We first focus on the NDR region located in the forward-bias window from 0 to 0.4 V (Fig. 2(a)). The PVR increases as the temperature is decreased, with the highest PVR of 4.29 obtained at 86 K (the lowest temperature studied here). More importantly, the current in this region can be well-fitted to a model based on band-to-band tunneling<sup>20</sup>

$$I = I_p \frac{V_{in}}{V_p} \exp\left(1 - \frac{V_{in}}{V_p}\right) + I_{th0} \left[ \exp\left(\frac{V_{in}}{nkT}\right) - 1 \right], \quad (1)$$

where  $V_{in}$  is the voltage across the heterojunction,  $I_p$  and  $V_p$  are, respectively, the peak current and peak voltage of the NDR,  $I_{th0}$  is the saturation current for thermionic emission, and  $n$  is the diode ideality factor. Essentially, the first term in Eq. (1) models the direct band-to-band tunneling current which dominates at low bias, while the second term models the thermionic emission current which dominates at high bias. Using  $I_p$ ,  $V_p$ ,  $I_{th0}$ , and  $n$  as fitting parameters, we obtained very good fits to our data as seen in Fig. 2(a). To

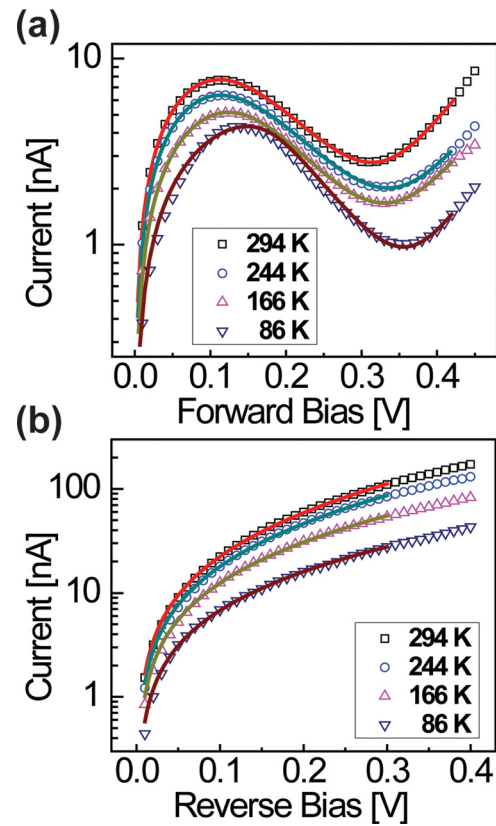


FIG. 2. (Color online) Measured (open symbols) and fitted (solid curves) current-voltage characteristics of the device at 4 different temperatures for both (a) forward and (b) reverse biases.

obtain the best fits, a temperature-dependent parasitic series resistance  $R_s$  was also included<sup>18</sup> so that  $V_{in} = V - IR_s$ , where  $V$  is the external applied voltage. The temperature-dependence of  $R_s$  is likely due to the presence of a small Schottky barrier at the interface between the Ni top contact and the Ge nanowire, and its inclusion into the model does not change the main results. From the fitting, the intrinsic peak voltage  $V_p \approx 0.082$  V was found to be roughly independent of temperature. The term for the so-called excess current, which accounts for tunneling via defect states in the band gap,<sup>20</sup> was not included here. We found that the excess current term was not needed to accurately reproduce the behavior of our device, suggesting that the device contains a low density of defect states and a high quality Si-Ge heterojunction between the n-type Si substrate and the p-type Ge nanowire.

Similar fittings were performed for reverse bias (Fig. 2(b)). Here, the current is modeled by the expression for tunneling across a triangular barrier<sup>20</sup>

$$I_R = \frac{CFV_R}{E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}\right), \quad (2)$$

$$F = \sqrt{\frac{qN(V_{bi} + V_R)}{\epsilon_s}}, \quad (3)$$

where  $V_R$  is the absolute value of the applied reverse bias,  $m^*$  is the effective tunneling mass,  $E_g$  is the effective band gap,  $\epsilon_s = 14\epsilon_0$  is the permittivity of the semiconductor (taken to be the average between that of Si and Ge<sup>20</sup>),  $F$  is the

maximum field at the junction interface,  $N$  is the doping concentration,  $V_{bi}$  is the diode built-in potential, and  $C$  is a device-dependent prefactor. From the literature, the effective tunneling mass  $m^*$  is estimated to be  $0.037m_0$  for the Si-Ge heterojunction.<sup>21</sup> The effective band gap is given by  $E_g = E_g(\text{Ge}) - \Delta E_C$ , where  $E_g(\text{Ge})$  is the band gap of Ge and  $\Delta E_C$  is the conduction band offset between Si and Ge, which is estimated to be 0.05 eV from the difference in electron affinities.<sup>20</sup>  $E_g(\text{Ge})$  has a temperature dependence established empirically as<sup>20</sup>

$$E_g(\text{Ge}) = 0.74 - 4.77 \times 10^{-4} \frac{T^2}{T + 235} \text{ eV.} \quad (4)$$

The series-resistance effect was not considered in this case since the Schottky barrier at the Ni/Ge contact would be forward-biased at these bias conditions and its contribution should be small. As a result, only two fitting parameters,  $N$  and  $V_{bi}$ , were used to fit all the curves at different biases and temperatures in Fig. 2(b). Excellent fits were obtained with  $N = 3 \times 10^{19} \text{ cm}^{-3}$  and  $V_{bi}$  ranging from 0.67 V to 1.17 V. The value of  $N$  is consistent with an assumption made in Eq. (3) that the doping level is similar on both sides of the junction.  $V_{bi}$  is given by  $qV_{bi} = E_g + E_p + E_n$ , where  $E_p(E_n)$  is the distance between the Fermi level and the valence (conduction) band edge. The fact that we obtained  $qV_{bi} > E_g$  is again consistent with the band diagram and the tunneling picture shown in Fig. 1(c). These analyses unambiguously verify that the band-to-band quantum mechanical tunneling model captures the dominant conduction mechanism in reverse bias, and again support the claim that the nanowire and the substrate form an effective tunnel junction for Esaki diode and TFET applications.

The temperature dependence of the peak current  $I_p$  is shown in Fig. 3. Theoretically,  $I_p$  can also be estimated from the tunneling model and has the following form:<sup>20,22</sup>

$$I_p = I_{p0} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}\right), \quad (5)$$

Here, the only temperature dependence term originates from the band gap  $E_g$ . Using Eq. (5) and keeping the same parameters used in the fitting results of Fig. 2, we obtained a good fit of  $I_p$  vs. temperature as shown in Fig. 3. This agreement suggests that the temperature dependence of  $I_p$  manifests itself only through the temperature dependence of the band gap (Fig. 3, inset), i.e., a reduction in  $E_g$  leads to a higher tunneling probability. This observation again justifies the use of Ge nanowires to form high-performance Esaki diodes and possibly TFETs.

In conclusion, we fabricated Esaki diodes from Ge/Si core/shell nanowires grown vertically on a Si substrate, showing a PVR of 2.75 at room temperature, a high peak current density of 2.4 kA/cm<sup>2</sup>, and a high tunneling current density of 237 kA/cm<sup>2</sup> at 1 V reverse bias. The data can be well-explained by band-to-band tunneling at both forward and reverse biases. The effective tunnel junctions based on small-diameter vertical nanowires are well-suited for the development of hybrid nanowire-CMOS systems, particularly low-power tunneling-based devices.

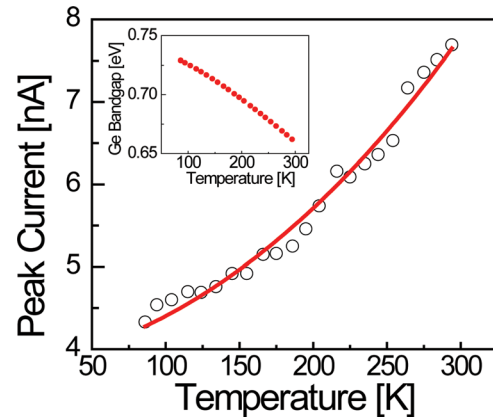


FIG. 3. (Color online) Measured peak current  $I_p$  vs temperature.  $I_p$  was extracted from the measured data (open circles) and is fitted using Eq. (5) (solid line). Inset: temperature dependence of the band gap of Ge used in the fitting.

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