Circuit Design for FPGAs in Sub-threshold Ultra-low Power Systems

Master of Science Thesis Defense of Yu Huang

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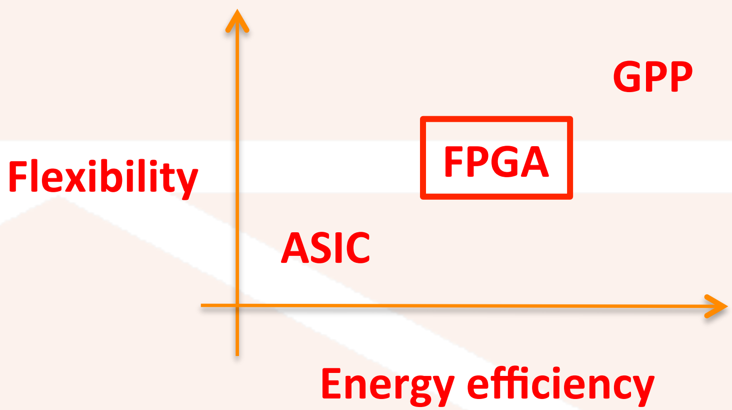
6/30/2015

Motivation

- Requirements of ubiquitous computing
  - Design cost
  - Small form−factor
  - Long-lasting
  - Energy efficient
  - Flexibility
- FPGA interconnect
  - Consumes 60%-70% power
  - Dominates delay and area
- Further energy efficiency in an ultra-low power(ULP) system

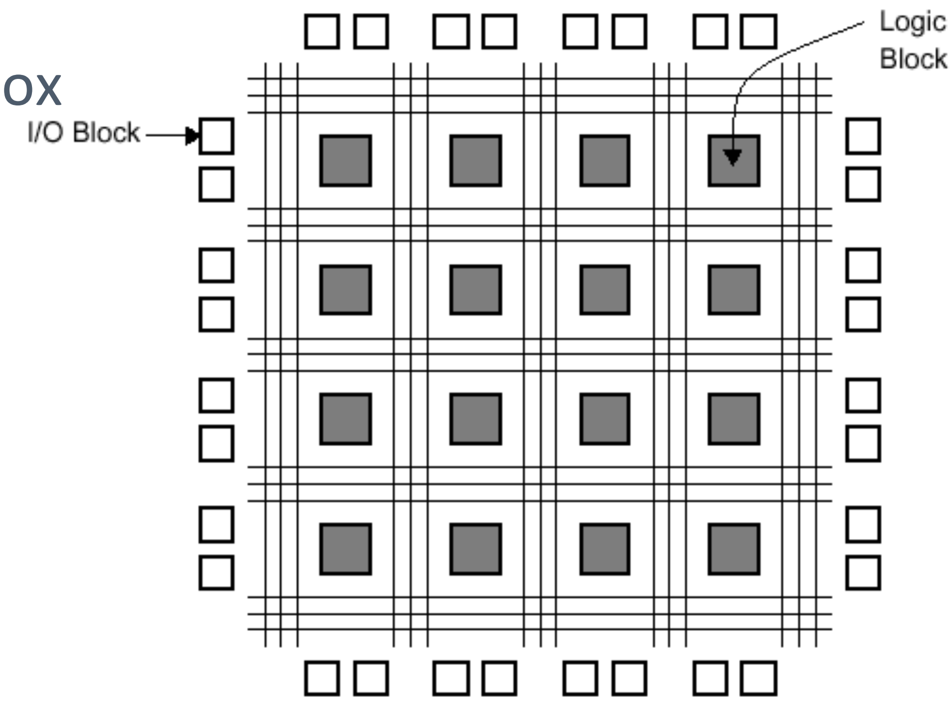


Outline

- Motivation
- Background of FPGA
- Optimization of the energy efficient low-swing interconnect for sub-threshold(SubVt) FPGAs
- Further energy reduction of FPGA interconnect: a voltage scaling technique
- An ultra-low swing single ended level converter design
- Conclusion and contribution

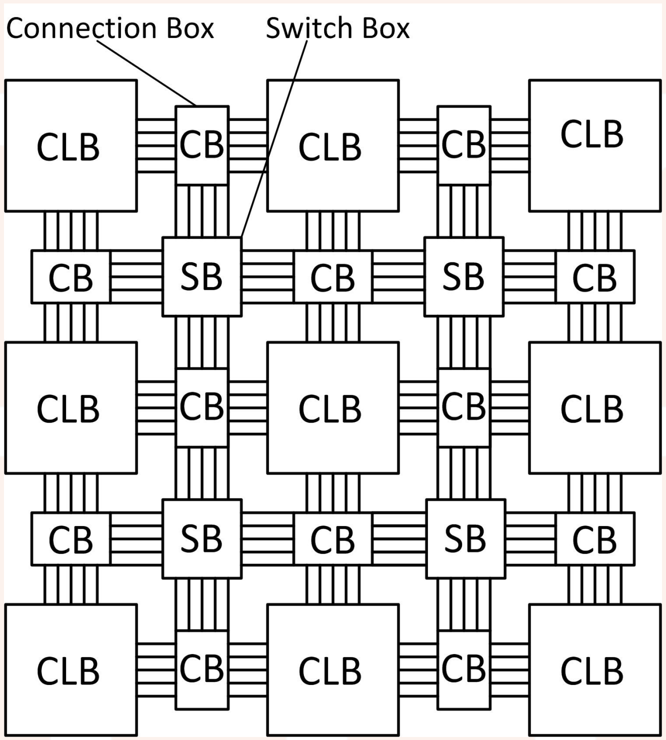
Background of FPGA

- Island-style FPGA architecture
  - CLB: Configurable(complex) logic block (or LB)
  - SB: Switch box
  - CB: Connection box

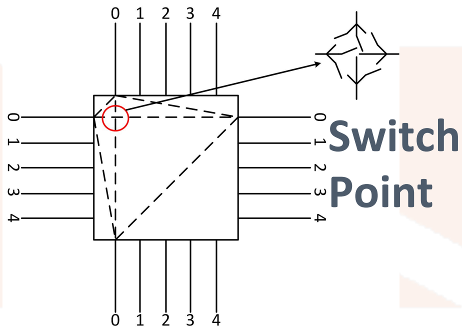


Background of FPGA

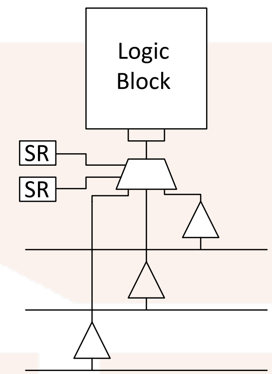
- Island-style FPGA architecture



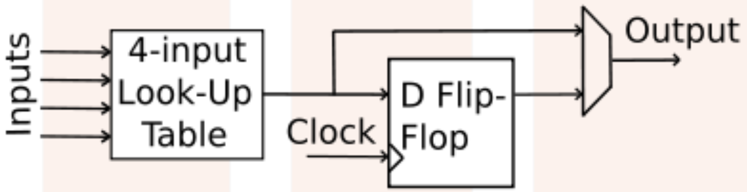
Switch Box



Connection Box

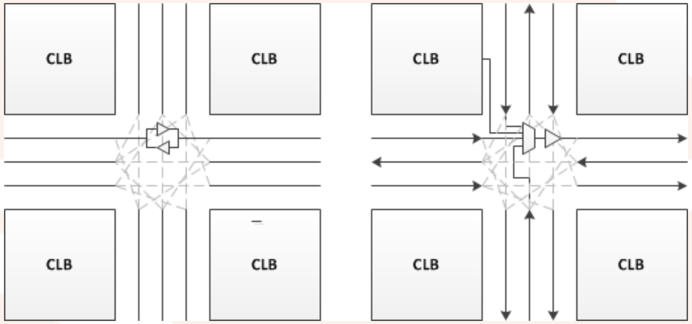


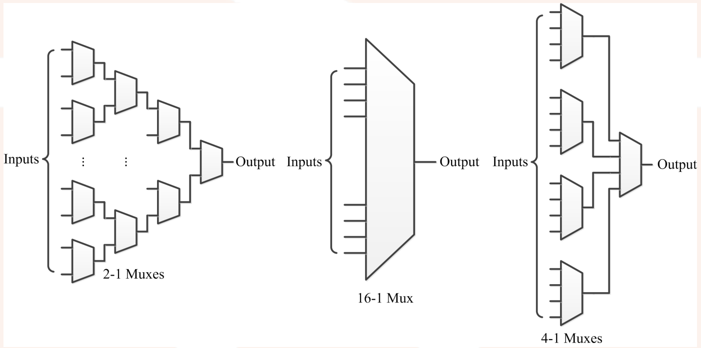
CLB (Basic Logic Element)



Optimization of subVt FPGA interconnect

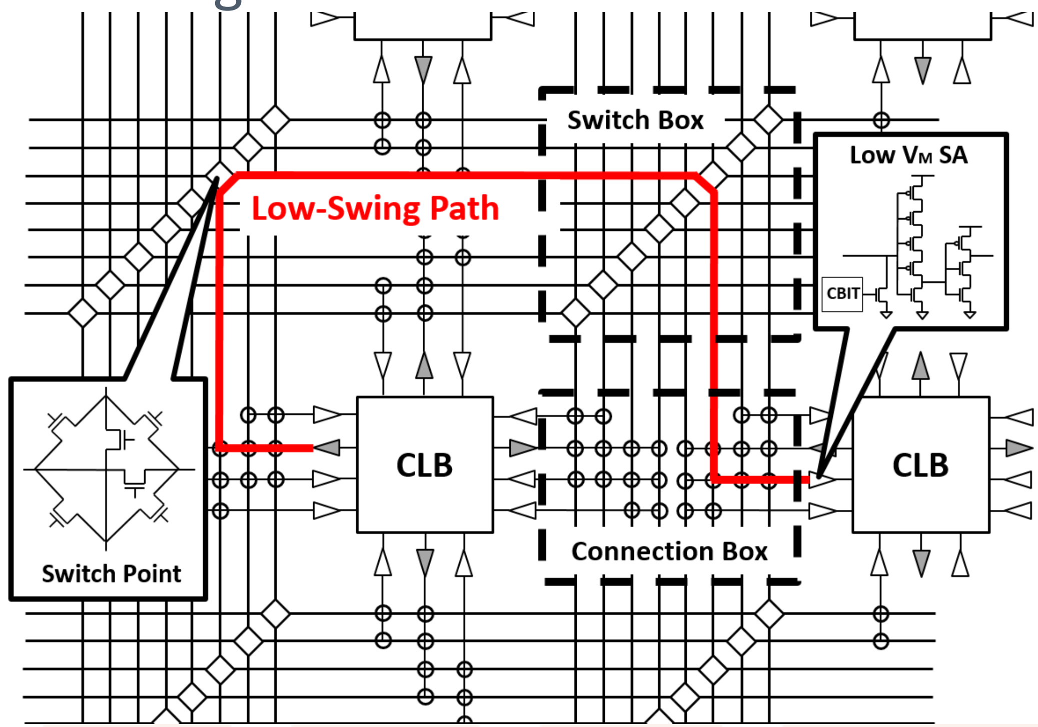
- Traditional options
  - Switch point
    - Bi-directional: tri-state buffers
    - Uni-directional: Mux and buffer
  - Connection box (will be compared)
    - Full mux
    - 1-stage mux
    - 2-stage mux





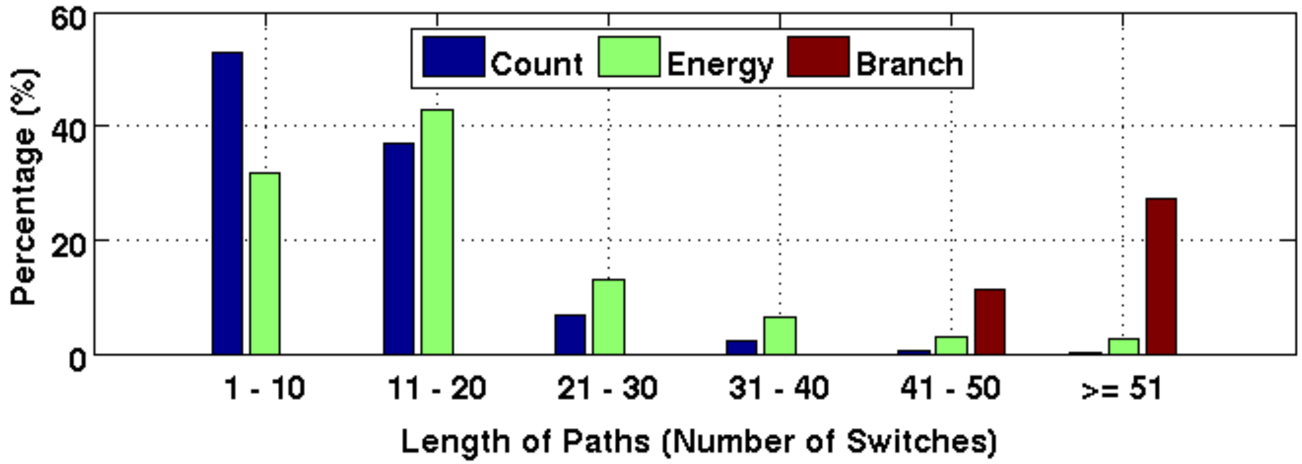
Optimization of subVt FPGA interconnect

- Basic structure of low-swing interconnect
  - Switch point: Pass Gate/ Transmission Gate
  - Sense amplifier: pull the signal back to nominal voltage
    - Weaken PUN
    - Sensitive for low-swing input
  - Connection box: Still mux-based



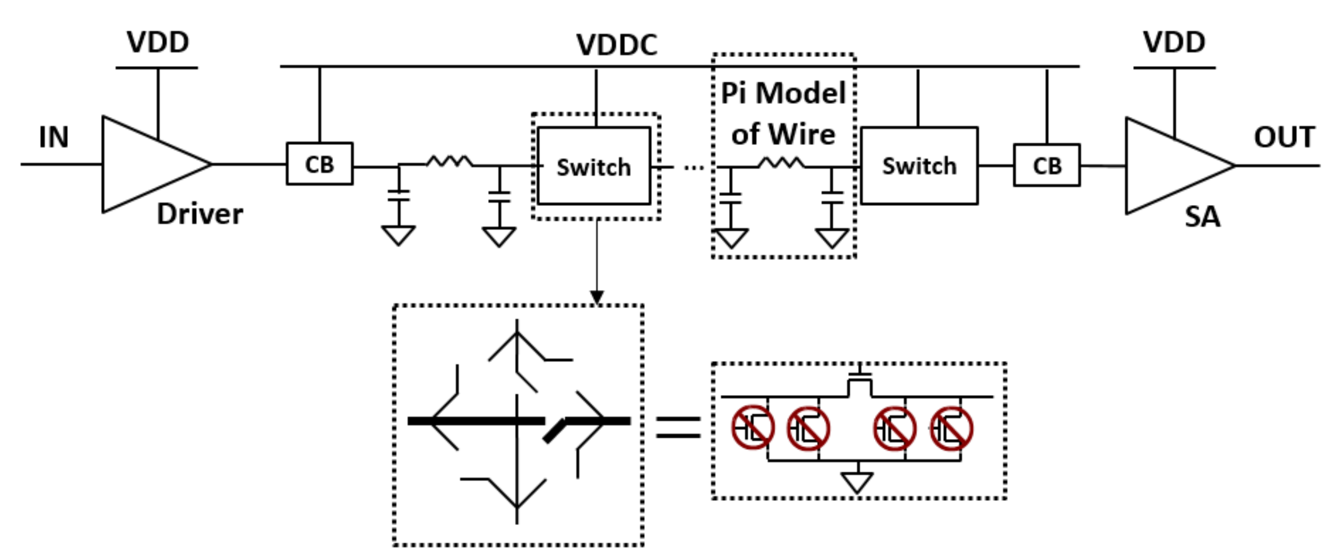
Optimization of subVt FPGA interconnect

- Global interconnect model
  - Based on MCNC benchmarks: 20 applications
  - MCNC benchmarks path distribution
    - Length: number of switches of the path
  - Observation:
    - Shorter than 40: occupy 98% of the total switch count,
      94% of the total global interconnect energy
      few branches.



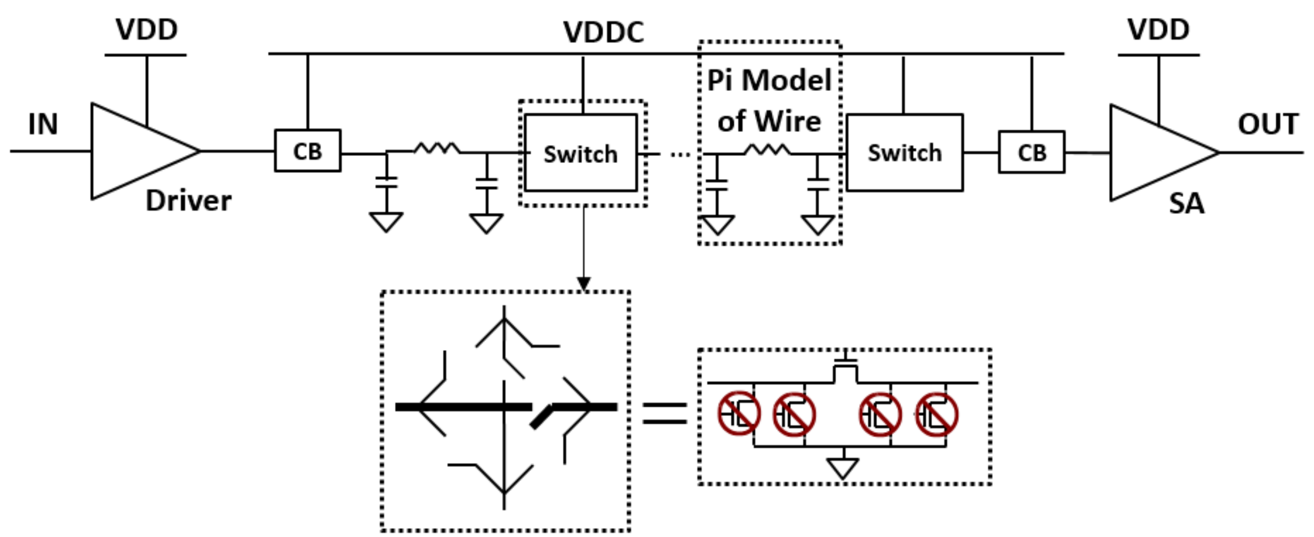
Optimization of subVt FPGA interconnect

- Global interconnect model
  - Length: 40 switch points (5 switches each)
  - No branches: worst case
  - Wire segment: pi model
  - Dual-VDD scheme: VDDC>VDD (previous work)



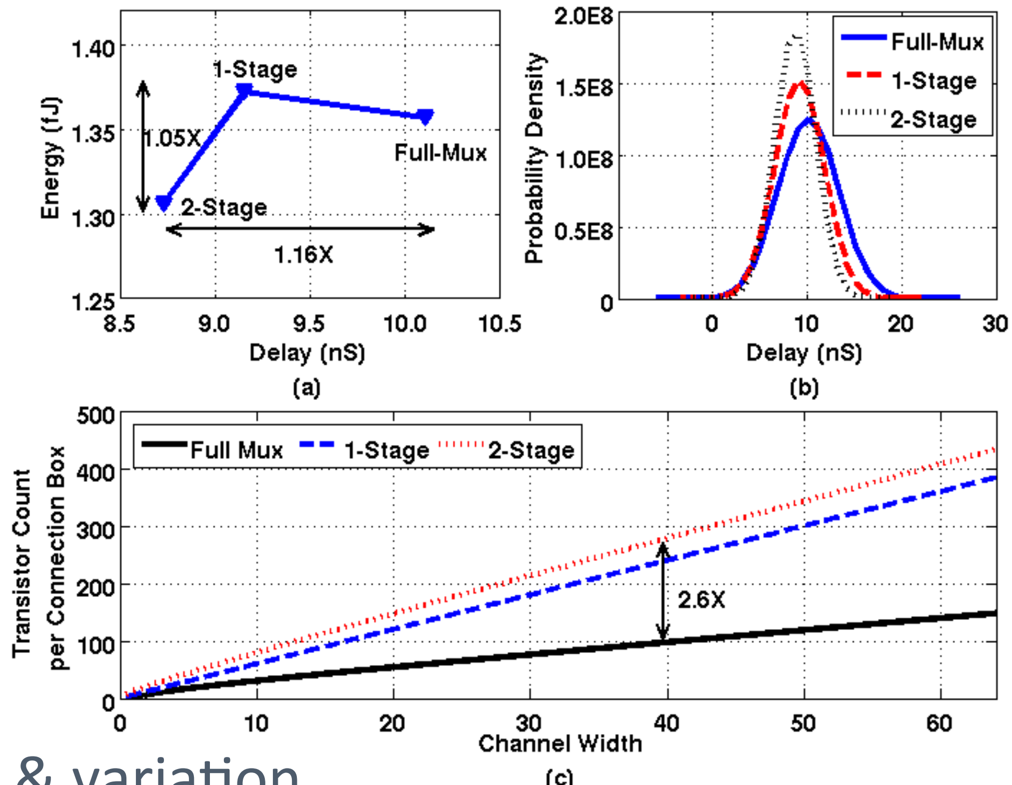
Optimization of subVt FPGA interconnect

- Redefine the problem
  - Dual-VDD: optimal combination?
  - Connection box
  - Driver
  - Switch point



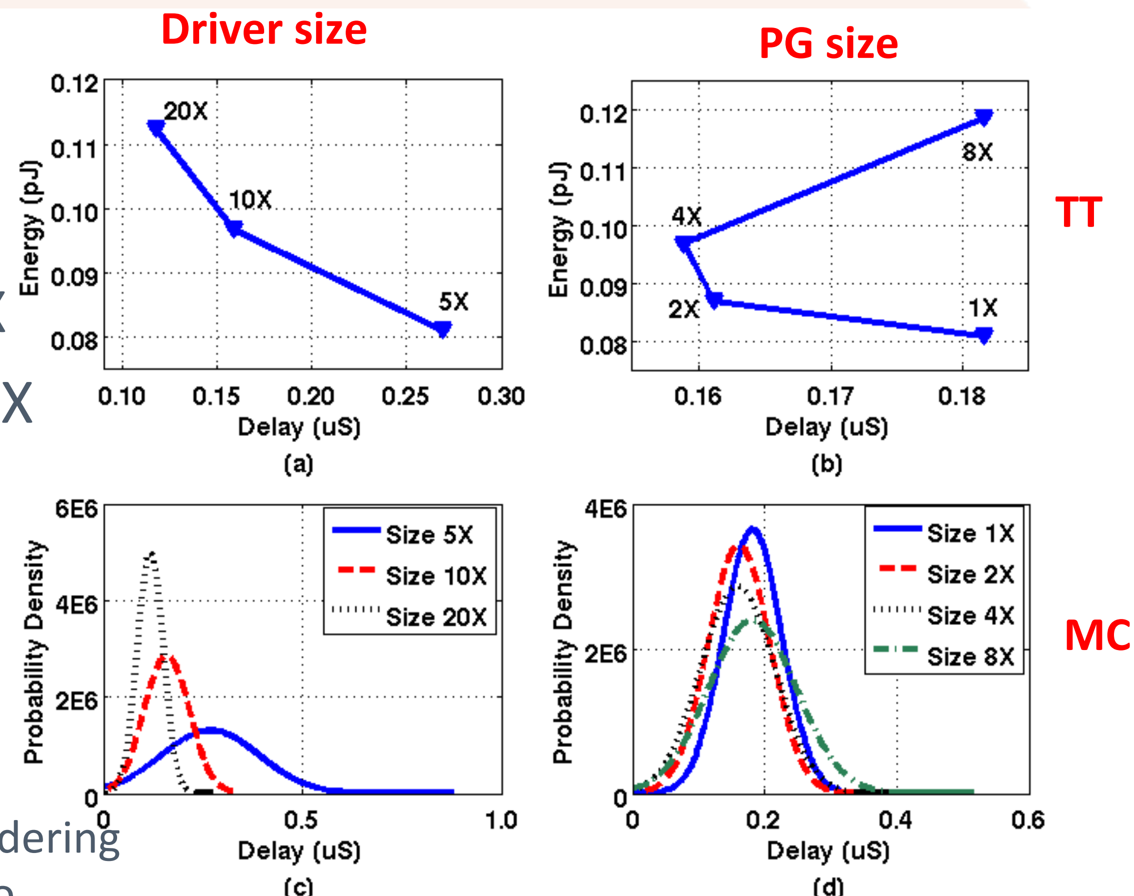
Optimization of subVt FPGA interconnect

- Optimization: Connection box (simulation)
  - @VDD=0.4V, VDDC=0.6V.
  - Connection box
    - Full mux
    - 1-stage
    - 2-stage
  - Decision
    - 2-stage
    - Best: energy & variation
    - Overhead: area(2.6X than full mux structure)



Optimization of subVt FPGA interconnect

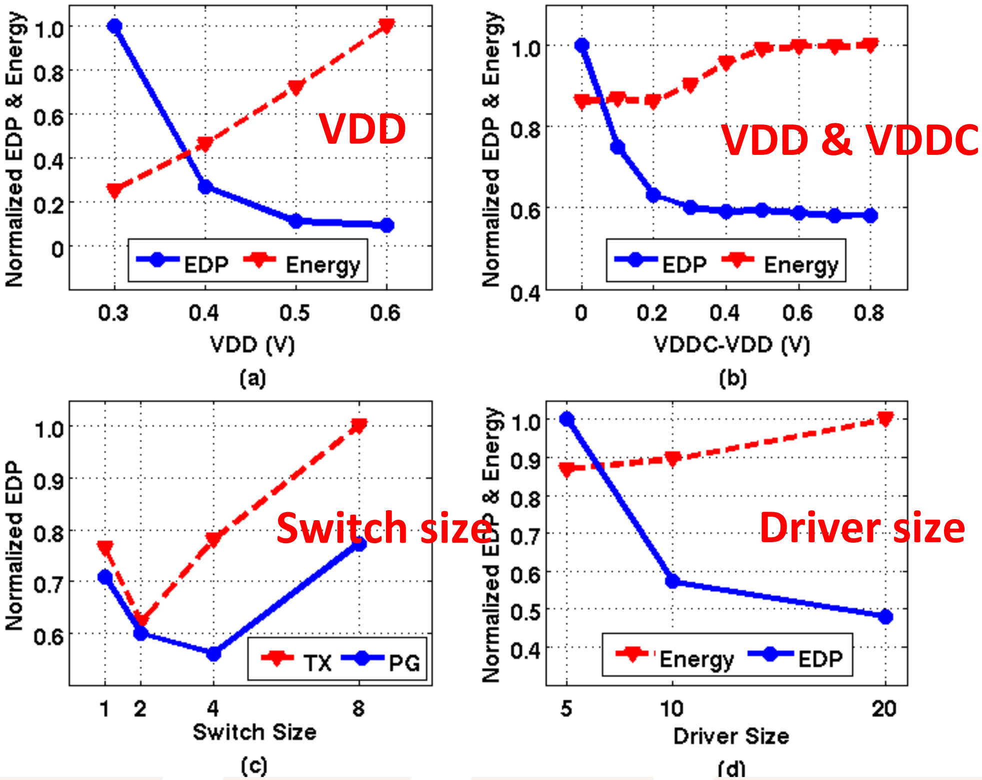
- Optimization: Driver, switch point (simulation)
  - @VDD=0.4V, VDDC=0.6V.
  - Driver size
    - 5X, 10X, 20X
    - Decision: 10X
  - Switch size
    - 1X,2X,4X,8X
    - Decision: 4X



* Decision is made considering measurement results too.

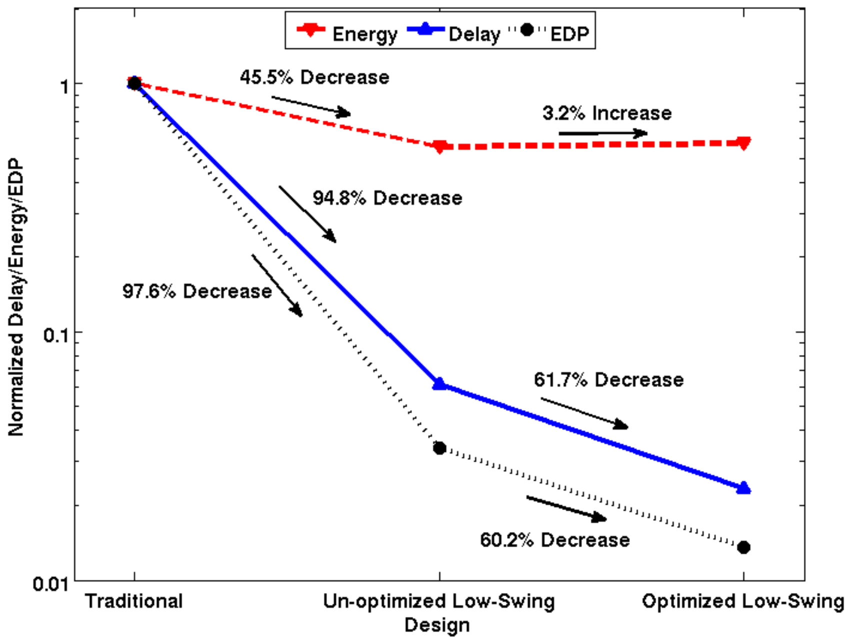
Optimization of subVt FPGA interconnect

- Optimization: Measurement of the chip
  - Dual-VDD scheme
    - VDD: 0.4V
    - VDDC: 0.6V
  - Switch point
    - Size: 4X
    - Topology: PG
  - Driver
    - Size: 10X



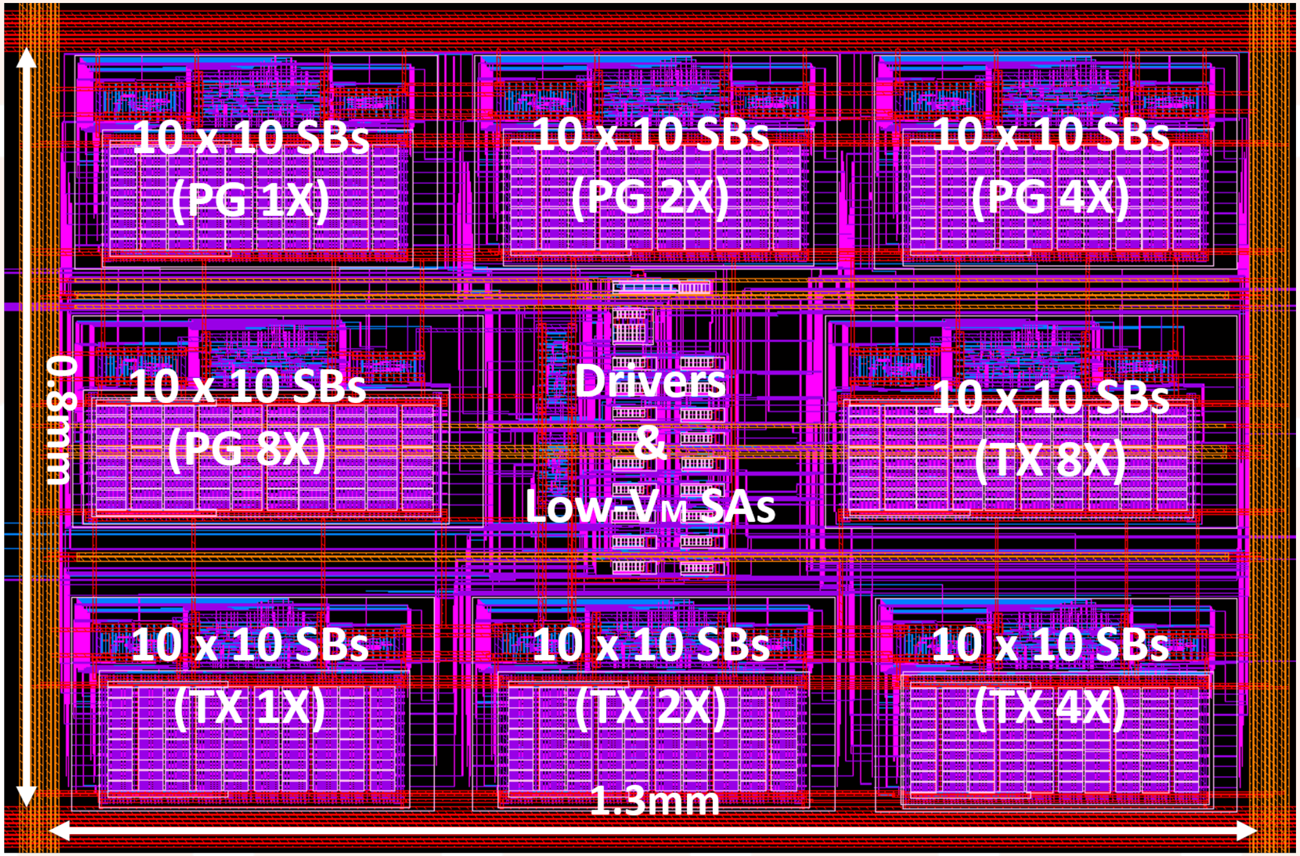
Optimization of subVt FPGA interconnect

- Comparison
  - Optimized, un-optimized, traditional(uni-directional)
  - Vs. traditional design:
    - 97.7% smaller delay
    - 42.7% smaller energy



Optimization of subVt FPGA interconnect

- Layout photo of the 130 nm CMOS chip



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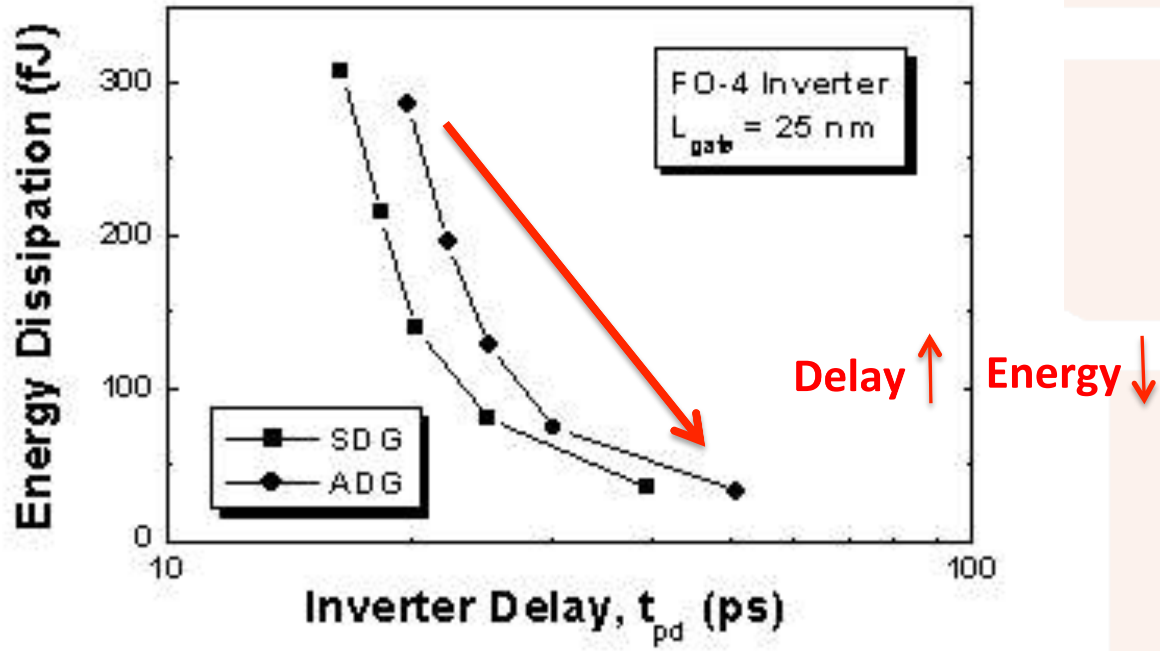
Further energy reduction of interconnect: voltage scaling

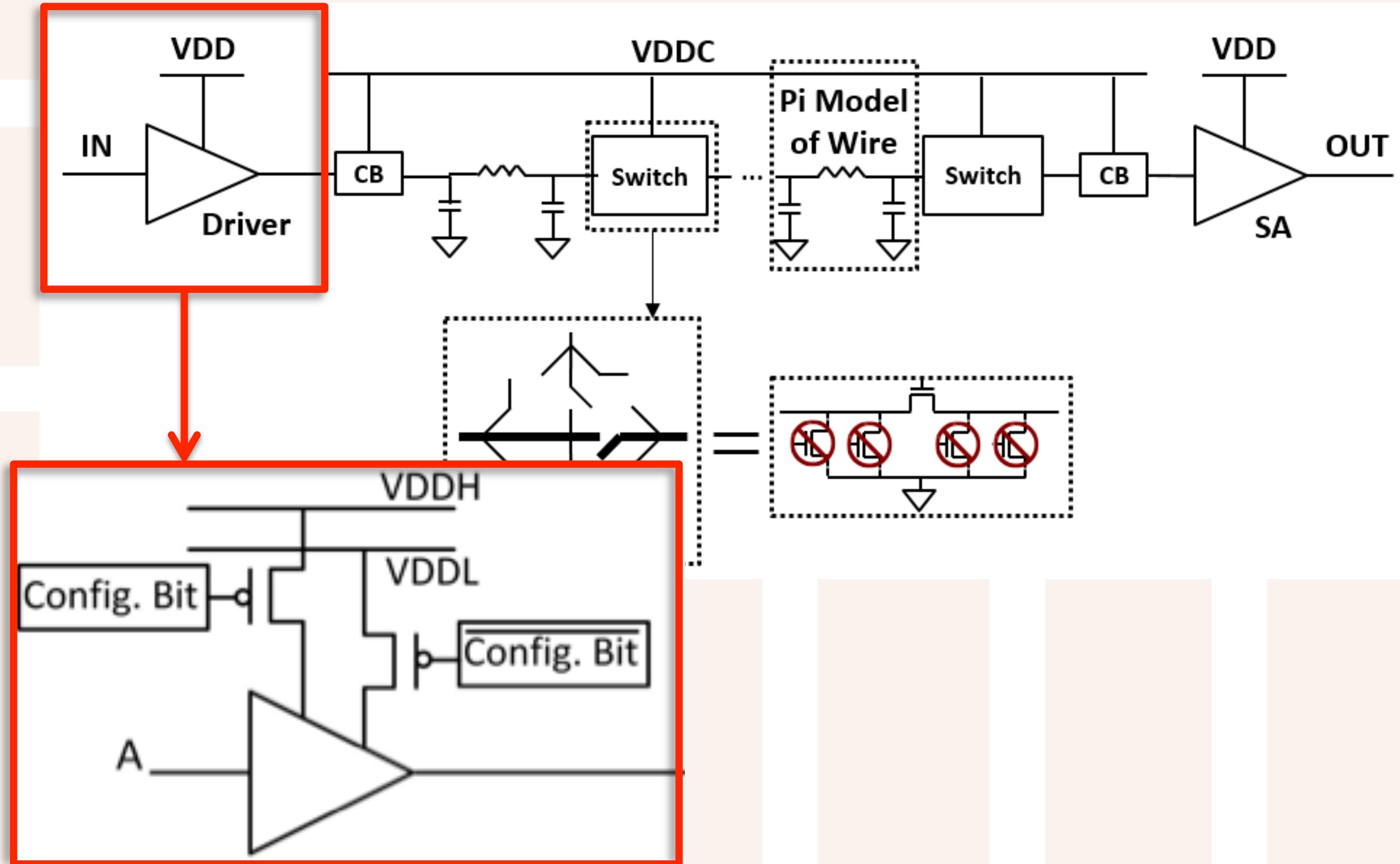
- Basic idea
  - Trade: delay & energy??



https://buffy.eecs.berkeley.edu/PHP/resabs/resabs.php?f_year=2004&f_submit=chapgrp&f_chapter=10

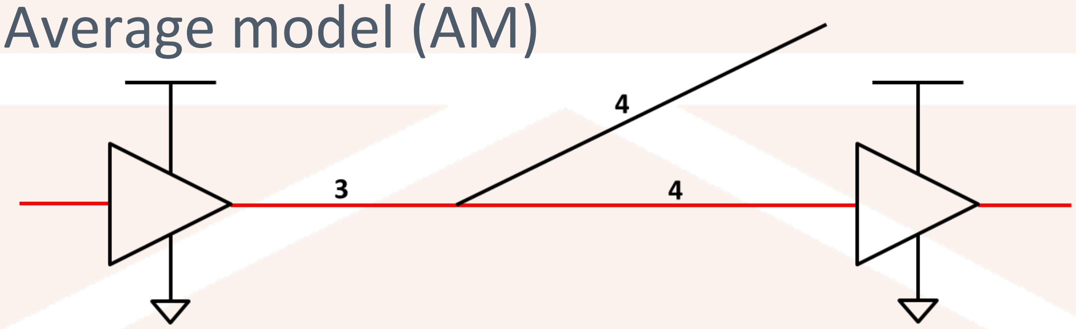
Further energy reduction of interconnect: voltage scaling

- Programmable header structure

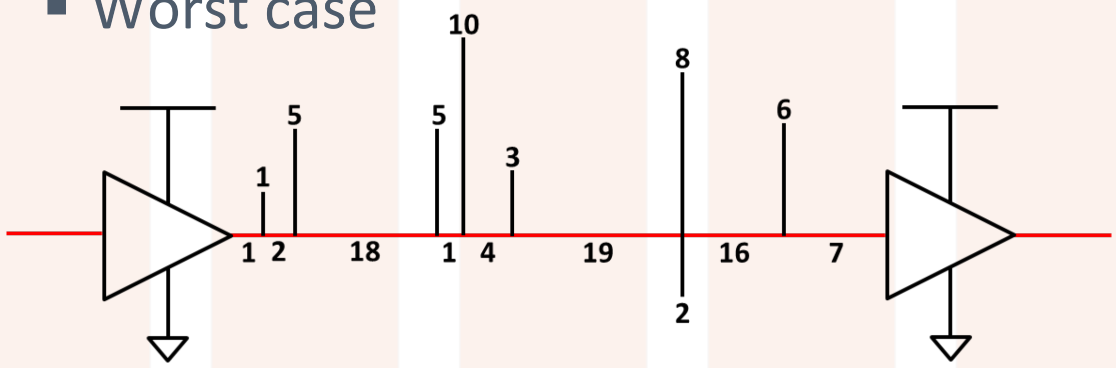


Further energy reduction of interconnect: voltage scaling

- Interconnect circuit models: based on MCNC benchmarks
  - Average model (AM)

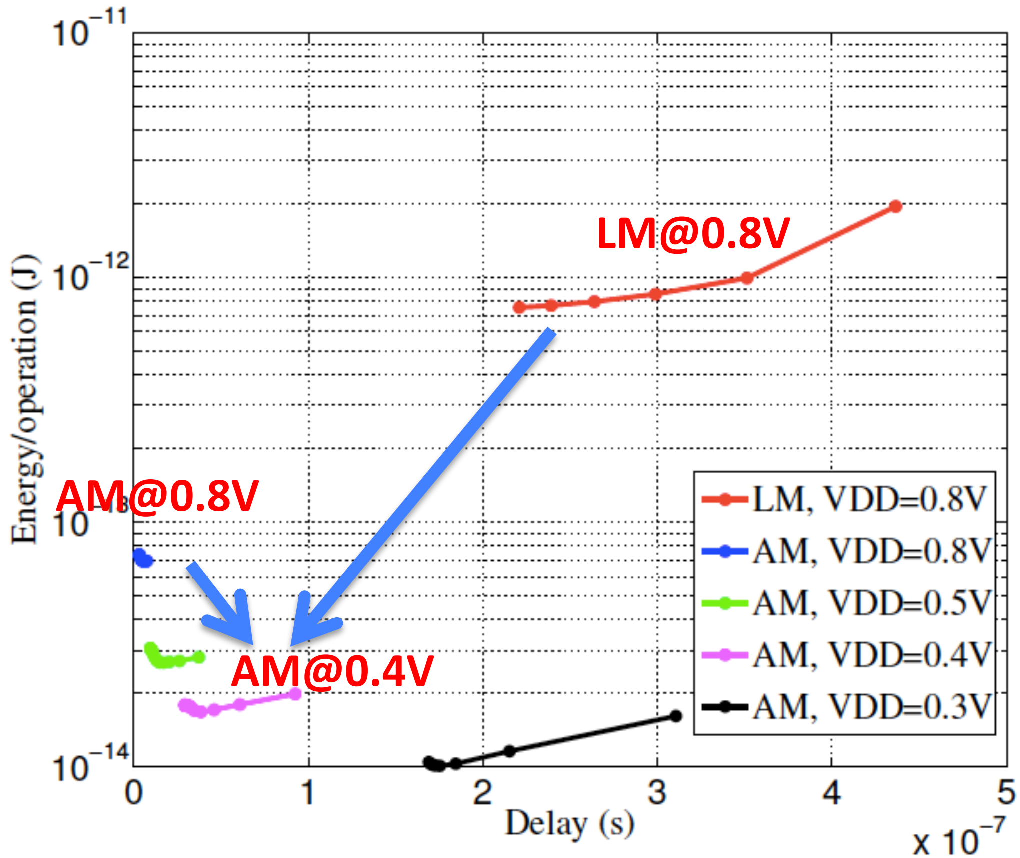


  - Long net model (LM)
    - Worst case



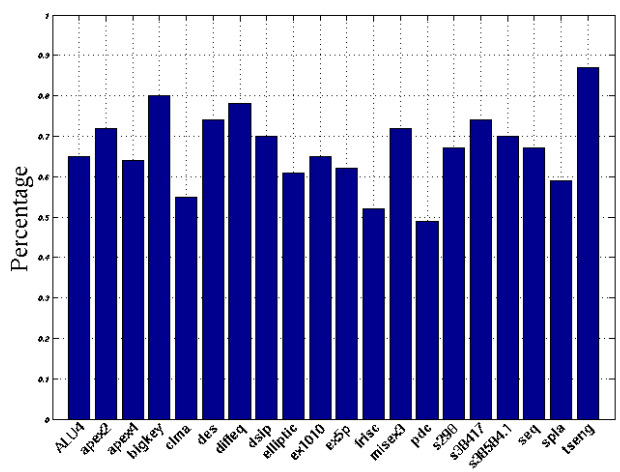
Further energy reduction of interconnect: voltage scaling

- Voltage scaling pre-exploration using AM and LM

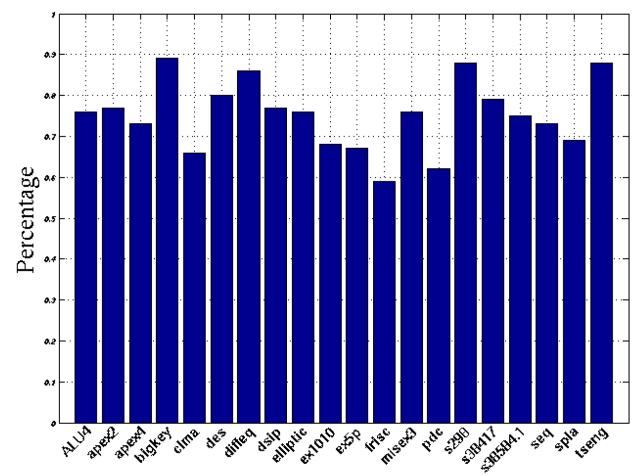


Further energy reduction of interconnect: voltage scaling

- Paths distribution of MCNC benchmarks compared with AM
  - Observations: similar distribution, short paths are the major part



Percentage of paths whose longest net is shorter than AM circuit in 20 MCNC benchmarks



Percentage of the paths whose switch count is less than AM circuit in 20 MCNC benchmarks

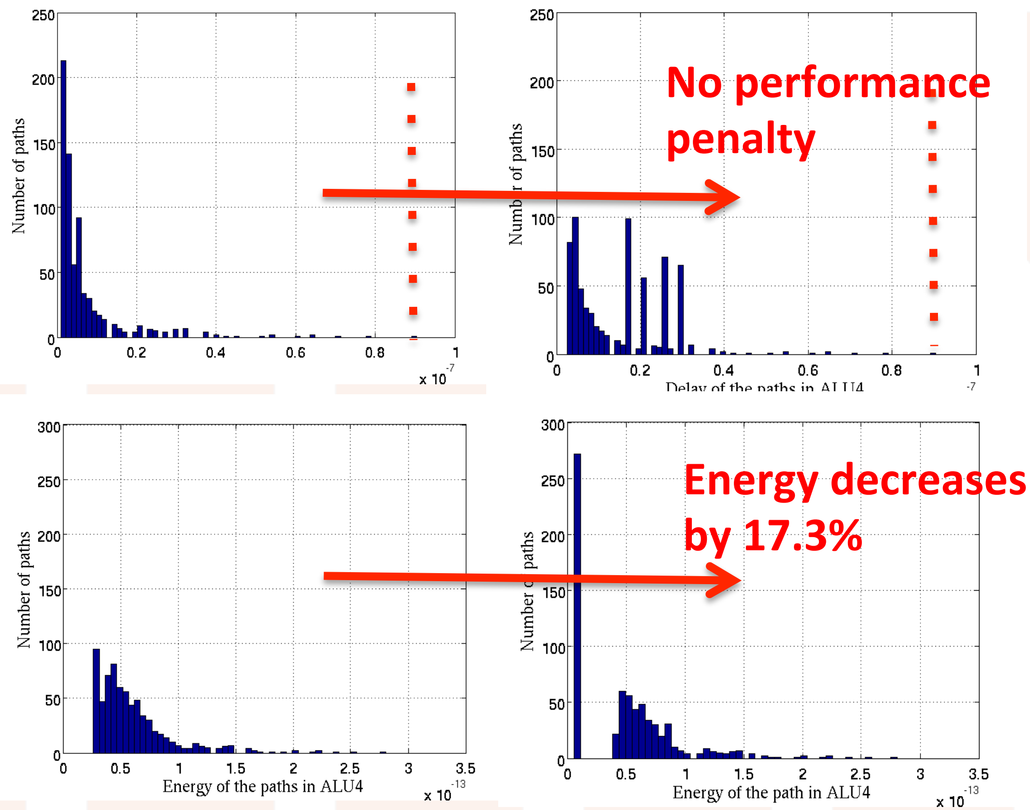
Further energy reduction of interconnect: voltage scaling

- Voltage scaling: a case study of ALU4
  - VDDH=0.8V, VDDL=0.4V
  - Applicable factor: 60%

No voltage scaling | Voltage scaling

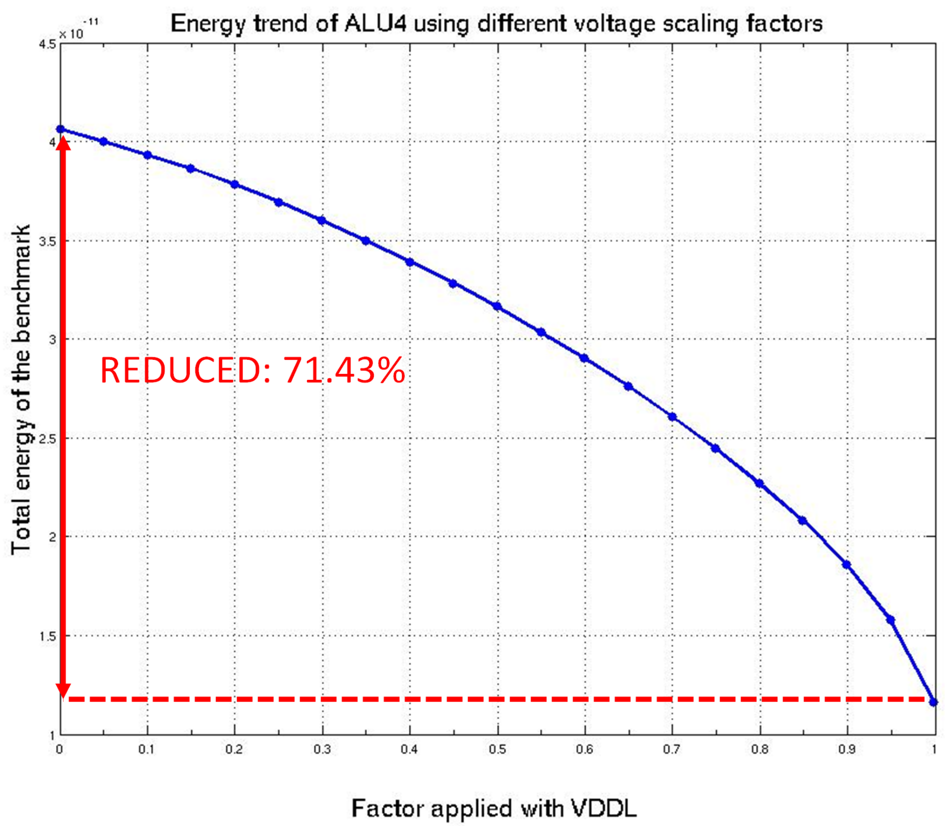
Delay distribution

Energy distribution



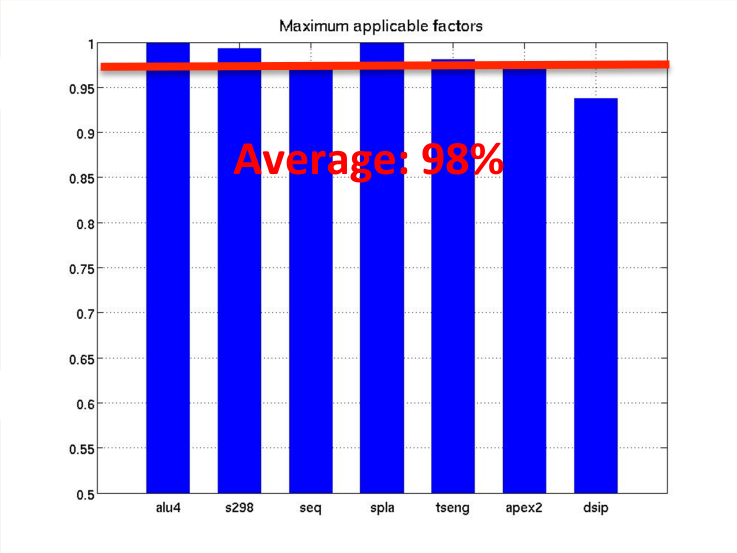
Further energy reduction of interconnect: voltage scaling

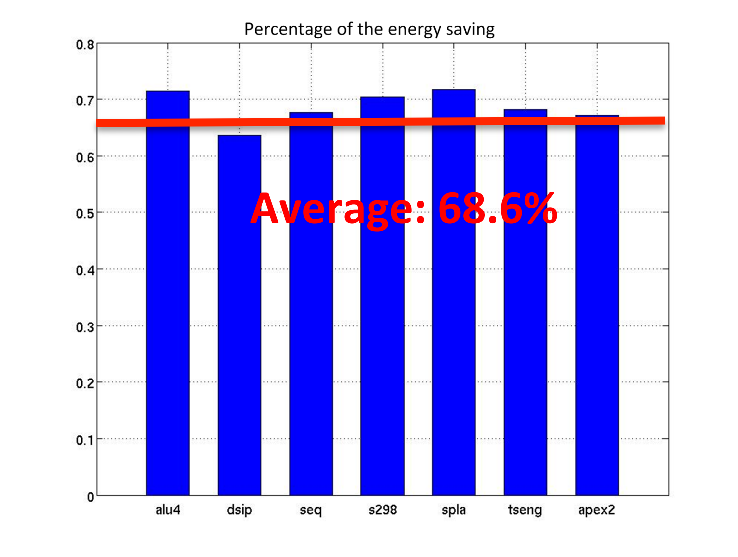
- Voltage scaling: a case study of ALU4
  - Applicable factor: sweeping from 0 to maximum (the max AF is 99% for ALU4)



Further energy reduction of interconnect: voltage scaling

- Voltage scaling:
  - For 7 representatives of MCNC benchmarks





Maximum applicable factors

Energy reduction with maximum applicable factors

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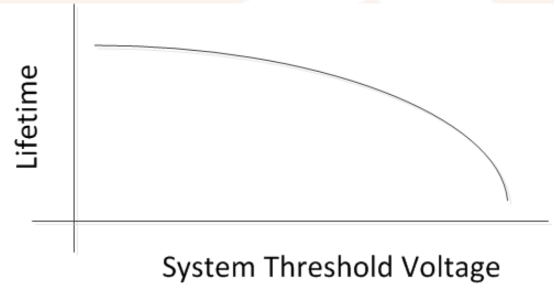
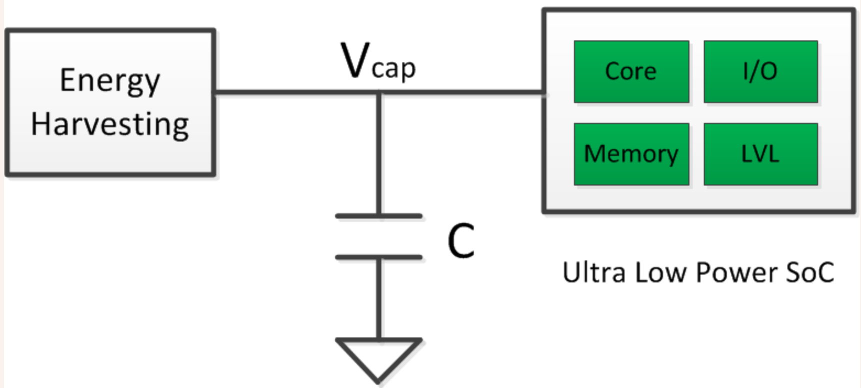
A single ended low-swing level converter design

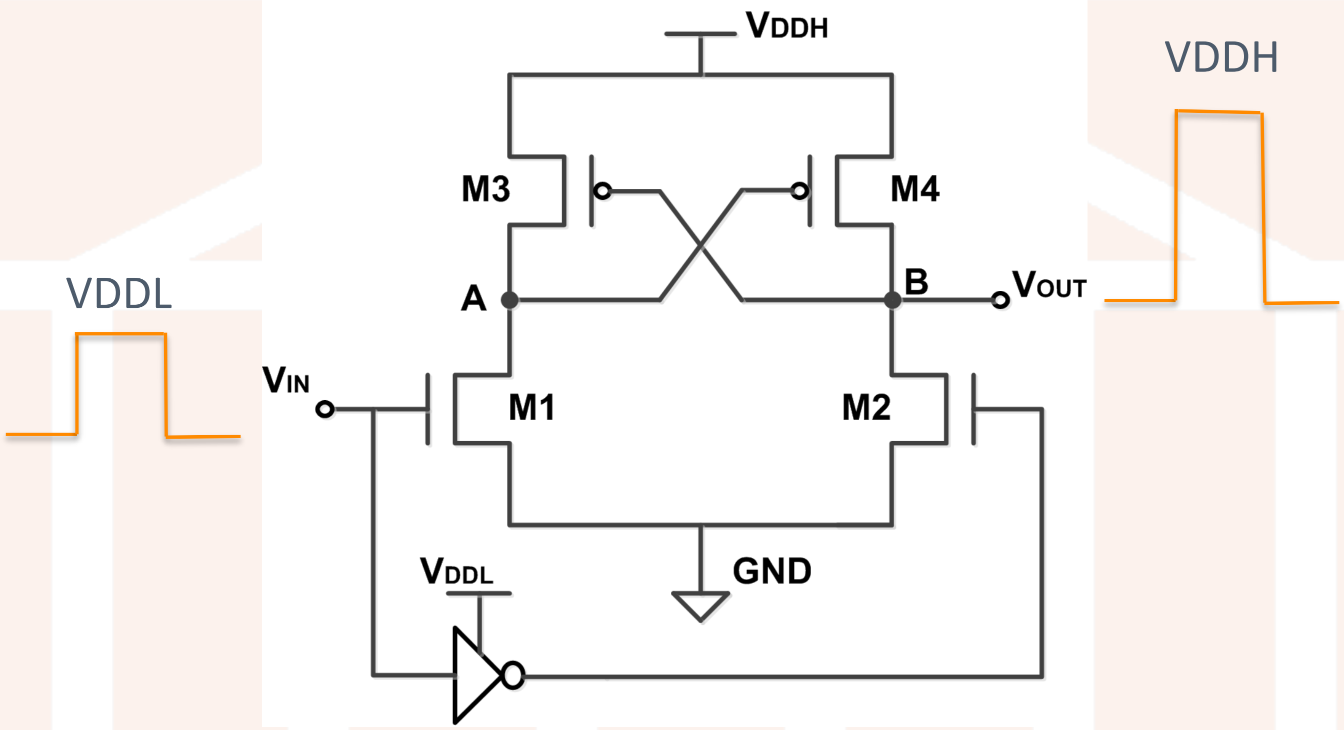
- Lowering system threshold voltage
- Increasing energy utilization of SoCs: energy harvesting system





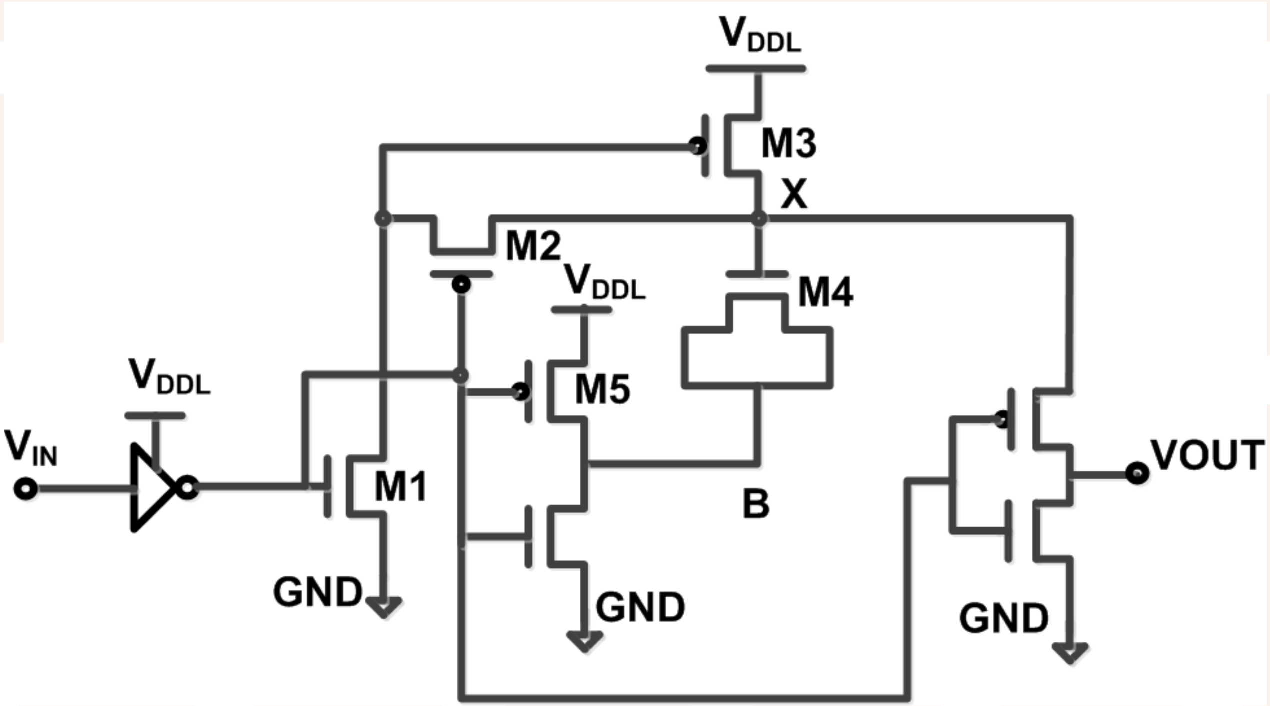
A single ended low-swing level converter design

- Traditional level converter
  - Switching ability: ~ 300mV – 400mV



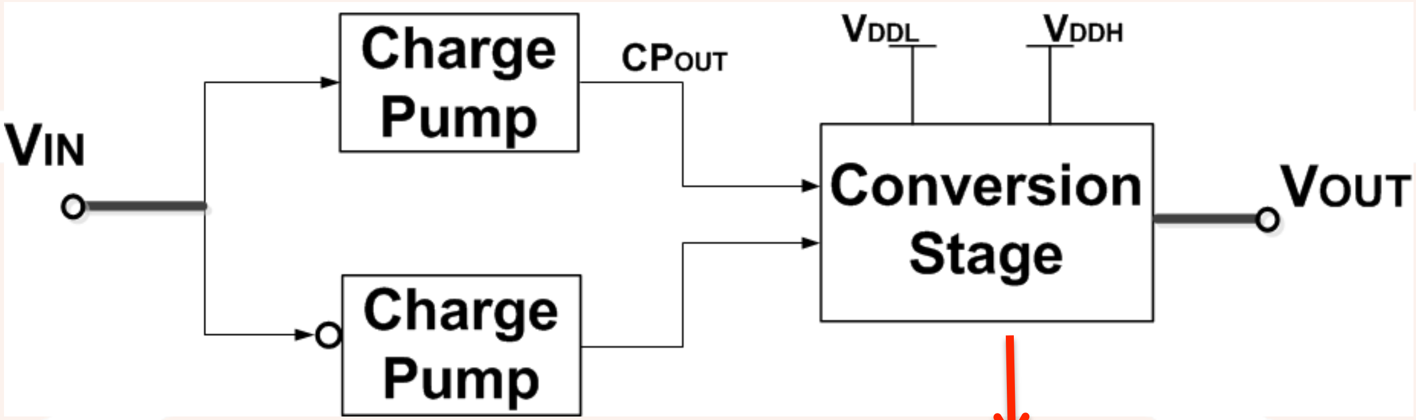
A single ended low-swing level converter design

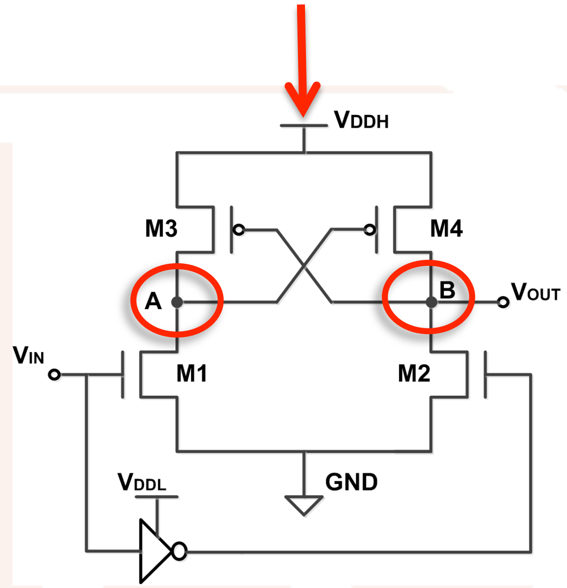
- Proposed design idea: using subthreshold 2X charge pump



A single ended low-swing level converter design

- Architecture of the proposed level converter

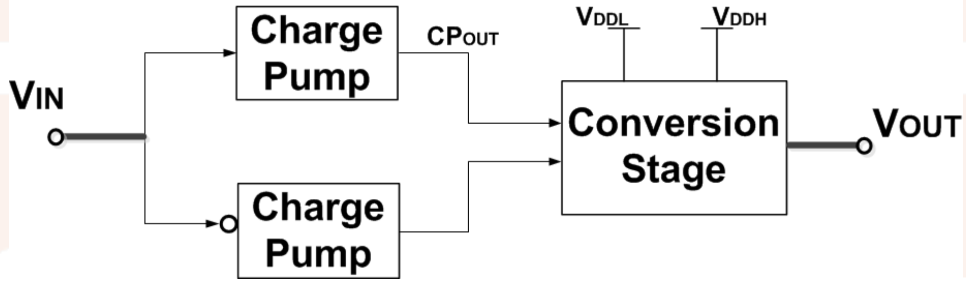


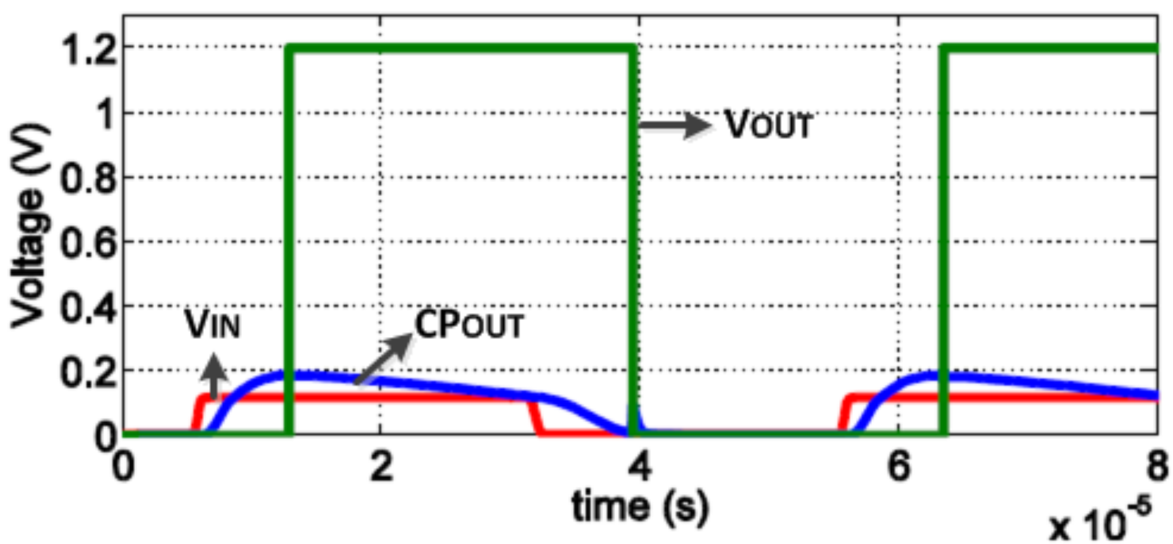


Can be any dual-input level converter design

A single ended low-swing level converter design

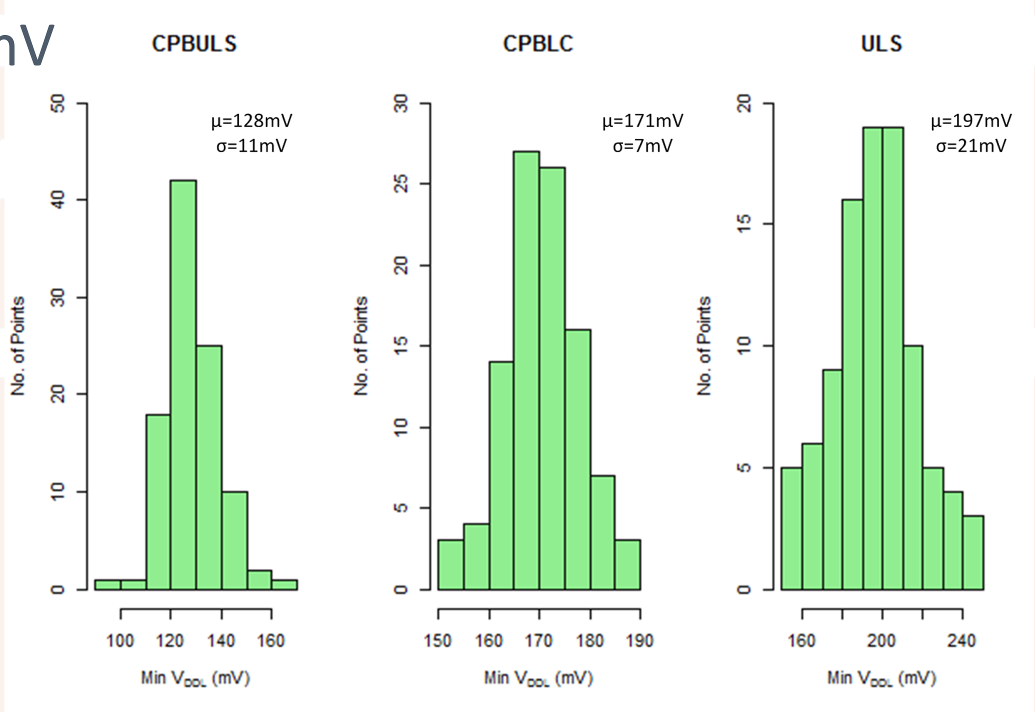
- Functional waveform of the proposed CPBULS (charge pump based ultra low swing) level converter





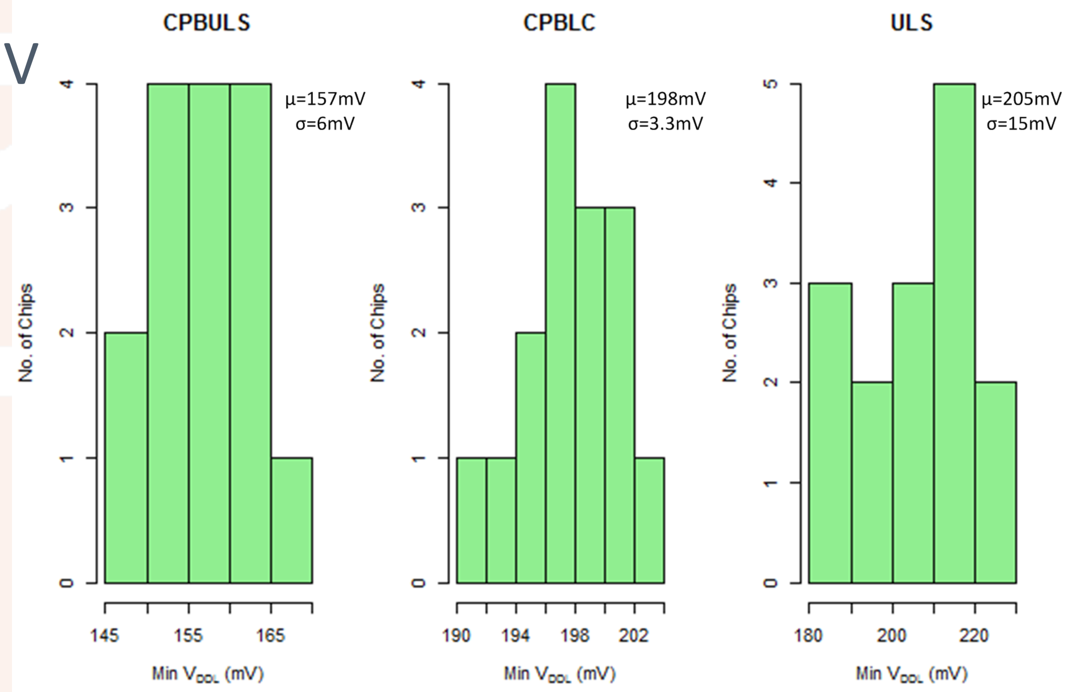
A single ended low-swing level converter design

- Simulation and measurement
  - Monte carlo simulations, iteration=100
  - CPBULS: 128mV
  - CPBLC: 171mV
  - ULS: 197mV



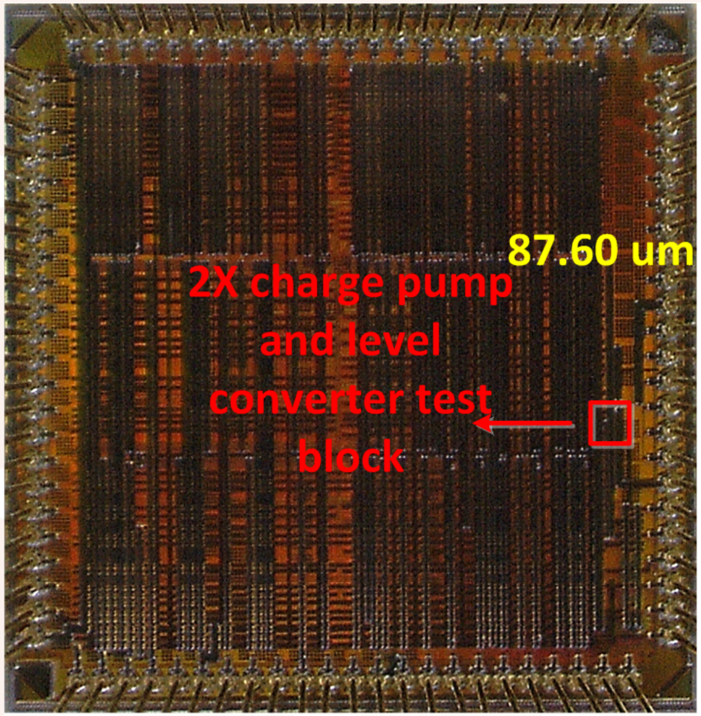
A single ended low-swing level converter design

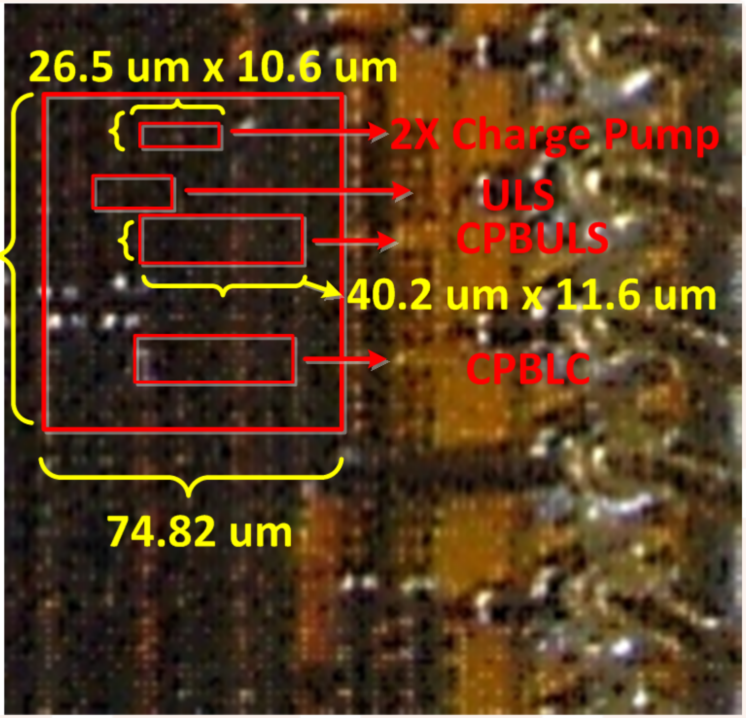
- Simulation and measurement
  - Measurement results: 130nm CMOS technology
  - CPBULS: 157mV
  - CPBLC: 198mV
  - ULS: 205mV



A single ended low-swing level converter design

- Die photo





A single ended low-swing level converter design

- Conclusion and comparison
  - Compared with [6]
    - 1.5X worse energy/conversion
    - 2X higher switching capability

Table 2: Comparison between prior work and the proposed work

	[31]	[23]	[10]	[6]	This Work
Minimum V_{DDL}	188mV	200mV	400mV	300mV	145mV
Energy/bit	-	10fJ	327fJ	850fJ	1.2pJ
Chip/Simulation	Chip	Simulation	Simulaton	Chip	Chip
Maximum Frequency	17.3MHz	10MHz	1MHz	8MHz	8kHz
Area(μm^2)	-	-	120.9	112000	466
Technology	130nm	90nm	180nm	130nm	130nm

∗ All the numbers in green squares are referenced work in the paper and thesis

Conclusion and contribution

- Optimized the subthreshold FPGA interconnect
  - Dual–VDD scheme
  - Switch box, connection box, driver
  - Signal degradation
  - Compared with the traditional design
    - 97.7% less delay
    - 42.7% less energy
- Voltage scaling technique to further reduce the energy consumption of FPGA interconnect
  - Programmable header structure
  - Explored the potentials of voltage scaling of the interconnect
    - 98% of the paths can be applied with lower driving voltage
    - 68.6% energy reduction without any performance penalty

Conclusion and contribution

- Ultra-low swing low power level converter design
  - Further extends system threshold voltage
    - Take more use of the energy in ultra-low power system: e.g. energy harvesting system
  - 145 mV switching ability from measurement results, potentially 99.6mV switching ability from simulation results

Publications

- **Yu Huang** , Aatmesh Shrivastava, Benton H. Calhoun. “A 145mV to 1.2V single ended level converter circuit for ultra-low power low voltage ICs.” In S3S Conference . ***Accepted***
- He Qi, Oluseyi Ayorinde, **Yu Huang** , Benton H. Calhoun. “Optimizing energy efficient low-swing interconnect for sub-threshold FPGAs.” In Field-programmable Logic and Applications (FPL) . ***Accepted***
- Oluseyi Ayorinde, He Qi, **Yu Huang** , Benton H. Calhoun. “Using island-style bi-directional intra-CLB routing in low-power FPGAs.” In Field-programmable Logic and Applications (FPL) . ***Accepted***

Acknowledgement

I would like to express my gratitude to my advisor, Professor Benton H. Calhoun for his useful comments, remarks, and engagement through the learning process of my Master's thesis.

I would also like to thank Professor Joanne Bechta Dugan and Professor Jack Stankovic for giving me useful suggestions .

Thank Aatmesh Shrivastava, He Qi, and Oluseyi Ayorinde, who willingly shared their precious time and given me their assistance throughout our collaboration.

And also, I want to thank everyone in the Robust Low Power VLSI group as well as my friends here in UVa who have helped me and spent so many happy times in work and life with me: Yousef Shaksheer, Yanqing Zhang, Kyle Craig, Peter Beshay, Ke Wang, Jiaqi Gong, James Boely, Alicia Klinefelter, Patricia Gonzalez, Arijit Banerjee, Divya Akella, Abhishek Roy, Chris Lukas, Farah Yahya, Hash Patel, Ningxi Liu, Manula Pathirana and Dilip Vasudevan.

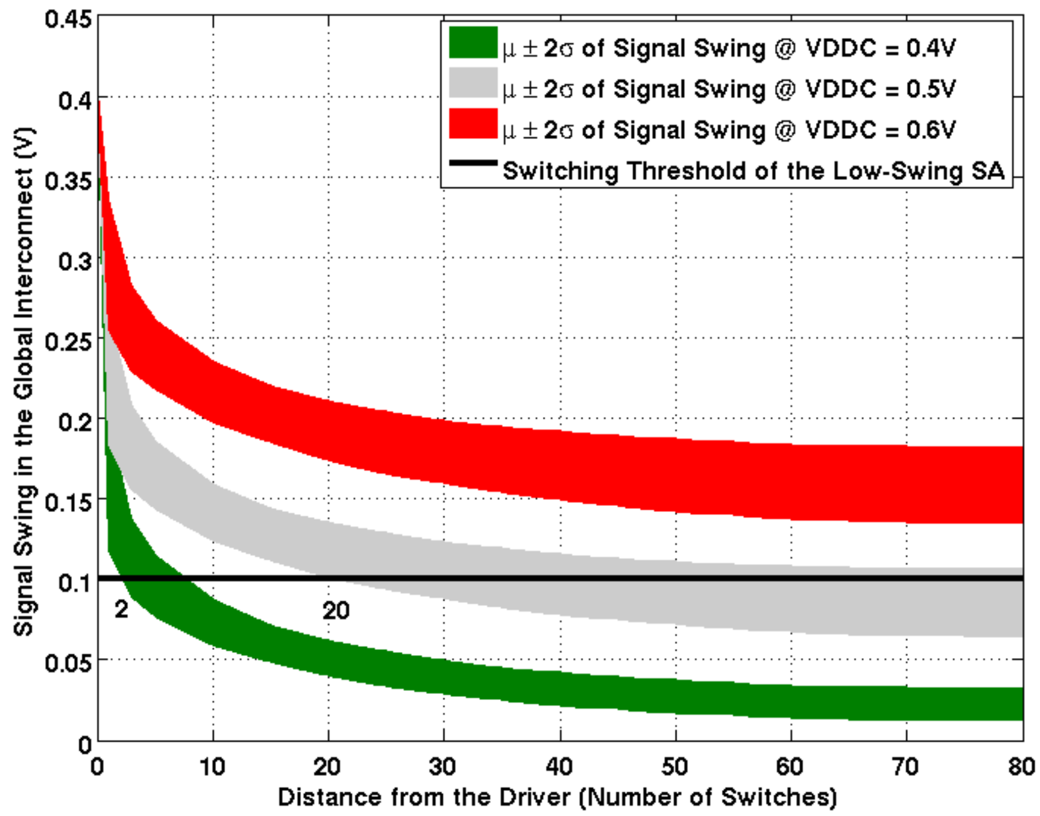
Thank all the people who care about me and encourage me.

Questions?

Thank you.

Optimization of subVt FPGA interconnect

- Signal degradation



Further energy reduction of interconnect: voltage scaling

- Path information of MCNC benchmarks

Benchmark	Total Switch #	Length of Longest Path	Average Switch#	Average Path Length
alu4	8,078	41	11.61	7.06
apex2	11,459	24	11.84	5.98
apex4	8,039	24	11.52	6.53
bigkey	6,191	19	6.05	4.48
clma	68,031	53	14.13	8.87
des	8,327	27	8.36	5.85
diffeq	6,734	34	7.15	5.14
dsip	5,944	19	8.61	5.92
elliptic	21,405	44	11.23	7.37
ex5p	7,313	25	10.95	6.68
ex1010	32,109	50	12.49	6.80
frisc	26,985	54	15.45	9.12
misex	7,624	21	10.66	5.87
pdc	41,282	39	18.02	9.14
s298	7,075	25	9.81	6.06
s38417	29,246	62	8.20	5.77
s38584.1	31,219	68	8.58	6.22
seq	10,867	25	12.38	6.53
spla	27,362	42	15.14	7.73
tseng	3,667	22	6.25	4.36
Average	N/A	N/A	11	7
Largest	N/A	68	N/A	N/A

Further energy reduction of interconnect: voltage scaling

- Header size exploration
  - 20X: the balance of energy, delay, area