## **Bibliography**

- Mark Aagaard, Robert Jones, and Carl-Johan Seger. Formal verification using parametric representations of Boolean constraints. In *DAC, Proceedings of Design Automation Conference*, pages 402–407, June 1999.
- [2] Aharon Aharon, Dave Goodman, Moshe Levinger, Yossi Lichtenstein, Yossi Malka, Charlotte Metzger, Moshe Molcho, and Gil Shurek. Test program generation for functional verification of PowerPc processors in IBM. In DAC, Proceedings of Design Automation Conference, pages 279–285, June 1995.
- [3] Robert L. Ashenhurst. The decomposition of switching functions. In *Proceedings of the International Symposium on the Theory of Switching*, Part I 29, pages 74–116, 1957.
- [4] Zeev Barzilai, J. Lawrence Carter, Barry K. Rosen, and Joseph D. Rutledge. HSS a highspeed simulator. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 601–617, July 1987.
- [5] Janick Bergeron. Writing Testbenches: Functional Verification of HDL Models. Kluwer Academic Publishers, 2nd edition, 2003.
- [6] Jules Bergmann and Mark Horowitz. Improving coverage analysis and test generation for large designs. In ICCAD, Proceedings of the International Conference on Computer Aided Design, pages 580–583, November 1999.

- [7] Valeria Bertacco and Maurizio Damiani. Boolean function representation based on disjointsupport decompositions. In *ICCD*, *Proceedings of the International Conference on Computer Design*, pages 27–33, October 1996.
- [8] Valeria Bertacco and Maurizio Damiani. Boolean function representation using parallel-access diagrams. In *Proceedings of the Sixth Great Lakes Symposium on VLSI*, March 1996.
- [9] Valeria Bertacco and Maurizio Damiani. The disjunctive decomposition of logic functions. In ICCAD, Proceedings of the International Conference on Computer Aided Design, pages 78–82, November 1997.
- [10] Valeria Bertacco, Maurizio Damiani, and Stefano Quer. Cycle-based symbolic simulation of gate-level synchronous circuits. In DAC, Proceedings of Design Automation Conference, pages 391–396, June 1999.
- [11] Valeria Bertacco and Kunle Olukotun. Efficient state representation for symbolic simulation. In DAC, Proceedings of Design Automation Conference, June 2002.
- [12] Beate Bollig, Martin Löbbing, and Ingo Wegener. Simulated annealing to improve variable orderings for OBDDs. In *International Workshop on Logic Synthesis*, pages 5.1–5.10, May 1995.
- [13] Karl Brace, Richard Rudell, and Randal E. Bryant. Efficient implementation of a BDD package. In *DAC, Proceedings of Design Automation Conference*, pages 40–45, 1990.
- [14] Robert K. Brayton and Curt McMullen. The decomposition and factorization of boolean expressions. In ISCAS, Proceedings of the International Symposyium on Circuits and Systems, pages 49–54, 1982.
- [15] Robert K. Brayton, Richard Rudell, Alberto Sangiovanni-Vincentelli, and Albert R. Wang. MIS: A multiple-level logic optimization system. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 6(6):1062–1081, November 1987.

- [16] Franc Brglez, David Bryan, and Krzysztof Koźmiński. Combinational profiles of sequential benchmark circuits. In ISCAS, Proceedings of the International Symposyium on Circuits and Systems, pages 1929–1934, May 1989.
- [17] Randal E. Bryant. Graph-based algorithms for boolean function manipulation. *IEEE Transactions on Computers*, 35(8):677–691, August 1986.
- [18] Randal E. Bryant. On the complexity of vlsi implementations and graph representations of boolean functions with application to integer multiplication. *IEEE Transactions on Computers*, 40:205–213, 1991.
- [19] Randal E. Bryant. Symbolic boolean manipulation with ordered binary-decision diagrams. ACM Computing Surveys, 24(3):293–318, September 1992.
- [20] Randal E. Bryant, Derek Beatty, Karl Brace, Kyeongsoon Cho, and Thomas Sheffler. COS-MOS: A compiled simulator for MOS circuits. In DAC, Proceedings of Design Automation Conference, pages 9–16, June 1987.
- [21] Jerry R. Burch, Edward M. Clarke, David E. Long, Ken L. MacMillan, and David L. Dill. Symbolic model checking for sequential circuit verification. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 13(4):401–424, 1994.
- [22] Jerry R. Burch and David E. Long. Efficient boolean function matching. In ICCAD, Proceedings of the International Conference on Computer Aided Design, pages 408–411, November 1992.
- [23] Gianpiero Cabodi, Paolo Camurati, Luciano Lavagno, and Stefano Quer. Disjunctive partitioning and partial iterative squaring: an effective approach for symbolic traversal of large circuits. In DAC, Proceedings of Design Automation Conference, pages 728–733, June 1997.

- [24] Gianpiero Cabodi, Paolo Camurati, and Stefano Quer. Improved reachability analysis of large finite state machine. In ICCAD, Proceedings of the International Conference on Computer Aided Design, pages 354–360, November 1996.
- [25] Srihari Cadambi, Chandra S. Mulpuri, and Pranav N. Ashar. A fast, inexpensive and scalable hardware acceleration technique for functional simulation. In DAC, Proceedings of Design Automation Conference, pages 570–575, June 2002.
- [26] A. Chandra, V. Iyengar, D. Jameson, R. Jawalekar, I. Nair, B. Rosen, M. Mullen, J. Yoon,
  R. Armoni, D. Geist, and Y. Wolfsthal. AVPGEN a test generator for architecture verification.
  *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 3(2):188–200, June 1995.
- [27] Olivier Coudert, Christian Berthet, and Jean Christophe Madre. Verification of synchronous sequential machines based on symbolic execution. In *Automatic Verification Methods for Finite State Systems, International Workshop*, volume 407 of *Lecture Notes in Computer Science*, pages 365–3. Springer, June 1989.
- [28] Olivier Coudert and Jean Christophe Madre. Implicit and incremental computation of primes and essential primes of Boolean functions. In DAC, Proceedings of Design Automation Conference, pages 36–39, June 1992.
- [29] CUDD-2.3.1. http://vlsi.Colorado.edu/fabio.
- [30] Herbert A. Curtis. A New Approach to the Design of Switching Circuits. Van Nostrand, Princeton, N.J., 1962.
- [31] Charles J. DeVane. Efficient circuit partitioning to extend cycle simulation beyond synchronous circuits. In *ICCAD*, *Proceedings of the International Conference on Computer Aided Design*, pages 154–161, nov 1997.

- [32] Masahiro Fujita, Hisanori Fujisawa, and Nobuaki Kawato. Evaluation and improvements of boolean comparison method based on binary decision diagrams. In *ICCAD*, *Proceedings of the International Conference on Computer Aided Design*, pages 2–5, November 1988.
- [33] Craig Hansen. Hardware logic simulation by compilation. In DAC, Proceedings of Design Automation Conference, pages 712–716, June 1988.
- [34] Faisal I. Haque, Khizar A. Khan, and Jonathan Michelson. *The Art of Verification with Vera*. Verification Central, 2001.
- [35] Scott Hauck. *Multi-FPGA Systems*. PhD thesis, University of Washington, Dept. of Computer Science and Engineering, 1995.
- [36] Pei-Hsin Ho, Thomas Shiple, Kevin Harer, James Kukula, Robert Damiano, Valeria Bertacco, Jerry Taylor, and Jiang Long. Smart simulation using collaborative formal and simulation engines. In *ICCAD*, *Proceedings of the International Conference on Computer Aided Design*, pages 120–126, November 2000.
- [37] Yoav Hollander, Matthew Morley, and Amos Noy. The *e* language: A fresh separation of concerns. In *Technology of Object-Oriented Languages and Systems*, volume TOOLS-38, pages 41–50, March 2001.
- [38] Alan J. Hu and David L. Dill. Reducing BDD size by exploiting functional dependencies. In DAC, Proceedings of Design Automation Conference, pages 266–271, June 1993.
- [39] Gérard Huet. Higher order unification 30 years later. In *Theorem Proving in Higher Order Logics*, volume 2410 of *Lecture Notes in Computer Science*, pages 3–12. Springer-Verlag, August 2002.
- [40] Prabhat Jain and Ganesh Gopalakrishnan. Hierarchical constraint solving in the parametric form with applications to efficient symbolic simulation based verification. In *ICCD*, *Proceedings of the International Conference on Computer Design*, pages 304–307, October 1993.

- [41] Prabhat Jain and Ganesh Gopalakrishnan. Efficient symbolic simulation-based verification using the parametric form of boolean expressions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 13:1005–1015, August 1994.
- [42] Steven Johnson. View from the fringe of the fringe. In CHARME, volume 2144 of Lecture Notes in Computer Science, pages 1–12. Springer-Verlag, September 2001.
- [43] Michael Kantrowitz and Lisa M. Noack. I'm done simulating; now what? verification coverage analysis and correctness checking of the DECchip 21164 Alpha microprocessor. In DAC, Proceedings of Design Automation Conference, pages 325–330, June 1996.
- [44] Richard M. Karp. Functional decomposition and switching circuit design. Journal of the Society for Industrial and Applied Mathematics, 11(2):291–335, 1963.
- [45] Kevin Karplus. Representing boolean functions with if-then-else dags. Technical Report UCSC-CRL-88-28, Baskin Center for Computer Engineering & Information Sciences, 1988.
- [46] Kevin Karplus. Using if-then-else dags for multi-level logic minimization. In Proceedings of Advanced Research in VLSI, pages 101–118, 1989.
- [47] Kevin Karplus. Using if-then-else dags to do technology mapping for field-programmable gate arrays. Technical Report UCSC-CRL-90-43, Baskin Center for Computer Engineering & Information Sciences, 1990.
- [48] James C. King. Symbolic execution and program testing. Communications of the ACM, 19(7):385–394, July 1976.
- [49] Tommy Kuhn, Tobias Oppold, Markus Winterholer, Wolfgang Rosenstiel, Marc Edwards, and Yaron Kashai. A framework for object oriented hardware specification, verification and synthesis. In DAC, Proceedings of Design Automation Conference, pages 413–418, June 2001.
- [50] Oded Lachish, Eitan Marcus, Shmuel Ur, and Avi Ziv. Hole analysis for functional coverage data. In DAC, Proceedings of Design Automation Conference, pages 807–812, June 2002.

- [51] Frédéric Mailhot and Giovanni DeMicheli. Algorithms for technology mapping based on binary decision diagrams and on boolean operations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 12:599–620, May 1993.
- [52] Sharad Malik, Albert Wang, Robert K. Brayton, and Alberto Sangiovanni-Vincentelli. Logic verification using binary decision diagrams in a logic synthesis environment. In *ICCAD*, *Proceedings of the International Conference on Computer Aided Design*, pages 6–9, November 1988.
- [53] Patrick C. McGeer, Jagesh V. Sanghavi, Robert K. Brayton, and Alberto Sangiovanni-Vincentelli. ESPRESSO-SIGNATURE: A new exact minimizer for logic functions. In DAC, Proceedings of Design Automation Conference, pages 618–624, June 1993.
- [54] In-Ho Moon, James Kukula, Kavita Ravi, and Fabio Somenzi. To split or to conjoin: The question in image computation. In DAC, Proceedings of Design Automation Conference, pages 23–28, June 2000.
- [55] Rajeev Murgai, Yoshihito Nishizaki, Narendra V. Shenoy, Robert K. Brayton, and Alberto Sangiovanni-Vincentelli. Logic synthesis for programmable gate arrays. In DAC, Proceedings of Design Automation Conference, pages 620–625, June 1990.
- [56] Gregory F. Pfister. The yorktown simulation engine: Introduction. In DAC, Proceedings of Design Automation Conference, pages 51–54, January 1982.
- [57] Kavita Ravi and Fabio Somenzi. High density reachability analysis. In *ICCAD*, *Proceedings* of the International Conference on Computer Aided Design, pages 154–158, November 1995.
- [58] Richard Rudell. Dynamic variable ordering for ordered binary decision diagrams. In IC-CAD, Proceedings of the International Conference on Computer Aided Design, pages 42–47, November 1993.

- [59] Tsutomu Sasao. Totally undecomposable functions: Applications to efficient multiple-valued decompositions. In *ISMVL*, pages 59–65, 1999.
- [60] Tsutomu Sasao and Munehiro Matsuura. DECOMPOS: An integrated system for functional decomposition. In *International Workshop on Logic Synthesis*, pages 471–477, 1998.
- [61] Claude E. Shannon. The synthesis of two-terminal switching circuits. *Bell Systems Technical Journal*, 28(1):59–98, 1949.
- [62] V. Yun-Shen Shen, Archie C. McKellar, and Peter Weiner. A fast algorithm for the disjunctive decomposition of switching functions. *IEEE Transactions on Computers*, C-20(3):304–309, 1971.
- [63] Theodore Singer. The decomposition chart as a theoretical aid. Technical Report BL-4, Sec.III, Harvard Computational Laboratory, 1953.
- [64] Hervé Touati, Hamid Savoj, Bill Lin, Robert K. Brayton, and Alberto L. Sangiovanni-Vincentelli. Implicit state enumeration of finite state machines using BDDs. In *ICCAD*, Proceedings of the International Conference on Computer Aided Design, pages 130–133, November 1990.
- [65] C. A. J. van Eijk and Jochen A. G. Jess. Exploiting functional dependencies in finite state machine verification. In *ED&TC*, *Proceedings of the European Design and Test Conference*, pages 9–14, March 1996.
- [66] Laung-Terng Wang, Nathan E. Hoover, Edwin H. Porter, and John J. Zasio. SSIM: A software levelized compiled-code simulator. In DAC, Proceedings of Design Automation Conference, pages 2–8, June 1987.
- [67] Chris Wilson and David L. Dill. Reliable verification using symbolic simulation with scalar values. In *DAC*, *Proceedings of Design Automation Conference*, pages 124–129, June 2000.

- [68] Saeyang Yang. Logic synthesis and optimization benchmarks user guide, version 3.0. Technical report, Microelectronics Center of North Carolina, January 1991.
- [69] Jun Yuan, Kurt Schultz, Carl Pixley, Hiller Miller, and Adnan Aziz. Modeling design constraints and biasing using bdds in simulation. In ICCAD, Proceedings of the International Conference on Computer Aided Design, pages 584–590, November 1999.