the nanoscale wires that the new chips would need. In addition, she said, they want to improve yields and performance, as well as use DNA to separate and eliminate nanotubes that don't conduct electricity.

Moreover, scientists must improve the basic chip-making process to ensure that the nanotubes adhere to the DNA properly and in the correct orientation.

The technique may need 10 to 20 years of work before it can be used commercially, said Wallraff.

# Researchers Use Software to Find Chip Flaws

Scientists have developed software that identifies problems in chips and recommends the best way to fix them. Developed at the University of Michigan, the software would help manufacturers cope with the growing number of bugs that take an increasing amount of time to fix as chips become more complex.

Processors now house a large number of transistors and perform a growing number of functions. This leads to more bugs and makes it difficult and time-consuming to identify them before vendors ship the chips, explained University of Michigan assistant professor Valeria Bertacco, who is working on the bug-finding software.

"As the complexity increases, so does the number of lines of code, which causes an explosion of bugs," said Gary Smith, chief analyst at the Gary Smith EDA consultancy.

This can delay the commercial release of chips and increase costs for manufacturers. Problems that occur after a processor ships can be particularly time-consuming and expensive to fix, Bertacco noted. Currently, though, fully debugging prototype chips can take up to a year, she said.

Because this would affect their budgets and market-related deadlines, chip makers usually fix only as many bugs as they can within a few months and then either ship their processors or cancel the project, according to Smith.

Manufacturers debug chips both before and after they are made, generally by designing and manufacturing special test boards and applying electric currents via the pins or internal nodes. Because of the analysis required to isolate and correct problems within the complex circuitry, the process relies on expensive logic analyzers to observe the internals.

The University of Michigan's FogClear software, run on an engineering workstation, could shorten the debugging process and reduce the number of prototypes and testing cycles vendors must conduct. It perhaps could even increase chips' reliability.

According to Bertacco, at any point in the chip-design flow, the software can examine two types of design-related errors: functional and electrical.

"A functional error is a bug in which the logic used to implement the design is incorrect in one or more circuit blocks," he explained. "An electrical error is one in which the circuit is functional but fails at the clock speed, voltage, and temperature intended for correct operation, typically because it doesn't finish evaluating within a clock cycle." Electrical errors tend to get worse as circuitry shrinks in size and performance demands grow.

The University of Michigan software uses mathematical techniques to examine the differences between the correct design and the actual circuit and find the precise location of bugs, said Bertacco. "Thus, the designer does not have to spend the effort required to wade through thousands of electrical inputs and millions of transistors to locate them."

"Our software can also narrow down the possible causes and develop fixes," he explained. "If we do not know that a chip has a bug, FogClear would not detect it by itself. However, when a bug has been observed, our software can locate and identify it."

The software conducts simulations of possible solutions to find the most cost-effective design variation that will fix the bugs, sometimes in ways that may be counterintuitive or not obvious to engineers doing the work in traditional ways.

In case studies, the researchers automatically repaired about 70 percent of major problems and reduced the debugging time from weeks to days, according to University of Michigan associate professor Igor Markov.