

THEME 2384.005, Robust design





Evaluation: Enhanced Observability Packet path reconstruction drop at drop append remaininc alternate hops PARSEC 83.76% 96.54% 100% network flow 100% 87.1% 97.6% Uniform traffic, 5 flits/packet **Packet interactions rouุter1 ∕** p16 router0 p87. ∠ p62 packets ordered by increasing execution time (timestampA) **p117** \succ common packets establish a p132 partial order of events timestampA timestampA

Distributed Alteration of Messages for On-Chip Network Debug Rawan Abdel-Khalek and Valeria Bertacco

Verification with Hardware Platforms







TASK 5.4: Scalable Verification



Debug Data Analysis

If an error is flagged , debug data is analyzed

Local Processing:

Reconstruct each packet's path

> Analyze packet latencies within routers

 determine routers and execution periods of interest
identify livelock bugs, starvations, misrouted segments, bugs in switch allocation and virtual allocation

Global Processing

Reconstruct events within each router

generate a partial order of interactions across routers





