



Motivation

Checkers that monitor architectural state are widely used in low-observability validation environments Bugs are detected by comparing architectural state

updates with those from a high-level golden model



memory address



- MOV r1, #0xBEEF **r1** = 0xBEEF
- ADD **r3**, r1, r2
- **r3** = 0xFEED ST r1, r3
- MEM(0xBEEF) = 0xFEED

0xBEE5 ≠ 0xBEEF : Mismatch!



7. Injecting synthetic bugs

Classifier model has to be trained on known bugs

- Known buggy unit along with associated bug signature(s)
- Large amount of training data required for learning

We developed a synthetic bug model and injection framework

- Random gate mutations to model bugs
- Automatic bug instrumentation and flexible injection control during simulation



BugMD: Automatic Mismatch Diagnosis for Bug Triaging

Biruk Mammo, Milind Furia, Valeria Bertacco, Scott Mahlke, and Daya S. Khudia

2. Limitations Diagnosis is difficult Several thousands of cycles between bug occurrence and manifestation Low-observability, limited information Simulation stops typically after first mismatch Patterns may emerge if simulation continues to collect more mismatches 3. (0x0C) ST r1, r3 design ISS value instr. type Instr. mismatch MEM[0xBEE5] = 0xFEED value count 4. (0x10) MOV r2, #4 0xBEEF MEM 0xBEE5 MEM ADDR $r^2 = 0x0004$ REG VALUE ALU 0xFEE4 **OxFEEE** 5. (0x14) ADD r4, r3, #1 CONTROL r4 = 0xFEE4 0x0020 PC VALUE 0x0028 6. (0x18) BR +0x10 PC = 0x0020What happens when design execution diverges? How do we automatically identify patterns? How do we get enough data to learn multiple patterns? 5. Learning patterns: features Unprocessed bug signatures are not amenable to machine learning ML algorithms take fixed-size, real valued feature vectors Bug signatures have arbitrary sizes, from 0 to millions of entries per simulation Symptoms need to be converted to meaningful, real-valued features Feature vector size needs to be reasonable compute differences and hamming distances design value **ISS** value instr. type mismatch namming type distance 0xBEE5 MEM ADDR MEM **0xBEEF** consider only **0xFEEE** REG VALUE ALU 0xFEE4 0xA windows of M instructions 0x1000 OVERFLOW ALU 0x1000 N+3 0x0000 group by mismatch type X instr. type take mean and stdev per group compute fraction of occurrence for each group # of samples fixed-length fraction of stdev mean mean stdev feature vector difference difference hamming hamming occurrence in window entries per mismatch type – instruction type pair

Results 8.

4-wide, out-of-order FabScalar core, 12 design units **6** instruction types 34 mismatch types **10,000** instruction window, feature vectors of size 470 **7080** synthetic bugs, over 40,000 bug signatures 6.8% 2.6% 4.2% 8.6% 2.2% 0.0% 0.3% 0.0% 3.8% 2.6% 9.9% 69.3% 4.2% 5.4% 5.1% 0.0% 0.0% 0.3% 0.0% 1.3%
 1.6%
 1.9%
 61.3%
 2.6%
 5.1%
 1.0%
 1.0%
 0.6%
 2.9

 2.6%
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 9% 7.3% 5.8% 2.2% 68.4% 1.0% 2.9% 2.2% 0.6% 2.9% <u>.3%</u> 0.0% 0.6% 0.3% 1.0% 90.1% 6.4% 0.0% 0.0% 0.6% i% 0.0% 0.0% 1.0% 4.2% 7.3% 78.9% 2.2% 2.9% 0.6% LSU 0.0% 0.0% 0.0% 1.9% 0.0% 0.0% 0.0% 0.0% 4.2% 92.7% 1.3% 0.0%
 RETIRE
 15.7%
 1.9%
 2.2%
 1.3%
 3.8%
 8.3%
 3.8%
 1.6%
 5.8%
 1.9%
 47.0%
 6.7%

 MAPTABLE
 0.0%
 0.3%
 0.3%
 16.3%
 1.0%
 1.0%
 0.3%
 0.3%
 6.7%







 Future work will explore better synthetic bug models and a cooperative selection of feature extraction approaches and classifiers

10. Technology transfer

- Industry interactions Dr. Daya S. Khudia was hired by
 - Intel Corporation
- Publications/presentations To appear in proceedings of
 - ICCAD'16
 - Manuscript uploaded to SRC

