2260 Hayward St. – 4620 CSE
Ann Arbor, MI 48109
Phone: (734) 647-7959
E-mail: twenisch@umich.edu

# Thomas F. Wenisch

Curriculum Vitae – February 2018

**Research Interests**

Computer architecture, server and data center energy efficiency, memory persistency, multiprocessor systems, performance evaluation methodology, medical imaging

**Education**

**PhD in Electrical and Computer Engineering,** Dec. 2007
*Carnegie Mellon University, Pittsburgh, PA*

- Dissertation title: Temporal Memory Streaming

**MS in Electrical and Computer Engineering**, May 2003
*Carnegie Mellon University, Pittsburgh, PA*

**Bachelor of Science in Computer Engineering,** Dec. 2000
**Bachelor of Arts in German,** Dec. 2000
*University of Rhode Island, Kingston, RI*

- Studied abroad at the Technische Universitaet Braunschweig, Germany in the Fall of 1999.

**Employment History**

| | | |
|---|---|---|
| 9/2017 - | University of Michigan | Ann Arbor, MI |
| **Associate Professor of Computer Science & Engineering**<br>**Associate Chair for External Affairs** | | |
| 9/2013 – 9/2017 | University of Michigan | Ann Arbor, MI |
| **Associate Professor of Computer Science & Engineering** | | |
| 7/2011 – 8/2013 | University of Michigan | Ann Arbor, MI |
| **Morris Wellman Faculty Development Assistant Professor of EECS** | | |
| 9/2007 – 6/2011 | University of Michigan | Ann Arbor, MI |
| **Assistant Professor, Computer Science & Engineering** | | |
| 6/15–8/15, 6/16-8/16, 6/17-8/17 | Google (Adecco) | Madison, WI |
| **Visiting Scientist (Consultant)** | | |
| 8/2013 – 8/2014 | Google | Madison, WI |
| **Visiting Scientist** | | |
| 9/2006 | AuthenTec | Melbourne, FL |
| **Security Consultant** | | |
| 9/2000 – 9/2006 | American Power Conversion | West Kingston, RI |
| **Software Developer** | | |
| 2/2000 – 8/2000 | Siemens AG | Munich, Germany |
| **Test Engineer (intern)** | | |

## Honors and Awards

Selection of "BiNoCHS: Bimodal Network-on-Chip for CPU-GPU Heterogeneous Systems" for **NOCS 2017 Best Paper Award.**

Recognized in the International Conference on Architectural Support for Programming Languages and Operating Systems **ASPLOS Hall of Fame**, 2017.

Selection of "Efficiently Scaling Out-of-Order Cores for Simultaneous Multithreading." as an Honorable Mention for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2016."

University of Michigan Computer Science & Engineering **Outstanding Achievement Award**, 2016. "For extraordinary accomplishments in scholarly research, classroom teaching, and student mentoring, and for leadership in service."

Recognized in the International Symposium of High Performance Computer Architecture **HPCA Hall of Fame**, 2015.

Selection of "Memory Persistency." for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2014."

University of Michigan **Henry Russel Award**, 2013.

University of Michigan College of Engineering **Ruth and Joel Spira Teaching Award**, 2013.

Selection of "Sonic Millip3De: A Massively Parallel 3D-Stacked Accelerator for 3D Ultrasound." for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2013."

Selection of "Computational Sprinting on a Hardware/Software Testbed." for **ASPLOS 2013 Best Paper Award.**

Selection of "Sonic Millip3De: A Massively Parallel 3D-Stacked Accelerator for 3D Ultrasound." for **HPCA 2013 Best Paper Award.**

Named the **Morris Wellman Faculty Development Assistant Professor of EECS** at the University of Michigan, 7/2011

Selection of "Computational Sprinting." for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2012."

Selection of "Computational Sprinting." for **HPCA 2012 Best Paper Award.**

Selection of "BigHouse: A Simulation Infrastructure for Data Center Systems." for **ISPASS 2012 Best Paper Award**

Recognized in International Symposium of Computer Architecture **ISCA Hall of Fame**, 2011.

Selection of "MemScale: Active Low-Power Modes for Main Memory." for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2011."

Selection of "Practical Off-chip Meta-data for Temporal Memory Streaming" for *IEEE Micro*'s "**Top Picks**" special issue for "most significant research papers in computer architecture based on novelty and long-term impact in 2009."

National Science Foundation **CAREER** Award, 2009-2013.
Proposal Title: Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture.

Lamme/Westinghouse Graduate Fellowship, 2004.

Intel Ph.D. Research Fellowship, 2003.

Honorable Mention, National Science Foundation Graduate Research Fellowship, 2002.

Laboratory for Computer Systems Fellowship, Carnegie Mellon University, 2001.

President's Award in Computer Engineering, University of Rhode Island, 2000.

Centennial Scholarship, University of Rhode Island, 1996-2000.

## Books

B. Falsafi & T. F. Wenisch. *A Primer on Hardware Prefetching*. Morgan & Claypool Synthesis Lectures on Computer Architecture. Morgan & Claypool, 2014.

**Refereed Conference Papers**

A. Mirhosseini, M. Sadrosadati, B. Soltani, H. Sarbazi-Azad, T. F. Wenisch. "BiNoCHS: Bimodal Network-on-Chip for CPU-GPU Heterogeneous Systems." *Proc. 11th IEEE/ACM International Symposium on Networks on Chip (**NOCS**)*, Oct. 2017. (**Best Paper Award**)

J. Zhou, S. Wei, R. Sampson, R. Jintamethasawat, O. D. Kripfgans, J. B. Fowlkes, T. F. Wenisch, C. Chakrabarti. "High volume rate 3D ultrasound imaging based on synthetic aperture sequential beamforming" *Proc. IEEE International Ultrasonics Symposium* (IUS), Sep. 2017.

A. Kolli, V. Gogte, A. Saidi, S. Diestelhorst, P. M. Chen, S. Narayanasamy, T. F. Wenisch. "Language-Level Persistency." *Proc. International Symposium on Computer Architecture (**ISCA**)*, Jun. 2017.

J. Huang, B. Mozafari, T. F. Wenisch. "Statistical Analysis of Latency Through Semantic Profiling. " In *Proceedings of Proceedings of the European Conference on Computer Systems (**EuroSys**)*, April 23-26, 2017.

J. Huang, B, Mozafari, G. Schoenebeck, T. F. Wenisch. "A Top-Down Approach to Achieving Performance Predictability in Database Systems." In *Proceedings of Proceedings of the ACM SIGMOD 2017 Conference (**SIGMOD**)*, May 14-19, 2017.

N. Agarwal, T. F. Wenisch, "Thermostat: Application-transparent Page Management for Two-tiered Main Memory." *Proc. International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Apr. 2017.

A. Kolli, J. Rosen, S. Diestelhorst, A. Saidi, S. Pelley, S. Liu, P. M. Chen, T. F. Wenisch. "Delegated Persist Ordering." *Proc. International Symposium on Microarchitecture (**MICRO**)*, Oct. 2016. (**Best Paper Nominee**.)

V. Gogte, A. Kolli, M. J. Cafarella, L. D'Antoni, T. F. Wenisch. "HARE: Hardware acceleration for regular expression matching." *Proc. International Symposium on Microarchitecture (**MICRO**)*, Oct. 2016.

S. Wei, J. Zhou, R. Sampson, R. Jintamethasawat, O. Kripfgans, J. B. Fowlkes, T. F. Wenisch, C. Chakrabarti., "Improving plane wave imaging performance through post-processing," 2016 IEEE International Ultrasonics Symposium (IUS), Oct. 2016, pp. 1-4.

R. Sampson, M. G. McGaffin, T. F. Wenisch, J. A. Fessler. "Investigating multi-threaded SIMD for helical CT reconstruction on a CPU." *Proc. 4th Intl. Mtg. on Image Formation in X-ray CT*, pp. 275-8, 2016.

F. Sleiman, T. F. Wenisch. "Efficiently Scaling Out-of-Order Cores for Simultaneous Multithreading." *Proc. of the International Symposium on Computer Architecture (**ISCA**)*, Jun. 2016. (**IEEE MICRO Top Picks Honorable Mention**.)

P. Tandon, F. Sleiman, M. J. Cafarella, T. F. Wenisch. "HAWK: Hardware Support for Unstructured Log Processing." *Proc. 32nd IEEE International Conference on Data Engineering (**ICDE**), May 2016.*

A. Kolli, S. Pelley, A. Saidi, P. M. Chen, T. F. Wenisch. "High-Performance Transactions for Persistent Memories." *Proc. of the 21st International Conf. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2016.

N. Agarwal, D. Nellans, E. Ebrahimi, T. F. Wenisch, J. Danskin, S. W. Keckler. "Selective GPU Caches to Eliminate CPU–GPU HW Cache Coherence." *Proc. of the 22nd International Symp. on High Performance Computer Architecture (**HPCA**)*, Mar. 2016.

R. Sampson, M. Yang, S. Wei, R. Jintamethaswat, J. B. Fowlkes, O. Kripfgans, C. Chakrabarti and T. F. Wenisch. "FPGA Implementation of Low Power 3D Ultrasound Beamformer." *Proc. of IEEE Ultrasonics Symposium* (IUS), Oct. 2015.

C.-H. Hsu, Y. Zhang, M. A. Laurenzano, R. Dreslinski, T. F. Wenisch, D. Meisner, J. Mars, L. Tang. "Adrenaline: Pinpointing and Reining in Tail Queries with Quick Voltage Boosting." *Proc. of the 21st International Symp. on High Performance Computer Architecture (**HPCA**)*, Feb. 2015.

N. Agarwal, D. Nellans, M. O'Connor, S. W. Keckler, T. F. Wenisch. "Unlocking Bandwidth for GPUs in CC-NUMA Systems." *Proc. of the 21st International Symp. on High Performance Computer Architecture (**HPCA**)*, Feb. 2015.

M. Chow, D. Meisner, J. Flinn, D. Peek, T. Wenisch. "The Mystery Machine: End-to-end performance analysis of large-scale Internet services." *11th USENIX Symposium on Operating Systems Design and Implementation (**OSDI**)*, Oct. 2014.

A. Lukefahr, S. Padmanabha, R. Das, R. G. Dreslinski Jr., T. F. Wenisch, and S. Mahlke. "Heterogeneous Microarchitectures Trump Voltage Scaling for Low-Power Cores." *Proc. of the International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, Aug. 2014.

M. Yang, R. Sampson, S. Wei, T. F. Wenisch, B. Fowlkes, O. Kripfgans and C. Chakrabarti. "High Volume Rate, High Resolution 3D Plane Wave Imaging." *2014 IEEE International Ultrasonics Symposium,* Jul. 2014.

S. Pelley, P. M. Chen, T. F. Wenisch. "Memory Persistency." *Proc. of the International Symposium on Computer Architecture (**ISCA**)*, Jun. 2014 (**IEEE Micro Top Picks**).

A. Hansson, N. Agarwal, A. Kolli, A. N. Udipi, T. F. Wenisch. "Simulating DRAM controllers for future system architecture exploration." *Proc. of the International Symp. on Performance Analysis of Systems and Software (**ISPASS**)*, Mar. 2014.

L. Shao, A. Raghavan, L. Emurian, M. C. Papaefthymiou, T. F. Wenisch, Milo M. K. Martin, K. P. Pipe. "On-chip Phase Change Heat Sinks Designed for Computational Sprinting." *Proc. of the 30th Annual Thermal Measurement, Modeling, and Management Symposium (**SemiTherm**)*, Mar. 2014

A. Kolli, A. Saidi, T. F. Wenisch. "RDIP: Return-address-stack directed instruction prefetching." *Proc. of the 46th Annual International Symp. on Microarchitecture (**MICRO**)*, Dec. 2013.

P. Tandon, J Chang, R. G. Dreslinski, V. Qazvinian, P. Ranganathan, T. F. Wenisch. "Hardware Acceleration for Similarity Measurement in Natural Language Processing." *Proc. of the International Conf. on Low Power Electronic Design (**ISLPED**)*, Aug. 2013.

R. Sampson, M. Yang, S. Wei, C. Chakrabarti, and T. F. Wenisch. "Sonic Millip3De with Dynamic Receive Focusing and Apodization Optimization." *2013 IEEE International Ultrasonics Symposium,* Jul. 2013.

J. M. Rosen, J. Wu, J. A. Fessler, T. F. Wenisch. "Iterative Helical CT Reconstruction in the Cloud for Ten Dollars in Five Minutes." *12th International Meeting on Fully Three-Dimensional Image Reconstruction in Radiology and Nuclear Medicine (**Fully3D**),* Jun. 2013.

K. Lim, D. Meisner, P. Ranganathan, A. Saidi, T. F. Wenisch. "Thin Servers with Smart Pipes: Designing SoC Accelerators for Memcached." *Proc., of the 40th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2013.

A. Raghavan, L. Emurian, L. Shao, M. Papaefthymiou, K. Pipe, T. F. Wenisch, M. M. K. Martin. "Computational Sprinting on a Hardware/Software Testbed." *Proc. of the 18th International Conf. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2013 (**Best Paper Award**).

R. Sampson, M. Yang, S. Wei, C. Chakrabarti, and T. F. Wenisch. "Sonic Millip3De: A Massively Parallel 3D-Stacked Accelerator for 3D Ultrasound." *Proc. of the 19th International Symp. on High Performance Computer Architecture (**HPCA**)*, Feb. 2013 (**Best Paper Award, IEEE Micro Top Picks**).

Q. Deng, D. Meisner, A. Bhattacharjee, T. F. Wenisch, and R. Bianchini. "CoScale: Coordinating CPU and Memory System DVFS in Server System." *Proc. of the 45th Annual International Symp. on Microarchitecture (**MICRO**)*, Dec. 2012.

A. Lukefahr, S. Padmanabha, R. Das, F. M. Sleiman, R. G. Dreslinski, T. F. Wenisch, and S. Mahlke. "Composite Cores: Pushing Heterogeneity into a Core." *Proc. of the 45th Annual International Symp. on Microarchitecture (**MICRO**)*, Dec. 2012.

F. Sleiman, R. Dreslinski, T. F. Wenisch. "Embedded Way Prediction for Large Last-Level Caches." *Proc. of the International Conf. on Computer Design (**ICCD**)*, Oct. 2012.

Q. Deng, D. Meisner, A. Bhattacharjee, T. F. Wenisch, R. Bianchini. "MultiScale: Memory System DVFS with Multiple Memory Controllers." *Proc. of the International Conf. on Low Power Electronic Design (**ISLPED**)*, Aug. 2012.

D. Meisner, J. Wu, T. F. Wenisch. "BigHouse: A Simulation Infrastructure for Data Center Systems" *Proc. of the International Symp. on Performance Analysis of Systems and Software (**ISPASS**)*, Apr. 2012 (**Best Paper Award**).

D. Meisner, T. F. Wenisch. "DreamWeaver: Architectural Support for Deep Sleep." *Proc. of the 17th International Conf. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2012.

A. Raghavan, Y. Luo, A. Chandawalla, M. Papaefthymiou, K. Pipe, T. F. Wenisch, M. M. K. Martin. "Computational Sprinting." *Proc. of the 18th International Symp. on High Performance Computer Architecture (**HPCA**)*, Feb. 2012 (**Best Paper Award, IEEE Micro Top Picks**).

K. Lim, Y. Turner, J Renato Santos, A. AuYoung, J. Chang, T. F. Wenisch, P. Ranganathan. "System-level Implications of Disaggregated Memory." *Proc. of the 18th International Symp. on High Performance Computer Architecture (**HPCA**)*, Feb. 2012.

A. Gutierrez, R. Dreslinski, T. F. Wenisch, T Mudge, A. Saidi, C. Emmons, N. Paver. "Full-System Analysis and Characterization of Interactive Smartphone Applications." *Proc. of the International Symp. on Workload Characterization (**IISWC**)*, Nov. 2011.

D. Meisner, T. F. Wenisch. "Does Low-power Design Imply Energy Efficiency for Data Centers?" *Proc. of the International Conf. on Low Power Electronic Design (**ISLPED**)*, Aug. 2011.

D. Meisner, C. Sadler, L. Barroso, W.-D. Weber, T. F. Wenisch. "Power Management of On-line Data Intensive Services." *Proc. of the 38th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2011.

D. Meisner, J. Wu, T. F. Wenisch. "Stochastic Queuing Simulation: A Scalable Data Center-level Evaluation Methodology." (short paper) *Proc. of the International Symp. on Performance Analysis of Systems and Software (**ISPASS**)*, Apr. 2011.

Q. Deng, D. Meisner, L. Ramos, T. F. Wenisch, R.Bianchini. "MemScale: Active Low-Power Modes for Main Memory." *Proc. 16th Int. Conf. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar 2011 (**IEEE Micro Top Picks**).

D. Meisner and T. F. Wenisch. "Peak Power Modeling for Data Center Servers with Switched-Mode Power Supplies." *Proc. of the International Conf. on Low Power Electronic Design (**ISLPED**)*, Aug. 2010.

S. Pelley, D. Meisner, P. Zandevakili, T. F. Wenisch, and J. Underwood. "Power Routing: Dynamic Power Provisioning in the Data Center." *Proc. of 15th International Conf. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2010.

C. Blundell, M. M. K. Martin, T. F. Wenisch. "InvisiFence: Performance-Transparent Memory Ordering in Conventional Multiprocessors." *Proc. of the 36th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2009.

Lim, J. Chang, T. Mudge, P. Ranganathan, S. K. Reinhardt, T. F. Wenisch. "Disaggregated Memory for Expansion and Sharing in Blade Servers." *Proc. of the 36th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2009.

S. Somogyi, T. F. Wenisch, A. Ailamaki, and B. Falsafi. "Spatio-Temporal Memory Streaming." *Proc. 36th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2009.

D. Meisner, B. T. Gold, and T. F. Wenisch. "PowerNap: Eliminating Server Idle Power." *Proc. of the 14th International Conf. on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Mar. 2009.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi and A. Moshovos. "Practical Off-chip Meta-data for Temporal Memory Streaming." *Proc. of the 15th International Symp. on High-Performance Computer Architecture (**HPCA**)*, Feb. 2009 (**IEEE Micro Top Picks**).

M. Ferdman, T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Temporal Instruction Fetch Streaming." *Proc. of the 41st Annual International Symp. on Microarchitecture (**MICRO**)*, Dec. 2008.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi and A. Moshovos. "Temporal Streams in Commercial Server Applications." *Proc. of the IEEE International Symp. on Workload Characterization (**IISWC**)*, 2008.

T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Mechanisms for Store-wait–free Multiprocessors." *Proc. of the 34th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2007.

S. Somogyi, T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Spatial Memory Streaming." *Proc. of the 33rd International Symp. on Computer Architecture (**ISCA**)*, Jun. 2006.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi and J. C. Hoe. "Simulation Sampling with Live-Points." *Proc. of the International Symp. on Performance Analysis of Systems and Software (**ISPASS**)*, Mar. 2006.

T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki, and B. Falsafi. "Store-Ordered Streaming of Shared Memory." *Proc. of the 14th International Conf. on Parallel Architectures and Compilation Techniques (**PACT**)*, Sep. 2005.

T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, A. Ailamaki, and B. Falsafi. "Temporal Streaming of Shared Memory." *Proc. of the 32nd International Symp. on Computer Architecture (**ISCA**)*, Jun. 2005.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, and J. C. Hoe. "TurboSMARTS: Accurate Microarchitecture Simulation Sampling in Minutes." (Short paper) *Proc. of the International Conf. on Measurement and Modeling of Computer Systems (**SIGMETRICS**),* Jun. 2005.

R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "SMARTS: Accelerating Microarchitecture Simulation via Rigorous Statistical Sampling." *Proc. of the 30th International Symp. on Computer Architecture (**ISCA**)*, Jun. 2003.

T. F. Wenisch, P. F. Swaszek and A. K. Uht. "Combined Error Correcting and Compressing Codes." *Proc. of the International Symp. on Information Theory (**ISIT**)*, Jun. 2001.

**Journal Articles**

S. Wei, M. Yang, J. Zhou, R. Sampson, O. Kripfgans, J.B. Fowlkes, T. F. Wenisch, C. Chakrabarti. "Low Cost 3D Flow Estimation of Blood with Clutter." *IEEE Transactions on on Ultrasonics, Ferroelectrics, and Frequency Control (**TUFFC**)* vol. 64, no. 5, pp 772-784, May 2017.

C.-H. Hsu, Y. Zhang, M. A. Laurenzano, R. Dreslinski, T. F. Wenisch, D. Meisner, J. Mars, L. Tang. "Achieving Low Tail Latency with High Energy Efficiency in Warehouse-Scale Computers with Adrenaline." *Transactions on Computer Systems (**TOCS**),* vol. 35, no. 1, Mar. 2017

Shao L., Raghavan A., Kim G., Emurian L., Rosen J., Papaefthymiou M., Wenisch T., Martin M., Pipe K., Figure-of-merit for phase-change materials used in thermal management, *International Journal of Heat and Mass Transfer*, vol. 101, Oct. 2016.

A. Lukefahr, S. Padmanabha, R. Das, F. M. Sleiman, R. G. Dreslinski, T. F. Wenisch, and S. Mahlke. "Exploring Fine-Grained Heterogeneity with Composite Cores." *IEEE Transactions on Computers (**TC**)*. 2015.

S. Pelley, P. M. Chen, T. F. Wenisch. "Memory Persistency: Semantics for Byte-Addressable NVRAM." ***IEEE MICRO** Special Issue on **Top Picks** in Computer Architecture 2014,* vol. 35 no. 3, May/Jun. 2015.

M. Yang, R. Sampson, S. Wei, T. F. Wenisch, and C. Chakrabarti, "Separable beamforming for 3-D medical ultrasound imaging," in *IEEE Transactions on Signal Processing (**TSP**)*, vol. 63, no. 2, pp. 279-290, Jan. 2015.

M. Yang, R. Sampson, S. Wei, T. F. Wenisch, and C. Chakrabarti, "High frame rate 3-D ultrasound imaging using separable beamforming," in *Journal of Signal Processing Systems (**JSPS**)*, vol. 78, no. 1, pp. 73-84, 2015.

S. Pelley, T. F. Wenisch, B. T. Gold, B. Bridge. "Storage Management in the NVRAM Era." *Proceedings of the Very Large Database Endowment (**VLDB**)*. vol. 7 no. 2, 2013.

A. Raghavan, Y. Luo, A. Chandawalla, M. Papaefthymiou, K. Pipe, T. F. Wenisch, M. M. K. Martin. "Utilizing Dark Silicon to Save Energy with Computational Sprinting." ***IEEE MICRO*** *Special Issue on Dark Silicon,* vol. 33 no. 5, Sep/Oct. 2013.

A. Raghavan, Y. Luo, A. Chandawalla, M. Papaefthymiou, K. Pipe, T. F. Wenisch, M. M. K. Martin. "Designing for Responsiveness with Computational Sprinting." ***IEEE MICRO*** *Special Issue on **Top Picks** in Computer Architecture 2012,* vol. 33 no. 3, May/Jun. 2013.

T. F. Wenisch, A. Buyuktosunoglu. "Energy-Aware Computing." (Guest Editor's Introduction) ***IEEE MICRO*** *Special Issue on Energy Aware Computing,* vol. 32 no. 5, Sep./Oct. 2012.

K. Sewell, R. G. Dreslinski, T. Manville, S. Satpathy, N. Pinckney, G. Blake, M. Cieslak, R. Das, T. F. Wenisch, D. Sylvester, D. Blaauw, and T. Mudge. "2D and 3D Swizzle-Switch Network Design" *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (**JETCAS**),* Jun. 2012.

Q. Deng, D. Meisner, L. Ramos, T. F. Wenisch, R. Bianchini. "Active Low-Power Modes for Main Memory with MemScale." ***IEEE MICRO*** *Special Issue on **Top Picks** in Computer Architecture 2011,* vol. 32 no. 3, May/Jun. 2012.

D. Meisner, B. T. Gold, and T. F. Wenisch. "The PowerNap Server Architecture." *ACM Transactions on Computer Systems (**TOCS**)*. Vol. 29, No. 1, Feb. 2011.

S. Somogyi, T. F. Wenisch, M. Ferdman, B. Falsafi. "Spatial Memory Streaming." *Journal of Instruction-Level Parallelism (**JILP**),* 13 (2011) 1-26.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi, and A Moshovos. "Making Address Correlated Prefetching Practical." ***IEEE MICRO*** *Special Issue on **Top Picks** in Computer Architecture 2009,* vol. 30 no. 1, Jan./Feb. 2010.

T. F. Wenisch, R. E. Wunderlich, M. Ferdman, A. Ailamaki, B. Falsafi, and J. C. Hoe. "SimFlex: Statistical Sampling of Computer System Simulation." ***IEEE MICRO*** *Special Issue on Computer Architecture Simulation and Modeling,* vol. 26, no. 4, Jul./Aug. 2006.

R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "Statistical Sampling of Microarchitecture Simulation." *ACM Transactions on Modeling of Computer Systems (**TOMACS**),* vol. 16, no. 3, Jul. 2006.

N. Hardavellas, S. Somogyi, T. F. Wenisch, R. E. Wunderlich, S. Chen, J. Kim, B. Falsafi, J. C. Hoe, A. Nowatzyk. "SimFlex: A Fast, Accurate, Flexible Full-System Simulation Framework for Performance Evaluation of Server Architecture." *ACM SIGMETRICS Performance Evaluation Review (PER)*, Vol. 31, No. 4, Mar. 2004.

A. K. Uht, D. Morano, A. Khalafi, M. de Alba, T. F. Wenisch, M. Ashouei and D. Kaeli. "Levo: IPC in the 10's via Resource Flow Computing." *IEEE Technical Committee on Computer Architecture Newsletter*, Special Issue: Oct. 2001.

**Workshop Papers**

A. Mirhosseini, M. Sadrosadati, B. Soltani, H. Sarbazi-Azad, T. F. Wenisch. "POSTER: Elastic Reconfiguration for Heterogeneous NoCs with BiNoCHS." *Proc. Conference on Parallel Architectures and Compilation Techniques (PACT),* Jun. 2017.

N. Agarwal, T. F. Wenisch, "Thermostat: Keeping your DRAM hot and NVRAM cool", to appear in Non-Volatile Memory Workshop (NVMW), March, 2017.

J. Zhou, S. Wei, R. Sampson, M. Yang, R. Jintamethasawat, O. Kripfgans, J. B. Fowlkes, T. F. Wenisch and C. Chakrabarti. "Low Complexity 3D Ultrasound Imaging Using Synthetic Aperture Sequential Beamforming." *Proc. of IEEE Workshop on Signal Processing Systems (SiPS)*, Oct. 2016.

A. Sriraman, S. Liu, S. Gunbay, S. Su, T. F. Wenisch. "Deconstructing the Tail at Scale Effect Across Network Protocols." *Workshop on Duplicating, Deconstructing, and Debunking (WDDD),* Jun. 2016.

A. Kolli, S. Pelley, A. Saidi, P. M. Chen, T. F. Wenisch. "High-performance transactions for persistent memories." *Non-Volatile Memory Workshop,* Mar. 2016.

S. Wei, M. Yang, R. Sampson, O. D. Kripfgans, J. B. Fowlkes T. F. Wenisch and C. Chakrabarti. "Low Cost Clutter Filter for 3D Ultrasonic Flow Estimation." *Proc. of IEEE Workshop on Signal Processing Systems*, Oct. 2015.

A. Kolli, S. Pelley, A. Saidi, P. M. Chen, T. F. Wenisch. "Persistency Programming 101." *Non-Volatile Memory Workshop,* Mar. 2015.

S. Wei, M. Yang, R. Sampson, T. F. Wenisch, B. Fowlkes, O. Kripfgans and C. Chakrabarti. "A Low Complexity Scheme for Accurate 3D Velocity Estimation in Ultrasound Systems." *Proc. of IEEE Workshop on Signal Processing Systems*, Oct. 2014.

M. Yang, R. Sampson, T.F. Wenisch, C. Chakrabarti. "Separable beamforming for 3-D synthetic aperture ultrasound imaging". In *2013 IEEE Workshop on Signal Processing Systems (SiPS),* Oct. 2013.

P. Tandon, M. J. Cafarella, T. F. Wenisch. "Minimizing Remote Accesses in MapReduce Clusters." *Proc. of the International Workshop on High Performance Data Intensive Computing (HPDIC),* May 2013.

P. Tandon, J. Chang, R. Dreslinski, P. Ranganathan, T. Mudge, T. F. Wenisch. "PicoServer Revisited: On the Profitability of Eliminating Intermediate Cache Levels." *Proc. of the Workshop on Duplicating, Deconstructing, and Debunking (WDDD),* Jun. 2012.

S. Pelley, T. F. Wenisch, K. LeFevre, " Do Query Optimizers Need to be SSD-aware?" *Proc. of the Second International Workshop on Accelerating Data Management Systems using Modern Processor and Storage Architectures (ADMS),* Jun. 2011.

R. Sampson, T. F. Wenisch, "ZCache Skew-ered." *Proc. of the 9th Workshop on Duplicating, Deconstructing, and Debunking (WDDD),* Jun. 2011.

D. Meisner, T. F. Wenisch, "Stochastic Queuing Simulation for Data Center Workloads." *Proc. of the Exascale Evaluation and Research Techniques Workshop,* Mar. 2010.

S. Pelley, D. Meisner, T. F. Wenisch, J. VanGilder. "Understanding and Abstracting Total Data Center Power." *Proc. of the Workshop on Energy Efficient Design (WEED),* Jun. 2009.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, and J. C. Hoe. "Statistical Sampling of Microarchitecture Simulation." *Proc. of the 2006 Workshop on the NSF Next Generation Software Program (NGS),* Apr. 2006.

S. Somogyi, T. F. Wenisch, N. Hardavellas, J. Kim, A. Ailamaki, and B. Falsafi. "Memory Coherence Activity Prediction in Commercial Workloads." *Proc. of the 3rd Workshop on Memory Performance Issues (WMPI)*, Jun. 2004.

R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "An Evaluation of Stratified Sampling of Microarchitecture Simulations." *Proc. of the 3rd Workshop on Duplicating, Debunking, and Deconstructing (WDDD),* Jun. 2004.

**Technical Reports**

L. Ceze, M. D. Hill, K. Sankaralingam, T. F. Wenisch "Democratizing Design for Future Computing Platforms." Computing Community Consortium. http://cra.org/ccc/wp-content/uploads/sites/2/2015/01/DemocratizingDesignforFutureComputingPlatforms-v2.pdf, Jun. 2017.

L. Ceze, T. F. Wenisch, M. D. Hill. "Arch2030: A Vision of Computer Architecture Research over the Next 15 Years." Computing Community Consortium. http://cra.org/ccc/wp-content/uploads/sites/2/2016/12/15447-CCC-ARCH-2030-report-v3-1-1.pdf, Dec. 2016.

P. Shenoy, T.F. Wenisch (ed.). "Report of the National Science Foundation Workshop on Sustainable Data Centers," Jun. 2016.

Computing Community Consortium. "21st Century Computer Architecture." A community white paper. http://cra.org/ccc/docs/init/21stcenturyarchitecturewhitepaper.pdf, Mar. 2012.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. C. Hoe, "TurboSmarts: Accurate Microarchitecture Simulation Sampling in Minutes," Technical Report 2004-3, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Nov. 2004.

T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki, and B. Falsafi. "SORDS: Just-In-Time Streaming of Temporally-Correlated Shared Data," TR 2004-2, Computer Architecture Laboratory at Carnegie Mellon (CALCM), Nov. 2004.

T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. C. Hoe, "Applying SMARTS to SPEC CPU2000," Technical Report 2003-1, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Jun. 2003.

**Patents**

A. Mirhosseini, T. F. Wenisch. "Cooperating Multithreaded Processor and Mode-Selectable Processor." Filed 1/18/18.

V. Gogte, M. Cafarella, T. F. Wenisch. "Detecting at least one predetermined pattern in stream of symbols." US Patent Appl. 20160267142, Filed 5/20/16

S. Diestelhorst, A. Kolli, A. G. Saidi, P. Chen, T. F. Wenisch. "Controlling Memory Access to Non-Volatile Memory." US Patent Appl. 20170123723, Filed 10/9/15.

P. Tandon, M. Cafarella, T. F. Wenisch. "Querying input data." US Patent Appl. 20160098411, Filed 9/23/14.

F. Sleiman, T. F. Wenisch. "A Data Processing Apparatus and Method for Executing a Stream of Instructions Out of Order with Respect to Original Program Order." US Patent Appl. 20170109172, Filed 4/1/14.

R. Sampson, T. F. Wenisch. "Hardware Acceleration for Beam-forming in Handheld 3-D Ultrasound Devices." US Patent 9,691,074, Issued 6/27/2017.

A. Saidi, T. F. Wenisch, A. Kolli. "Prefetching based upon return address." US Patent Pend., Filed 11/20/12.

F. Sleiman, R.G. Dreslinski, and T. F. Wenisch. "A Data Processing Apparatus Having a Cache Configured to Perfom Tag Lookup and Data Access in Parallel, and a Method of Operating the Data Processing Apparatus." US Patent No. 8,825,955, Issued 9/2/14.

A. Raghavan, M. Papaefthymiou, K. Pipe, T.F. Wenisch, M.M.K. Martin. "Computational Sprinting Using Multiple Cores." US Patent Appl 20140317389, Filed 11/18/11.

D. Roberts, T. Mudge, and T. F. Wenisch. "Cache memory with power saving state." US Patent No. 8,285,936, Issued 10/9/2012.

D. Meisner, T. F. Wenisch. "Computer Energy Conservation with a Scalable PSU Configuration." US Patent 8,751,843, Issued 6/10/2014.

T. F. Wenisch, S. R. Berard, D. J. Smith. "Computer Network Security System." US Patent No. 7,100,054. Issued 8/29/2006.

T. F. Wenisch. "Software-based Watchdog Method and Apparatus." US Patent No. 7,162,714. Issued 1/9/2007.

C. Kuiawa, D. Cardimino, T. Giaquinto, T. F. Wenisch. "Uninterruptible Power Supply Management Network System." US Patent Appl. 20030033548. Filed 8/7/2001.

**Keynote Presentations**

Report from the Arch2030 Visioning Workshop: Where are Computer Architects headed and what does it mean for GreenMetrics?". GreenMetrics Workshop (**Keynote**), Jun. 2017.

"Killer Microseconds and the Tail at Scale." Workshop on Resource Efficient Cloud Computing (**Keynote**), Jun. 2015.

"Power Management of On-line Data Intensive Services." (**Invited Plenary Talk**) Dasan Conference, Korean Federation of Science and Technology Society, Nov. 2011.

"Thinking Outside the Box: Power Management at the System Level & Beyond." (**Invited Plenary Talk**) Int. Symp. on Low Power Electronic Design (ISLPED), Aug. 2009.

**Presentations**

"BiNoCHS: Bimodal Network-on-Chip for CPU-GPU Heterogeneous Systems." International Symposium on Networks on Chip (NOCS), Oct. 2017.

"Thermostat: Application-transparent Page Management for Two-tiered Main Memory" International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Apr. 2017.

"Efficiently Scaling Out-of-Order Cores for Simultaneous Multithreading." International Symposium on Computer Architecture (ISCA), Jun. 2016.

"Killer Microseconds and the Tail at Scale." U. Rhode Island, Nov. 2016.

"Killer Microseconds and the Tail at Scale." Stony Brook U., Nov. 2015.

"Killer Microseconds and the Tail at Scale." U. Wisconsin, Aug. 2015.

"Computational Sprinting." Princeton, Dec. 2014.

"Computational Sprinting." U. Massachusetts - Amherst, Feb. 2014.

"Computational Sprinting." U. Wisconsin, Oct. 2013.

"Power Management from Smartphones to Data Centers." National Security Agency, May 2013.

"Power Management from Smartphones to Data Centers." UC Santa Barbara, Feb 2013.

"Power Management from Smartphones to Data Centers." Facebook, July 2012.

"Power Management from Smartphones to Data Centers." Oracle, July 2012.

"Efficiency Challenges in Warehouse-Scale Computers." UIUC, Mar. 2012.

"Efficiency Challenges in Warehouse-Scale Computers." Washington U., Mar. 2, 2012.

"Efficiency Challenges in Warehouse-Scale Computers." U. Edinburgh, Mar. 2012.

"Efficiency Challenges in Warehouse-Scale Computers." Wayne State U., Jan. 2012.

"Power Management of On-line Data Intensive Services." POSTECH, Korea, Nov. 2011.

"Making Enterprise Computing Green." Princeton University, Oct. 2011.

"Making Enterprise Computing Green." Yahoo!, Jul. 2011.

"Architectures and Evaluation Methods for On-line Data Intensive Services Running on Warehouse Scale Computers." NSF Workshop on Sustainable Energy-Efficient Data Management, May 2011.

"Server/data center energy efficiency challenges." ASPLOS PC Symposium, Oct. 2010.

"Making Enterprise Computing Green." IBM Austin Research Lab, Aug. 2010.

"Making Enterprise Computing Green." Microsoft Research, Feb. 2010.

"Making Enterprise Computing Green." U. Washington, Feb. 2010.

"Making Enterprise Computing Green." Wayne State University, Oct. 2009.

"Making Enterprise Computing Green." Yahoo! HKN Seminar Series, Mar. 2009.

"Making Enterprise Computing Green." Merit Member Conference, Jun. 2009.

"Making Enterprise Computing Green." Tutorial at the International Conference on High-Performance Computing (HiPC), Dec. 2008.

"Improving Memory System Performance and Eliminating Idle-power Waste in Commercial Servers." Intel Research Bangalore, Dec. 2008.

"Hiding Memory Latency in Commercial Server Application." Indian Inst. of Sci., Dec. 2008.

"Mechanisms for Store-Wait-Free Multiprocessors." ARM, Nov. 2008.

"Making Enterprise Computing Green: Energy-efficiency Challenges in Enterprise Data Centers." Carnegie Mellon University, Oct. 2008.

"Hiding Memory Latency in Commercial Server Application." IBM TJ Watson, Jul. 2008.

"Mechanisms for Store-Wait-Free Multiprocessors." 34th International Symposium on Computer Architecture (ISCA), Jun. 2007.

"Temporal Memory Streaming." University of Toronto, University of Michigan, MIT, Columbia University, UT-Austin, Microsoft Research-Silicon Valley, Microsoft Research-Redmond, HP Labs in Feb.-Apr. 2007.

"Improving the Simulation and Programmability of Future Multiprocessor Systems." Brown University, Jan 2007.

"SimFlex: Simulation Sampling Theory and Practice." University of Pittsburgh, Feb. 2006.

"Store-Ordered Streaming of Shared Memory." 14th International Conference on Parallel Architectures and Compilation Techniques (PACT), Sep. 2005.

"Temporal Streaming of Shared Memory." 32nd International Symposium on Computer Architecture (ISCA), Jun. 2005.

"TurboSMARTS: Accelerating Microarchitecture Simulation Sampling in Minutes." Princeton, Sep. 2004.

"Breaking the Memory Wall." Intel, Santa Clara, CA, Oct. 2003.

"SMARTS: Accelerating Microarchitecture Simulation via Rigorous Statistical Sampling." 30th International Symposium on Computer Architecture (ISCA), Jun. 2003.

"Combined Error Correcting and Compressing Codes" International Symposium on Information Theory (ISIT), Jun. 2001.

**Press Coverage**

"Your Future iPhone May Be Stuffed With Wax," *Wired* 8/23/13.

"'Sprinting' chips could push phones to the speed limit," *New Scientist* #2852, 2/20/12.

"Could 'Computational Sprinting' Speed Up Smart Phones without Burning Them Out?," *Scientific American*, 2/29/12.

"Researchers Propose 'Computational Sprinting' To Speed Up Chips By 1000% – But Only For A Second," *TechCrunch*, 2/28/12.

"Researchers propose 'overclock' scheme for mobiles; Processing at a sprint to overcome tech limitations," *The Register*, 2/21/12.

"Study explores computing bursts for smartphones," *PhysOrg.com*, 2/21/12.

"Green Data Centers." WEMU 89.1 FM **Radio Interview.** 7/27/2011.

"PowerNap plan could save 75 percent of data center energy." *U-M News Service*, 3/5/09.

"'Napping' data centers could cut energy use by 75 percent." *ZDNet Asia*, 3/6/09.

"Optimizing The Sleep Cycle." *Processor.com*, 6/5/09.

"Merit Member Conference Covers Cool Learning Technology." *WWJ Radio*, 6/11/09.

**Grants**

Applications Driving Architectures (ADA) Center (Semiconductor Research Corporation; $27,500,000; 2018-2023; V. Bertacco-Director; T. Wenisch-Theme Leader; 14 additional investigators)

II-New: Infrastructure for THz Computing and Signal Processing Organization (NSF; II-1727610; $620,000; 2017-2020; P. Mazumder-PI, T.Wenisch-Co-PI; 3 additional investigators)

VehiQL: Query Processing for Visual Data Streams (Toyota Research Institute; $1,126,926; 2017-2020; T.Wenisch-PI, J. Deng, M. Cafarella-Co-PIs)

Managing Huge Pages in a Two-Tiered Main Memory (Google; $71,000; 2016)

VEC: Medium: Large-Scale Visual Recognition: From Cloud Data Centers to Wearable Devices (NSF/Intel; IIS-1539011; $1,350,000; J. Deng-PI, T.Wenisch-Co-PI, additional co-Investigators; 2015-2018)

CCF/SHF: Small: Memory Persistency: programming paradigms for byte-addressable, non-volatile memories (NSF; CCF-1525372; $499,996; T.Wenisch-PI, P. Chen-Co-PI; 2015-2018)

NSF Workshop on Sustainable Data Centers (NSF; CSR-1523304; $50,000; T.Wenisch-PI; 2015-2016)

Explicit Huge Pages: Implications of Discarding the 4KB Page Size (Google; $65,000; 2015)

Accelerated Statistical Image Reconstruction Methods (NIH; U01 EB01875301; $1,947,603 J. Fessler-PI, T. Wenisch-Co-PI; numerous co-Investigators; $411,559 to Wenisch; 2014-2018)

CCF/SHF: Medium: Collaborative Research: Advanced Architectures for Hand-held 3D Ultrasound (NSF; CCF-1406739; $1,000,000; T.Wenisch, C. Chakrabarti (ASU), B. Fowlkes, J. Rubin; 2014-2018)

CCF/SHF: Medium: Collaborative Research: Ultra-Responsive Architectures for Mobile Platforms (NSF; CCF-1161505; $900,000; CCF-1623834; $115,228; M. Martin (U. Penn), T. Wenisch, M. Papaefthymiou, K. Pipe; 2012-2016)

RunDMC: Durable Memory Consistency (Oracle; $150,000; 2012)

A Data-Centric Approach to Energy Proportionality (Google; $1,500,000; R. Bianchini (Rutgers), S. Gurumurthi (U. Virginia), F. Chong (UCSB), T. Wenisch; $375,000 to Wenisch; 2010-2012)

Re-architecting Memory and Processors for Energy Efficiency (Google; $100,000; T. Wenisch-PI, T. Mudge–Co-PI, D. Blaauw–Co-PI, D. Sylvester–Co-PI, 2010)

Toward Energy-Proportional Web Search Clusters (Google; $65,000; 2010)

CAREER: Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture (NSF; CCF-0845157; T. Wenisch–PI; $400,000; 2009-2013)

Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture (Intel; $120,000; 2009-2011)

CSR-DMSS,SM: Beyond Solid State Disks: Using FLASH to save energy in Enterprise Systems (NSF; CSR-0834403; T. Wenisch–PI, T. Mudge–Co-PI; $280,000; 2008-2011)

CPA-CSA: Virtualization Mechanisms for Zero-Idle-Power and Thermally-Efficient Data Centers (NSF; CCF-0811320; T. Wenisch–PI; $275,000; 2008-2011)

Disaggregated Memory for Energy-Efficient Data Centers (HP Labs; T. Mudge–PI, T. Wenisch–Co-PI; $145,000; 2008-2009)

FloVent License Grant (Flomerics; $9,600; 2008-2009)

Equipment Donation (Intel; $30,000; 2008)

## Professional Activities & External Service

**Program Committee Chair,** International Symposium on Performance Analysis of Software and Systems (ISPASS), 2018.

**General Co-Chair,** IEEE International Symposium on Low Power Electronic Design (ISLPED), 2018.

Shadow Program Committee Coordinator**,** International Conf. on Architectural Support for Programming Languages and Operating Systems **(**ASPLOS), 2018.

**Selection Committee Chair,** IEEE MICRO Top Picks, 2017.

**Associate Editor in Chief**, IEEE Computer Architecture Letters, 2017-.

Associate Editor, ACM Transactions on Architecture and Code Optimization, 2017-.

Member, SIGARCH/TCCA Reviewing Reviewing Committee, 2017-.

**Program Committee Co-Chair,** IEEE International Symposium on Low Power Electronic Design (ISLPED), 2017.

Guest Editor, IEEE Internet Computing Special Issue on Energy-Efficient Data Centers, 2017.

Co-organizer of the Architecture 2030 Workshop, with ISCA 2016.

Co-organizer of the USENIX Workshop on Cool Topics in Sustainable Data Centers (CoolDC), 2016.

**IEEE TCCA Executive Committee Member,** 2015-.

Co-organizer of the NSF Workshop on Sustainable Data Centers, 2015.

Associate Editor, ACM Transactions on Design Automation of Electronic Systems, 2015-.

Associate Editor, IEEE Computer Architecture Letters, 2015-2016.

**Program Committee Co-Chair,** IEEE International Symposium on Microarchitecture (MICRO), 2014

**Program Committee Chair,** IEEE International Symposium on Workload Characterization (IISWC), 2012.

**Co-Chair,** HotPower 2012.

Guest Editor, IEEE Micro Special Issue on Energy-Aware Computing (Sep.-Oct. 2012).

Panelist: “Collaborative Tools and Reproducibility of Research Experiments in Exascale Computer Systems.” EXADAPT Workshop held with ASPLOS (2012).

Program Track Co-Chair, Architecture for the Networking, Architecture & Storage Conference (NAS) 2011.

Invited Delegate to NSF Workshop on Sustainable Energy Efficient Data Management (SEEDM), May 2011.

Co-organizer of the Exascale Evaluation and Research Techniques (EXERT) Workshop held in conjunction with ASPLOS 2010, 2011.

Co-organizer of the Annual Workshop on Modeling, Benchmarking, and Simulation (MoBS), held in conjunction with ISCA 2009, 2010, 2011.

Tutorial presentation: T. F. Wenisch. "Making Enterprise Computing Green". Held in conjunction with HiPC 2008 (Bangalore, India).

Tutorial presentation: T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. Hoe. "SimFlex: Fast, Accurate and Flexible Simulation of Computer Systems". Held in conjunction with:
38th Annual International Symposium on Microarchitecture (MICRO), Nov. 2005
33rd International Symposium on Computer Architecture (ISCA), Jun. 2006.

Panelist: "Cycle-Accurate Simulators: Knowing When to Say When." held with ISCA (2008).

Principal developer of the Flexus full-system multiprocessor computer architecture simulation framework, publicly available at http://www.ece.cmu.edu/~simflex.

Principal developer of the TurboSmartsim simulation sampling & checkpointing extensions to SimpleScalar, publicly available at http://www.ece.cmu.edu/~simflex.

Workshops Chair for PACT (2012).

Workshops & Tutorials chair for IISWC (2010).

Publications chair for PACT (2010).

Publications chair for MICRO (2009).

Finance chair for PACT (2008).

National Science Foundation Panelist 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018.

Technical Program Committee Member for ISCA (2013, 2015, 2016, 2018), HPCA (2013, 2014, 2015, 2017), ASPLOS (2011, 2013, 2014, 2018), SIGMETRICS (2013, 2018), ISPLED (2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017), DAC (2016), IGCC (2012), ICPP (2010, 2012), HiPEAC (2011, 2012), ISPASS (2009, 2010, 2012, 2017), HotPower (2009, 2011, 2012, 2013), WEED (2009, 2010, 2011, 2012), MICRO (2011, 2014, 2016, 2017), ICS (2009, 2011), PACT (2009, 2010), HotMetrics (2010), eEnergy (2010), DATE (2008, 2009), WISH (2009), IEEE MICRO Top Picks (2009, 2012, 2014, 2015, 2016, 2017, 2018), TRANSACT (2008), MOBS (2008), CMP-MSI (2008).

Member of the ACM and IEEE.

**PhD Alumni**

David Meisner, 2012 (Facebook)

Steven Pelley, 2014 (Snowflake)

Faissal Sleiman, 2015 (Pure Storage)

Prateek Tandon, 2015 (Amazon Web Services)

Neha Agarwal, 2017 (Google)

Aasheesh Kolli, 2017 (Pennsylvania State University)

Richard Sampson, 2017 (Philips)

**Teaching**

EECS 370 – Computer Organization (F'09, F'14, F'15, F'17)

EECS 470 – Computer Architecture (F'07, W'09, W'10, F'11, F'12, F'16)

EECS 570 – Parallel Computer Architecture (W'11, W'12, W'13, W'15, W'16, W'17)

EECS 598 – Enterprise Systems (W'08)