EECS 470 Fall ‘07
Homework 5
Due Fri. Nov. 16th at the start of discussion. No late homeworks.

Name: _______________________________  unique name: ________________

You are to turn in this sheet as a cover page for your assignment. The rest of the assignment should be stapled to this page. This is an individual assignment, all of the work should be your own. Assignments that are unstapled, lack a cover sheet, or are difficult to read will lose at least 50% of the possible points and we may not grade them at all. This assignment is worth a bit less than 2% of your grade in the class and is graded out of 30 points. Remember you may drop one homework assignment.

1) Given a virtually indexed, physically-tagged cache that is four-way associative and has 64-byte blocks, what is the largest total size the cache could have if pages were 8KB in size? What is the largest number of sets it could have in that case? How would these two values change if the cache were direct-mapped? [4]

2) Consider a virtual memory system where a TLB access takes 4ns and there is a single level of a set-associative, write-back data cache with the following parameters:
   • indexing the cache to access the data portion takes 10ns
   • indexing the tag array of the data cache takes 8ns
   • tag comparisons take 3ns
   • multiplexing the output data takes 1ns

   Assume these are the only parts that affect the cache access time. For each of the following configurations, calculate the amount of time it takes to get data from the cache on a hit, including any needed TLB access time. Please explain your answers for full credit.
   a. The page size is 4KB and the data cache is 16 KB, 4-way set associative, with block size of 16 bytes. The cache is physically-indexed and physically-tagged. [2]
   b. The page size is 4KB and the data cache is 16 KB, 4-way set associative, with block size of 16 bytes. The cache is virtually-indexed and virtually-tagged. [2]
   c. The page size is 4KB and the data cache is 16 KB, 4-way set associative, with block size of 16 bytes. The cache is virtually-indexed and physically-tagged. [2]

3) Describe one hardware and one software solution to mitigate the synonym problem in the D-cache. [6]

4) In one or two sentences, explain why it is difficult to support multiple page sizes in a hardware TLB. [5]

5) Consider a system where:
   • VA is 32-bit wide
   • PA is 40-bit wide
   • page size is 4 KByte
   • each process has its own 2-level hierarchical page table
   • the 4-KByte first-level page table holds descriptors (4 bytes each) to L2 page tables
   • the 4-KByte second-level page table holds PTEs (4 bytes each)
   • The system employs a top-down hierarchical page table (similar to SPARC v8)

   a. Show which bits of the virtual address and indicate index the first- and the second-level page tables. [3]
   b. If a process accesses $2^{32}$ bytes of memory (i.e., its entire virtual address space), how many bytes of physical memory need to be allocated to its hierarchical page table? [3]
   c. If a process accesses $2^{22}$ bytes of memory, what are the upper bound and lower bound on the amount of physical memory allocated to its hierarchical page table? (explain how you computed each bound) [3]