EECS 470 Fall ‘07
Homework 1
Due Friday Sep. 14th at the start of discussion. Late homeworks are not accepted.

Name: ___________________________ unique name: __________________

You are to turn in this sheet as a cover page for your assignment. The rest of the assignment should be stapled to this page. Assignments that are unstapled, lack a cover sheet, or are difficult to read will lose at least 50% of the possible points and we may not grade them at all. This is an individual assignment; all work should be your own.
- If you use references other than the text and class notes, be sure to cite them!
- This assignment is worth about 2% of your grade in the class and is graded out of 30 points.
- Remember you may drop one homework assignment score.
- Please state any assumptions.

1. Understanding Pipelines. Consider the following code segment:

\[
\text{Loop: } \text{LD R1, } 0(R2) \; ; \text{R1=MEM[R2+0]} \\
\text{DADDI R1, R1, } #1 \; ; \text{R1=R1+1} \\
\text{SD } 0(R2), \text{R1} \; ; \text{MEM[R2+0]=R1} \\
\text{DADDI R2, R2, } #4 \; ; \text{R2=R2+4} \\
\text{DSUB R4, R3, R2} \; ; \text{R4=R3-R2} \\
\text{BNEZ R4, Loop } \; ; \text{if(R4!=0) goto Loop}
\]

a. Show the timing of the instruction sequence of the RISC pipeline in Appendix A. Assume there is no forwarding but that a read and write in the same clock cycle “forwards” through the register file. Your answer should be drawn like figure A.5. Memory accesses take one cycle. How many cycles does a single iteration of this loop take to execute? [3]
b. As part “a” but assume normal forwarding and bypassing. Assume the branch is predicted not-taken. [3]
c. Assume the RISC pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware. Schedule the instruction including the branch delay slot. You may reorder the instructions and modify the individual instruction operands, but do not change the number or opcode of the instructions. Again provide a timing diagram and indicate the number of cycles needed for a single iteration of the loop. [5]

2. Digital Logic Design. Consider the following Moore-type state-machine:

\[(1 \& !B) \quad \text{X=1} \quad \text{X=0} \quad (1 \& B) + (A \& !B) \]

\[(A \& B) + !A \& !B\]

Draw a circuit diagram which implements this state-machine. You are to use only 2-input AND, OR and XOR gates, inverters, and D flip-flops. The inputs are not available in inverted form. [5]

3. Cache Design. Consider a 64-KB 4-way set-associative cache with 64-byte lines. Both the virtual and physical address spaces are 32-bits in size.

a. How many bits are used for the tag comparison, set index, and byte offset respectively? [2]
b. How many bytes (total) are used to store the tags for this cache? [2]
c. What would your answer to b) be if the cache were fully-associative? Direct-mapped? [2]
4. **Performance Analysis.** Assume an in-order processor runs at 0.8 CPI (1.25 IPC) when all instructions hit in the instruction cache and all loads hit in the data cache. For a given workload, 25% of instructions are loads, the instruction cache miss rate is 1%, the data cache miss rate is 10%, and the average miss latency for both caches is 100 cycles. What are the net CPI and IPC after taking into account the cache effects? [4]

5. **Averaging Methods.** According to Tom’s Hardware (http://www.tomshardware.com), the Intel Core 2 Extreme QX6850 is 1.57 times faster than the AMD Athlon 64 X2 6000+ on the PCMark 2005 (CPU) benchmark, 1.09 times faster on the PCMark 2005 (Mem) benchmark, and 1.26 times faster on the Quake IV THG Timedemo.
   a. Which averaging method should be used to summarize the speedup of the Intel chip over the AMD chip, and why? [2]
   b. Calculate average speedup. [2]