CURRICULUM VITAE

Todd M. Austin

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I Personal Data

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II Academic History

A. Education

Doctor of Philosophy in Computer Science, University of Wisconsin-Madison, March 1996.
Thesis: "Hardware and Software Mechanisms for Reducing Load Latency".
Advisor: Professor Gurindar S. Sohi

Master of Science in Computer Engineering, Rochester Institute of Technology, August 1990.
Thesis: "Exploiting Implicit Parallelism in SPARC Instruction Execution".
Advisor: Professor Jim E. Heliotis

Bachelor of Science in Electrical Engineering with a second major in Computer Science, University of Wisconsin-Madison, December 1987.

B. Present Positions

Professor of Computer Science and Engineering, The University of Michigan.
Director, Center for Future Architectures Research (C-FAR)

C. Career Highlights

- I work broadly in computer architecture, VLSI design, compilers, and verification, and I have had a number of highly visible projects, including (ordered most recent to older):
  - EVA - next-generation platforms for mobile vision computing
  - Testudo - massively scalable security vulnerability analysis technologies
  - BulletProof - ultra low-cost defect-tolerant microarchitectures
  - Subliminal - ultra low-power subthreshold-voltage architectures
  - Razor - timing-error tolerant pipeline designs
  - MUSE - symbolic execution of dynamic instruction traces to identify security bugs
  - DIVA - dynamic pipeline verification
  - CryptoManiac - crypto-specific processor architectures
  - SafeC - dynamic detection of C program pointer errors
  - SimpleScalar - architectural modeling tools

- I was one of the earliest and strongest proponents of run-time verification, which is the concept of lessening verification cost by adding on-line correction for faults and bugs that cannot be handled at design time. My work on the DIVA fault-tolerant pipeline is a widely cited work in computer architecture, with over 550 references to date. My later work on Razor, which is a technique to tolerate circuit-timing faults, has received much attention by industry as companies explore the possibility of adopting Razor in their designs (e.g., ARM, Intel, IBM). Today, run-time verification is a prominent research area in computer architecture.

- I am the developer of the SimpleScalar Tool Set, a popular collection of computer architecture performance analysis tools. In 2007, almost 3 out of 10 papers published in top computer architecture conferences used the SimpleScalar tools to evaluate their designs. The papers I co-authored about SimpleScalar are widely cited papers with over 6,500 references to date.

- In 2007, I won the Maurice Wilkes Award for “innovative contributions in computer architecture, including the SimpleScalar Toolkit and the DIVA and Razor architectures”. This award is the top mid-career ACM award in computer architecture. In 2016, I became an IEEE Fellow.

- I am co-author (with Andrew Tanenbaum) of “Structured Computer Architecture”, a popular undergraduate computer architecture textbook. I joined Andrew as co-author of the sixth edition, which includes a detailed treatment of architectures from Intel and ARM.

- I have a strong commitment to sharing my passion for computing with others. For example, I have been working in Ethiopia to help their national university develop IT programs, including a graduate program to train professors. During my 2012 sabbatical, I had the good fortune to spend a semester teaching at Addis Ababa University in Ethiopia.

- At the University of Michigan, I have earned a reputation as an outstanding mentor and teacher. The evaluation scores I receive for courses are consistently high, even hitting a perfect 5.0 score on occasion. In addition, I have had good success at placing my PhD students into tenure-track academic positions, including Virginia Tech and Seattle University.

D. Academic Appointments

September 2009 - present	Professor, Computer Science and Engineering, The University of Michigan
June 2003 - August 2009	Associate Professor, Computer Science and Engineering, The University of Michigan
July 1999 - June 2003	Assistant Professor, Computer Science and Engineering, The University of Michigan
January 1997 - May 1999	Adjunct Assistant Professor, Computer Science and Engineering, Oregon Graduate Institute
January 1992 - March 1996	Research Assistant, Computer Sciences Department, University of Wisconsin - Madison
January 1990 - Dec 1991	Teaching Assistant, Computer Sciences Department, University of Wisconsin - Madison

E. Honors and Awards

- IEEE Fellow for “contributions to simulation techniques and resilient system design in computer architecture”, 2017.
- Distinguished Paper Award, 2016 IEEE Symposium on Security and Privacy (Oakland 2016), this is the top “best paper” award (of four given each year) at the Oakland conference.
- Nominated for a 2016 Pwnie Award in the category of Most Innovative Research, for the research “A2: Analog Malicious Hardware”.
- 2015 University of Michigan College of Engineering Research Excellence Award
- 2013 IEEE Senior Membership
- 2012 Richard Newton GSRC Industrial Impact Award for “development of the DIVA technology”. The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is “at least five years old and has had significant industrial impact.”
- 2010 GSRC Margarida Jacome Best Poster/Demo Award, given to graduate student Andrea Pellegrini and Profs. Valeria Bertacco and Todd Austin for demo of the work from “Fault-Based Attack of RSA Authentication”, September 2010.
- 2009 Ted Kennedy Family Team Excellence Award, given to Profs. Austin, Blaauw, Mahlke, Mudge, and Papaefthymiou for work in low-power research and design, February 2009.
- 2008 Richard Newton GSRC Industrial Impact Award for “development of the Razor technology” (awarded to Profs. Todd Austin and David Blaauw). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is “at least five years old and has had significant industrial impact.”
- 2007 Maurice Wilkes Award for “innovative contributions in Computer Architecture including the SimpleScalar Toolkit and the DIVA and Razor architectures”, June 2007.
- Microprocessor Report Analysts' Choice Award for Innovation, 2007, for “introducing and implementing Razor technology”, April 2007.
- “Top Pick” Award, for the paper “Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation,” in the IEEE MICRO Top Picks of 2004, March 2005.
- Henry Russel Award, University of Michigan, March 2004.
- University of Michigan College of Engineering Education Excellence Award, January 2004.
- Best Paper Award, “Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation”, in the 36th International Symp. on Microarchitecture (MICRO-36), November 2003.
- Ruth and Joel Spira Outstanding Teacher Award, September 2002.
- Packard Fellowship nominee (one of two from UM), April 2002.
- Alfred P. Sloan Research Fellow, March 2002.
- CAREER Award, National Science Foundation, February 2001.
- Best Paper Award, “DIVA: A Reliable Substrate for Deep Submicron Microarchitecture Design”, in the 32nd Int’l Symp. on Microarchitecture (MICRO-32), November 1999.
- Best Presentation Award, “DIVA: A Reliable Substrate for Deep Submicron Microarchitecture Design”, at the 32nd Int’l Symp. on Microarchitecture (MICRO-32), November 1999.
- Intel Exceptional Mentor Award, August 1998.

- Intel Individual Inter-Divisional Award, presented by Intel MAP Santa Clara for work on development of the SPEC'98 benchmark suite, April 1997.
- Nominee for Outstanding Graduate Researcher Award (3 nominees total), UW-Madison Computer Sciences Department, 1996.

F. Student Honors and Awards

- C-FAR Best Student Demo Runner-Up Award, for the demo "Cold Boot Attacks on the DDR3 Memory Scrambler", by Misiker Aga and Salessawi Ferede Yitbarek, May 2016.
- NVIDIA Fellowship, awarded to Jason Clemons, April 2012.
- CSE Honors Research Competition First Prize, awarded to Joe Greathouse, December 2011.
- GSRC 2011 Margarida Jacome Best Poster/Demo Award, given to Jason Clemons for his demonstration of the Michigan Visual Sonification System (MVSS), November 2011.
- CGO 2011 Best Student Presentation, awarded to Joe Greathouse for presentation of the paper "Highly Scalable Distributed Dataflow Analysis", by Joe Greathouse, Chelsea LeBlanc, Valeria Bertacco and Todd Austin, April 2011.
- Intel Fellowship Award, awarded to Kypros Constantinides, April 2009.
- CSE Honors Research Competition First Prize, awarded to Leyla Nazhandali, March 2005.

III Research Experience

A. Research Interests

The design and implementation of high-performance, power-efficient, and cost-effective computing systems. My research interests include computer architecture, reliable system design, hardware and software verification, and performance analysis tools and techniques.

B. Doctoral Students Supervised

Student	Thesis Title/Topic	Graduation Date/ (First Employment)
Eric Larson	Dynamic Compilation and Optimization	April 2004 (faculty Seattle Univ.)
Rajeev Krishna	Formal Specification of Architectural Semantics	April 2004 (med student, Ohio St)
Dan Ernst	High-Performance Scheduling Architectures	April 2005 (faculty UW-Eau Clare)
Leyla Nazhandali	Area and Power Constrained Architectures	May 2005 (faculty Virginia Tech)
Kypros Constantinides	Defect-Tolerant Microarchitectures	April 2009 (Microsoft)
Andreas Moustakas	Instruction-Level Symbolic Simulation	August 2009 (M.S. only) (Apple Computer)
Joseph Greathouse	Highly Scalable Distributed Dataflow Analysis	December 2012 (AMD)
Jason Clemons	Visual Computing Architectures	March 2013 (NVIDIA)
William Arthur	Control-Flow Security	April 2016 (Univ. of Michigan)
Salessawi Ferede Yitbarek	Near-Memory Computing Paradigms	May 2018 (expected)
Zelalem Aweke	Secure Computing with Restricted Pointers	May 2018 (expected)
Misiker Aga	Subtractive Security Technologies for Provably Secure Hardware	May 2019 (expected)

C. Masters Students Supervised

Student	Research Topic	Graduation Date
Lisa Wu	CryptoManiac: A Fast Flexible Architecture for Secure Communication	May 2001
Saugata Chatterjee	Microprocessor Verification at Runtime	May 2001
Patrick Cassleman	A Self-Tuned 3DES Implementation	May 2001
Ryan Vinson	Simulation Test Infrastructure Development	May 2001
Chris Burke	A Self-Tuned Secure Hash Implementation	May 2001
John McDonald	The AVID Pre-Execution Processor	May 2002
Christopher Drake	Dynamic Verification of Crypto Algorithms	May 2002
Andrew Hamel	Semi-static Approaches to Dynamic Scheduling	May 2002
Mike Geiger	Architectural Support for Natural I/O	May 2003
Amit Marathe	Architectural Support for Network I/O	May 2003
Aneesha Raines	Architectural Support for Secure Hashing	May 2003
Chris Weaver	Self-Tuning Digital Systems	Dec 2004
Curt Gomulinski	SimpleScalar/ARM System-Level Simulation	May 2003
Andrew Hamel	X86-based Performance Simulation	May 2004
Seokwoo Lee	Dynamic Timing Simulation	May 2005
Michael Minuth	Subthreshold Processor ISA Design	May 2006
Javin Olson	Subthreshold Microarchitecture Implementation	May 2006
Anna Reeves	Subthreshold Processor Physical Placement	May 2006
Mojtaba Mehrara	Brick and Mortar Silicon Processing	May 2006
Meghna Singhal	Testing Infrastructure for Subthreshold Designs	May 2007
Ellie Sager	Application-Specific Optimizations for Security	May 2007
David Flannery	Low-cost Dense Supercomputers	May 2007
Vincentius Robby	FPGA-based Server Platform	May 2009
Robert Perricone	Algorithm-Level Fault Tolerance	May 2011

D. Undergraduate Research Supervised

Student	Research Topic	Graduation Date
David Ramos	Distributed Program Verification Techniques	May 2009
Dan Zhang	FPGA-Based Fault Analysis Infrastructure	May 2009

E. Doctoral Thesis Committee Member

Student	Thesis Title/Topic	Graduation Date
Suhwan Kim	True Adiabatic Circuitry for High-Performance Low-Energy VLSI	January 2001
Krisztian Flautner	Automatic Monitoring for Interactive Performance and Power Reduction	April 2001
Hsien-Hsin Lee	Improving Energy and Performance of Data Cache Architectures by Exploiting Memory Reference Characteristics	June 2001
Glenn Reinman	Decoupled Fetch Architectures	June 2001 (at UC-San Diego)
Stevan Vlaovic	Modeling and Analysis of x86-Based Front-End Architectures	February 2002
Diana Keen	Novel Designs and Uses of Communication in Auxiliary Processing Systems	June 2002 (at UC-Davis)
Byron Cook	Structuring ISAs with Higher-order Functions	September 2002 (at OGI)
Xun Liu	Design methodologies for low power intellectual property based systems	April 2003
David Greene	Dynamic Fetch Optimization	May 2003
Paul Racunas	Reducing Load Latency through Memory Instruction Characterization	August 2003
Nam Sung Kim	Leakage Reduction Techniques for Embedded Memory Systems	February 2004
Steve Raasch	Processor Resource Allocation and its Impact on Performance in SMT Microprocessors	March 2004
Eric Halnor	Design and Applications of Indirection-Based Cache Structures	October 2004
Aseem Agarwal	Statistical Timing Analysis for Process Variation	March 2005
David Oehmke	Design and Applications of a Virtual Context Architecture	March 2005
Robert Senger	Design and Implementation of a Low Power Sensor Processor Platform	December 2005
Feng Gao	Gate-Level Techniques for Low Power and Reliable Circuit Design	June 2005

Student	Thesis Title/Topic	Graduation Date
Jeff Ringenberg	The Fast, Efficient, and Representative Benchmarking of Future Microarchitectures	May 2005
Jayakumaran Sivagnaname	SIO Circuit Techniques	May 2005
Kai-hui Chang	Function Design Error Diagnosis	May 2007
Hongtao Zhong	Architectural and Compiler Mechanisms for Accelerating Single Thread Applications	January 2008
Martha Mercaldi	Polymorphic Network Topologies	August 2008
Kevin Fan	Automatic Design of Efficient Application-Centric Architectures	August 2008
Smith Krishnaswamy	Density-Aware Physical Placement Strategies	August 2008
Zaher Andraus	Scalable Hardware Verification	October 2008
Ilya Wagner	Hardware Patching Technologies	October 2008
Alex Li (UIUC)	Resilient Design by Treating System Anomalies	June 2009
Brian Wyman	Polynomial Decomposition Over Rings	June 2010
Ken Zick	Physically-Adaptive Computing via Introspection and Self-Optimization in Reconfigurable Systems	October 2010
Shantanu Gupta	Adaptive Architectures for Robust and Configurable Performance	May 2011
Amir Hormati	Static and Dynamic Compilation of Streaming Languages	May 2011
Andrew DeOrio	Correct Communication in Multi-core Processors	December 2012
Amin Ansari	Overcoming Hard-Faults in High-Performance Microprocessors	June 2011
Mojtaba Mehrara	Compiler and Runtime Techniques for Automatic Parallelization of Sequential Applications	June 2011
Chien-Chih Yu	Probabilistic Analysis for Error Modeling, Reliability Estimation, and Robust Design	May 2012
John Sartori	Stochastic Processing	May 2012
Andrea Pellegrini	Adaptive Distributed Architectures for Future Semiconductor Technologies	August 2013

Student	Thesis Title/Topic	Graduation Date
Davoud Jamshidi	Accelerating Data Transfer for Throughput Processors	August 2016
Biruk Mammo	Reining in the Functional Veri?cation of Complex Processor Designs	December 2016
Shaizeen Aga	In-Memory Computation	December 2017 (expected)
Kaiyuan Yang	Circuit Techniques for Low-Power and Secure Internet-of-Things Systems	May 2018 (expected)

F. Research Grants

- Center for Future Architectures Research (C-FAR), for $28.7M (funded by STARnet), 1/2013-1/2018, I am Director of the center, which includes 26 faculty from 16 universities.
- Gigascale System Research Center, "Information Systems Platform Design", for $2.2M (Michigan funding), 11/2009-8/2012, I was Associate Director of the center, which included 44 faculty from 17 universities.
- Gigascale System Research Center, "Better Than Worst-Case Design Techniques", for $1.4M, 5/2003-5/2009, currently thrust leader for the Resilient System Design thrust, which includes 19 faculty from 12 universities.
- National Science Foundation, "Design Methodologies for Defect-Tolerant Computing Systems," $250,000 (jointly funded by Semiconductor Research Corporation), 5/2006-5/2009.
- National Science Foundation, "CSR---EHS: Ultra low cost system-level defect protection," $175,000, 1/2007-1/2010
- National Science Foundation, "ITR - (ASE) - (int + sim): Self-Correcting Techniques for Low Power Robust Computing," $1.2M., 5/2004-5/2008
- Intel Corporation, "Support for Dynamic Verification Research," $35,000, 9/2003.
- National Science Foundation, "Collaborative Research: ITR: Mobile Supercomputing," $310,000, 9/2003 - 5/3007.
- National Science Foundation, "Collaborative Research: Application Specific Architecture Customization and Co-Exploration," $150,000, 9/2003 - 5/2006.
- Sloan Fellowship, $40,000, 3/2003-3/2005
- National Science Foundation, **CAREER Award**, "New Directions in Speculative Execution", $390,000, 3/2001-3/2006.
- Intel Corporation: "Self-Tuned Digital Systems, Safe at Any Speed", $35,000, 8/2002.
- MARCO/DARPA, "Design for Verifiability: Solving the Functional Verification Bottleneck", $300,000, 5/2001-5/2006.
- Compaq Corporation: "New Directions in Microarchitecture Research", $10,000 gift, 8/2000-8/2001.
- National Science Foundation, "SimpleScalar: Industrial Strength Simulation Infrastructure", $1,160,000 total with $596,000 to PI Austin, Co-PIs: Profs. Burger and Keckler at UT-Austin, 1/2000 - 1/2004.
- DARPA PAC/C, "A Power Analyzer for Pocket Computers", $800,000 total, $330,000 to PI Austin, Co-PIs: Prof. Mudge (UM), Prof. Grunwald (UC-Boulder), 1/2000 - 12/2002.
- Compaq Corporation: "New Directions in Microarchitecture Research", $30,000 gift, 8/1999-8/2002.
- Intel Corporation: "Self-Tuned Digital Systems, Safe at Any Speed", $35,000 gift, 8/2001.

IV Teaching Experience

A. Graduate Courses Taught

Course Number	Title	Year	Class Size	Rating (our of 5)
UM EECS 598	Human-Inspired Computing	Winter 2008	15	4.88
UM EECS 570	Advanced Parallel Architectures	Fall 2008	34	4.82
		Fall 2006	22	4.05
UM EECS 573	Advanced Microarchitecture	Fall 2012	22	4.20
		Fall 2010	24	4.88
		Winter 2010	26	4.81
		Winter 2007	19	4.50
		Winter 2003	31	4.57
		Winter 2002	14	4.91
		Winter 2001	24	4.96
		Winter 2000	22	5.00
OGI CSE 521	Intro to Computer Architecture	Spring 1999	51	N/A
		Spring 1998	58	N/A
OGI CSE 582	Advanced Computer Architecture	Fall 1998	22	N/A
		Fall 1997	16	N/A
		Winter 1997	12	N/A
OGI CSE 511	Principles of Computer Design	Winter 1998	64	N/A
OGI CSE 513	Intro to Operating Systems	Spring 1997	54	N/A

B. Undergraduate Courses Taught

Course Number	Title	Year	Class Size	Rating (out of 5)
EECS 370	Computer Organization	Winter 2013	282	TBD
		Fall 2009	160	4.71
		Winter 2009	134	4.81
		Fall 2004	140	4.56
		Winter 2004	113	4.65
		Fall 2003	123	4.28
UM EECS 470	Computer Architecture	Winter 2011	35	4.75
		Fall 2002	98	4.45
		Fall 2001	96	4.72
		Fall 2000	86	4.94
		Fall 1999	68	4.83
UW CS 302	Intro to Programming	Fall 1992	26, 24	N/A
		Winter 1992	30, 28	N/A
		Fall 1991	32, 29	N/A

V Industry Experience

A. Work Experience

April 1996 - May 1999 Senior Computer Architect, Intel Corporation, Portland, OR

As a Senior Computer Architect in Intel's Microcomputer Research Labs, I led microarchitecture research efforts for future-generation microprocessors. Other responsibilities included management of associate researchers, computer system simulator design and implementation, and development of university relations.

January 1988 - April 1990 Associate Engineer, Xerox Corporation, Webster, NY

I was employed as an Associate Engineer with work in both hardware and software areas. My initial project involved the development of high-speed disk arrays (18 MB/sec) used in high-speed digital printers and copiers. Later, my work included the development of embedded processor simulation tools and design and development of an X server for the Xerox D-Machines.

Sept 1985 - August 1987 Cooperative Education Student, Eastman Kodak, Rochester, NY

I was employed as a Cooperative Education Student through the University of Wisconsin -- Madison Electrical Engineering Department.

B. Consulting

July 2005 - present Intempo Design LLC Ann Arbor, MI

Intempo Design LLC provides a variety of technical consulting services, ranging from intellectual property and patent litigation-related services to design services, including simulation model design and implementation.

July 1999 - present SimpleScalar LLC, Ann Arbor, MI

SimpleScalar LLC develops and markets technologies used to design, evaluate and verify computer system designs. SimpleScalar LLC also maintains and licenses the SimpleScalar tool set, a popular collection of microprocessor performance analysis tools.

July 2002 - July 2005 BitRaker Incorporated, San Diego, CA

BitRaker Incorporated produces tools and technologies for power-sensitive embedded system developers.

Sept 1990 - April 1996 Sage Software, Madison, WI

As the sole employee of Sage Software, I provided systems programming services to many companies in southern Wisconsin. My services included X server development, device driver development, and embedded systems programming.

VI Publications

A. Books Published

Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization (6th Edition), Pearson, 2012.

B. Book Chapters

Nam Sung Kim, Todd Austin, Trevor Mudge, and Dirk Grunwald, "Challenges for Architectural Level Power Modeling," in *Power Aware Computing*, eds. R. Melhem and R. Graybill, Kluwer Academic Publications, 2002.

C. Invited Articles

Todd Austin, Chris Weaver, Lisa Wu, and Rajeev Krishna, "Application Specific Architectures: A Recipe for Fast, Flexible and Power Efficient Designs," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES'01)*, November 2001.

D. Journal Articles

Mohit Tiwari and Todd Austin, "On Architectural Support for Systems Security," *IEEE Micro* Vol. 36 No. 5, Sept-Oct 2016.

Jason Clemons, Yingze Bao, Mohit Bagra, Todd Austin, and Silvio Savarese, "Scene Understanding for the Visually Impaired Using Visual Sonification by Visual Feature Analysis and Auditory Signatures," *Journal of Vision*, Vol. 12, No. 9, August 2012 (journal abstract).

Bo Zhai, Sanjay Pant, Leyla Nazhandali, Scott Hanson, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Todd Austin, Dennis Sylvester, and David Blaauw, "Energy-Efficient Subthreshold Processor Design," *IEEE Transactions on VLSI Systems*, August 2009.

K. Constantinides, O. Mutlu, V. Bertacco, and T. Austin, "A Flexible Software-Based Framework for Online Detection of Hardware Defects," *IEEE Transactions on Computers*, July 2009.

M. Mehrara and T. Austin, "Exploiting Selective Placement for Low-cost Memory Protection," *ACM Transactions on Architecture and Code Optimization*, Vol. 5, No. 3, November 2008.

T. Austin, V. Bertacco, S. Mahlke, and K. Cao, "Reliable Systems on Unreliable Fabrics," *IEEE Design and Test*, Vol. 25, No. 4, July 2008.

S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, D. Blaauw, "Exploring Variability and Performance in a Sub-200-mV Processor," *IEEE Journal of Solid State Circuits (JSSC)*, Vol. 43, No. 4, April 2008.

Ilya Wagner, Valeria Bertacco and Todd Austin, "Microprocessor Verification via Feedback-Adjusted Markov Models", *IEEE Transactions on Computer-aided Design (TCAD)*, Vol. 26, No. 6, June 2007.

Kypros Constantinides, Stephen Plaza, Jason Blome, Bin Zhang, Valeria Bertacco, Scott Mahlke, Todd Austin and Michael Orshansky, "Architecting a Reliable CMP Switch", *ACM Transactions on Architecture and Code Optimization (TACO)*, Vol. 4, No. 1, March 2007.

Shidhartha Das, David Roberts, Seokwoo Lee, Sanjay Pant, David Blaauw, Todd Austin, Krisztián Flautner, Trevor Mudge, "A Self-Tuning DVS Processor using Delay-Error Detection and Correction," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 41, No. 4, April 2006.

Dan Ernst, Nam Sung Kim, Shidhartha Das, Seokwoo Lee, David Blaauw, Todd Austin, Trevor Mudge, Krisztian Flautner, "Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation," *IEEE MICRO special issue on* **Top Picks From Microarchitecture Conferences of 2004**, Vol. 24, No. 6, March 2005.

T. Austin, D. Blaauw, S. Mahlke, T. Mudge, C. Chakrabati, and W. Wolf, "Mobile Supercomputers," IEEE Computer, Vol. 37, No. 5, May 2004.

Brad Calder, Todd Austin, and Tim Cusac, "Binary Instrumentation for Rapid Creation of Productivity Tools," in IQ: The Information Quarterly, Vol. 3, No. 4, November 2004.

Doug Burger, Todd Austin, and Stephen Keckler, "Recent extensions to the SimpleScalar tool suite," ACM SIGMETRICS Performance Evaluation Review, Vol. 31, No. 4, March 2004.

Todd Austin, David Blaauw, Trevor Mudge, and Krisztián Flautner, "Making Typical Silicon Matter with Razor", IEEE Computer, Vol. 37, No. 3, March 2004.

Shubhendu S. Mukherjee, Christopher T. Weaver, Joel Emer, Steven K. Reinhardt, and Todd Austin, "Measuring Architectural Vulnerability Factors", *IEEE MICRO special issue on* **Top Picks From Microarchitecture Conferences of 2003**, Vol. 23, No. 6, December 2003.

Nam Sung Kim, Todd Austin, David Blaauw, Trevor Mudge, Krisztián Flautner, Jie S. Hu, Mary Jane Irwin, Mahmut Kandemir, and Vijaykrishnan Narayanan, "Leakage Current: Moore's Law Meets Static Power", *IEEE Computer*, Vol. 36, No. 12, December 2003.

Todd Austin, Eric Larson, and Dan Ernst, "SimpleScalar: An Infrastructure for Computer System Modeling," *IEEE Computer*, Vol. 35, No. 2, February 2002.

Shubhendu S. Mukherjee, Sarita V. Adve, Todd Austin, Joel Emer, and Peter S. Magnusson, "Performance Simulation Tools," *IEEE Computer*, Vol. 35, No. 2, February 2002.

Todd Austin, "Design for Verification", *IEEE Design and Test*, Vol. 18, No. 6, September 2001.

Glenn Reinman, Brad Calder, and Todd Austin, "Optimizations Enabled by a Decoupled Front-End Architecture," *IEEE Transactions on Computers*, Vol. 50, No. 4, April 2001.

Todd Austin, "DIVA: A Dynamic Approach to Microprocessor Verification," *Journal of Instruction Level Parallelism*, Vol. 2, No. 1, May 2000.

Gary Tyson and Todd Austin, "Memory Renaming: Fast, Early, and Accurate Processing of Memory Communication," *International Journal of Parallel Programming*, Vol. 27, No. 5, August 1999.

Pradip Bose, Tom Conte, and Todd Austin, "Challenges in Processor Modeling and Validation: Current Practices and Future Needs," *IEEE Micro*, Vol. 19, No. 3, July/August 1999.

E. Refereed Conference Papers

Salessawi Ferede Yitbarek, Misiker Tadesse Aga, Reetuparna Das, and Todd Austin, "Cold Boot Attacks are Still Hot," in the 2017 IEEE Symposium on High Performance Computer Architecture (HPCA-2017), February 2017.

Kaiyuan Yang, Matthew Hicks, Qing Dong, Todd Austin, and Dennis Sylvester, "A2: Analog Malicious Hardware," in the *2016 IEEE Symposium on Security and Privacy (Oakland 2016)*, May 2016. (Won the **Distinguished Paper Award**.)

Zelalem Birhanu Aweke, Salessawi Ferede Yitbarek, Rui Qiao, Reetuparna Das, Matthew Hicks, Yossi Oren, and Todd Austin, "ANVIL: Software-Based Protection Against Next-Generation Rowhammer Attacks," in the *2016 Annual International Symposium on Architecture Support for Programming Languages and Operating Systems (ASPLOS-2016)*, April 2016.

Salessawi Ferede Yitbarek, Tao Yang, Reetuparna Das, and Todd Austin, "Exploring specialized near-memory processing for data intensive operations," in the 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE-2016), March 2016.

William Arthur, Sahil Madeka, Reetuparna Das, and Todd Austin, "Locking Down Insecure Indirection with Hardware-Based Control-Data Isolation," in the *2015 Annual International Symposium on Microarchitecture (MICRO-2015)*, December 2015.

William Arthur, Ben Mehne, Reetuparna Das, and Todd Austin, "Getting in Control of Your Control Flow with Control-Data Isolation," in the 2015 International Symposium on Code Generation and Optimization (CGO-2015), February 2015.

Jason Clemons, Andrea Pellegrini, Silvio Savarese and Todd Austin, "EVA: An Efficient VisionArchitecture for Mobile Systems," in the 2013 International Conference on Compilers Architecture and Synthesis for Embedded Systems (CASES 2013), October 2013.

William Arthur, Biruk Mammo, Ricardo Rodriguez, Todd Austin, and Valeria Bertacco, "Schnauzer: Scalable Profiling for Likely Security Bug Sites," in the 2013 International Symposium on Code Generation and Optimization (CGO-2013), February 2013.

A. Pellegrini, R. Smolinski, L. Chen, X. Fu, S. Hari, J. Jiang, S. Adve, T. Austin, and V. Bertacco, "CrashTest'ing SWAT: Accurate, Gate-Level Evaluation of Symptom-Based Resiliency Solutions," in the *2012 Design, Automation and Test in Europe Conference (DATE-2012)*, March 2012.

Joseph Greathouse, Hongyi Xin, Yixin Luo and Todd Austin, "A Case for Unlimited Watchpoints," in the ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2012), March 2012.

Jason Clemons, Sid Yingze Bao, Silvio Savarese, Todd Austin, and Vinay Sharma, "MVSS: Michigan Visual Sonification System," in the 2012 International Conference on Emerging Signal Processing Applications (ESPA-2012), January 2012.

Jason Clemons, Haishan Zhu, Silvio Savarese and Todd Austin, "MEVBench: A Mobile Computer Vision Benchmarking Suite," in the *2011 IEEE International Symposium on Workload Characterization (IISWC-2011)*, November 2011.

Jason Clemons, Andrew Jones, Robert Perricone, Silvio Savarese, and Todd M. Austin, "EFFEX: an embedded processor for computer vision based feature extraction," in the 2011 Design Automation Conference (DAC-2011), June 2011.

Joe Greathouse, Zhiqiang Ma, Matthew Frank, Ramesh Peri, and Todd Austin, "Demand-Driven Software Race Detection using Hardware Performance Counters," in the *2011 International Symposius on Computer Architecture (ISCA-2011)*, June 2011.

Joseph Greathouse, Chelsea LeBlanc, Valeria Bertacco and Todd Austin, "Highly Scalable Distributed Dataflow Analysis," in the *2011 International Symposium on Code Generation and Optimization (CGO-2011)*, April 2011.

Andrea Pellegrini, Rob Smolinski, Lei Chen, Xin Fu, Siva Kumar Sastry Hari, Junhao Jing, Sarita Adve, Todd Austin and Valeria Bertacco, "CrashTest'ing SWAT: Accurate, Gate-Level Evaluation of Symptom-Based Resiliency Solutions," in the *2011 Workshop on Silicon Errors in Logic and System Effects (SELSE-2011)*, March 2011.

Kypros Constantinides and Todd Austin, "Using Introspective Software-Based Testing for Post-Silicon Debug and Repair," in the *2010 IEEE/ACM Design Automation Conference (DAC-2010)*, June 2010.

Andrea Pellegrini, Valeria Bertacco and Todd Austin, "Fault-Based Attack of RSA Authentication," in the *2010 Design, Automation and Test in Europe Conference (DATE-2010)*, March 2010.

Joseph L. Greathouse, Ilya Wagner, David A. Ramos, Gautam Bhatnagar, Todd Austin, Valeria Bertacco and Seth Pettie, "Testudo: Heavyweight Security Analysis via Statistical Sampling," in the *41st Annual International Symposium on Microarchitecture (MICRO-41)*, November 2008.

Kypros Constantinides, Onur Mutlu, and Todd Austin, "Online Design Bug Detection: RTL Analysis, Flexible Mechanisms, and Evaluation," in the *41st Annual International Symposium on Microarchitecture (MICRO-41)*, November 2008.

Andrea Pellegrini, Kypros Constantinides, Dan Zhang, Shobana Sudhakar, Valeria Bertacco, and Todd Austin, "CrashTest: A Fast High-Fidelity FPGA-Based Resiliency Analysis Framework," in the *IEEE 26th International Conference on Computer Design (ICCD-2008)*, October 2008.

Kypros Constantinides, Valeria Bertacco, and Todd Austin, "Low-Cost Protection for SER Upsets and Silicon Defects," *TECHCON 2008*, September 2008.

Martha Mercaldi Kim, John D. Davis, Mark Oskin, and Todd Austin, "Polymorphic On-Chip Networks," in the *35th Annual International Symposium on Computer Architecture (ISCA-2008)*, June 2008.

Kypros Constantinides, Onur Mutlu, Todd Austin, and Valeria Bertacco, "Software-Based On-Line Detection of Hardware Defects: Mechanisms, Architectural Support, and Evaluation," in the 40th Annual International Symposium on Microarchitecture (MICRO-40), December 2007.

Scott Hanson, Bo Zhai, Mingoo Seok, Brian Cline, Kevin Zhou, Meghna Singhal, Michael Minuth, Javin Olson, Leyla Nazhandali, Todd Austin, Dennis Sylvester, David Blaauw, "Performance and variability optimization strategies in a sub-200mV, 3.5pJ/inst, 11nW subthreshold processor," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2007.

Martha Mercaldi, Mojtaba Mehrara, Mark Oskin and Todd Austin, "Architectural Implications of Brick and Mortar Silicon Manufacturing", in the *34th Annual International Symposium on Computer Architecture (ISCA-2007)*, June 2007.

Mojtaba Mehrara, Mona Attarian, Smitha Shyam, Kypros Constantinides, Valeria Bertacco, and Todd Austin, "Low-cost Protection for SER Upsets and Silicon Defects", in Design and Test in Europe (DATE-2007), March 2007.

Kypros Constantinides, Smitha Shyam, Sujay Phadke, Valeria Bertacco and Todd Austin, "Ultra Low-Cost Defect Protection for Microprocessor Pipelines", International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), October 2006.

Ilya Wagner, Valeria Bertacco and Todd Austin, "Shielding Against Design Flaws with Field Repairable Control Logic", IEEE/ACM Design Automation Conference (DAC), July 2006.

Bo Zhai, Leyla Nazhandali, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Sanjay Pant, David Blaauw, Todd Austin, "A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2006.

Shidhartha Das, David Roberts, Seokwoo Lee, Sanjay Pant, David Blaauw, Todd Austin, Trevor Mudge, Krisztián Flautner, "A Self-Tuning Dynamic Voltage Scaled Processor Using Delay-Error Detection and Correction," IEEE International Conference on Integrated Circuit Design & Technology (ICICDT), May 2006.

Kypros Constantinides, Jason Blome, Stephan Plaza, Bin Zhang, Valeria Bertacco, Scott Mahlke, Todd Austin, and Michael Orshansky, "BulletProof: A Defect Tolerant CMP Switch Architecture," in the 12th International Symposium on High-Performance Computer Architecture (HPCA-2006), February 2006.

Ilya Wagner, Valeria Bertacco, and Todd Austin, "Depth-Driven Verification of Simultaneous Interfaces," in the *2006 Asian South Pacific Design Automation Conference (ASPDAC-2006)*, January 2006.

Todd Austin and Valeria Bertacco, "Deployment of Better Than Worst-Case Design: Solutions and Needs," in the *2005 IEEE International Conference on Computer Design (ICCD-2005)*, October 2005.

Leyla Nazhandali, Michael Minuth, and Todd Austin, "SenseBench: Toward an Accurate Evaluation of Sensor Network Processors," in the *2005 IEEE International Symposium on Workload Characterization (IISWC-2005)*, October 2005.

Leyla Nazhandali, Michael Minuth, Bo Zhai, Javin Olson, Todd Austin and David Blaauw, "A Second-Generation Sensor Network Processor with Application-Driven Memory Optimizations and Out-of-Order Execution," in the *2005 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES-2005)*, September 2005.

Ilya Wagner, Valeria Bertacco, and Todd Austin, "StressTest: An Automatic Approach to Test Generation via Activity Monitors," in the *42nd Design Automation Conference (DAC-2005)*, June 2005.

Leyla Nazhandali, Bo Zhai, Ryan Helfand, Michael Minuth, Javin Olson, Sanjay Pant, Anna Reeves, Todd Austin, and David Blaauw, "Energy Optimization of Subthreshold-Voltage Sensor Processors," in the *32nd Annual International Symposium on Computer Architecture (ISCA-2005)*, June 2005.

S. Das, S. Pant, D. Roberts, S. Lee, D. Blaauw, T. Austin, T. Mudge, and K. Flautner, "A Self-Tuning DVS Processor Using Delay-Error Detection and Correction," in the *2005 Symposia on VLSI Technology and Circuits (VLSI-2005)*, June 2005.

David Roberts, Todd Austin, David Blaauw, Krisztian Flautner, and Trevor Mudge, "Error Analysis for the Support of Robust Voltage Scaling," in the *6th International Symposium on Quality Electronic Design (ISQED-2005)*, March 2005.

Himanshu Kaul, Dennis Sylvester, David Blaauw, Trevor Mudge, and Todd Austin, "DVS for On-Chip Bus Designs Based on Timing Error Correction," in the *2005 Design, Automation and Test in Europe Conference (DATE-2005)*, March 2005.

Todd Austin, Valeria Bertacco, David Blaauw, and Trevor Mudge, "Opportunities and Challenges for Better Than Worst-Case Design," in the *2005 Asian South Pacific Design Automation Conference (ASPDAC-2005)*, January 2005.

Brad Calder, Todd Austin, Don Yang, Timothy Sherwood, Suleyman Sair, David Newquist, Tim Cusac, "BitRaker Anvil: Binary Instrumentation for Rapid Creation of Simulation and Workload Analysis Tools," in the *2004 International Embedded Solutions Event (GPSx-2004)*, September 2004.

Rajeev Krishna, Scott Mahlke, and Todd Austin, "Memory System Design Space Exploration for Low-Power, Real-Time Speech Recognition," in the *2004 Int'l. Conference on Hardware/Software Codesign and System Synthesis*, September 2004.

Seokwoo Lee, Shidhartha Das, Toan Pham, Todd Austin, David Blaauw, and Trevor Mudge, "Reducing Pipeline Energy Demands with Local DVS and Dynamic Retiming," in the *2004 International Symposium on Low Power Electronics and Design (ISLPED-2004)*, August 2004.

Nam Sung Kim, Tae Ho Kgil, Valeria Bertacco, Todd Austin, and Trevor Mudge, "Microarchitectural Power Modeling Techniques for Deep Sub-Micron Microprocessors," in the *2004 International Symposium on Low Power Electronics and Design (ISLPED-2004)*, August 2004.

Todd Austin, "Designing Robust Microarchitectures," in the *41st Design Automation Conference (DAC-2004)*, June 2004.

Seokwoo Lee, Shidhartha Das, Valeria Bertacco, Todd Austin, David Blaauw, and Trevor Mudge, "Circuit-Aware Architectural Simulation," in the *41st Design Automation Conference (DAC-2004)*, June 2004.

Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Toan Pham, Rajeev Rao, Conrad Ziesler, David Blaauw, Todd Austin, Trevor Mudge, and Krisztián Flautner, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," in the *36th Annual International Symposium on Microarchitecture (MICRO-36)*, December 2003, received **Best Paper Award**.

Shubhendu S. Mukherjee, Christopher Weaver, Joel Emer, Steven K. Reinhardt, and Todd Austin, "A Systematic Methodology to Compute the Architectural Vulnerability Factors for a High-Performance Microprocessor," in the *36th Annual International Symposium on Microarchitecture (MICRO-36)*, December 2003.

Rajeev Krishna, Scott Mahlke, and Todd Austin, "Architectural Optimizations for Low-Power, Real-Time Speech Recognition," in the *2003 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES-2003)*, October 2003.

Eric Larson and Todd Austin, "High Coverage Detection of Input-Related Security Faults," in the *12th USENIX Security Symposium (SEC-2003)*, August 2003.

Dan Ernst, Andrew Hamel, and Todd Austin, "Cyclone: A Broadcast-Free Dynamic Instruction Scheduler with Selective Replay," in the *ACM/IEEE 30th Annual International Symposium on Computer Architecture (ISCA-2003)*, June 2003.

Dan Ernst and Todd Austin, "Efficient Dynamic Scheduling Through Tag Elimination," in the *ACM/IEEE 29th International Symposium on Computer Architecture (ISCA-2002)*, May 2002.

Glenn Reinman, Brad Calder and Todd Austin, "High Performance and Energy Efficient Serial Fetch Architecture," in the *4th International Symposium on High Performance Computing (ISHPC-IV)*, May 2002.

Chris Weaver, Kenneth C. Barr, Eric D. Marsman, Dan Ernst, and Todd Austin, "Performance Analysis Using Pipeline Visualization," in the *2001 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2001)*, June 2001.

Eric Larson, Saugata Chatterjee, and Todd Austin, "The MASE Microarchitecture Simulation Environment", in the *2001 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2001)*, June 2001.

Lisa Wu, Chris Weaver, and Todd Austin, "CryptoManiac: A Fast Flexible Architecture for Secure Communication", in the *ACM/IEEE 28th International Symposium on Computer Architecture (ISCA-2001)*, June 2001.

Chris Weaver and Todd Austin, "A Fault Tolerant Approach to Microprocessor Design" in the *IEEE International Conference on Dependable Systems and Networks (DSN-2001)*, June 2001.

Maher Mneimneh, Fadi Aloul, Saugata Chatterjee, Chris Weaver, Karem Sakallah, and Todd Austin, "Scalable Hybrid Verification of Complex Microprocessors", in the *38th Design Automation Conference (DAC-2001)*, June 2001.

Saugata Chatterjee, Chris Weaver, and Todd Austin, “Efficient Checker Processor Design”, in the *ACM/IEEE 33rd International Symposium on Microarchitecture (MICRO-33)*, December 2000.

Eric Larson and Todd Austin, “Compiler Controlled Value Prediction Using Branch Predictor Based Confidence”, in the *ACM/IEEE 33rd International Symposium on Microarchitecture (MICRO-33)*, December 2000.

Jerome Burke, John McDonald, and Todd Austin, “Architectural Support for Fast Symmetric-Key Cryptography,” in the *ACM/IEEE Ninth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-IX)*, October 2000.

Todd Austin, “DIVA: A Reliable Substrate for Deep Submicron Microarchitecture Design,” in the *ACM/IEEE 32nd Annual Symposium on Microarchitecture (MICRO-32)*, November 1999, received **Best Paper Award**.

Glenn Reinman, Brad Calder and Todd Austin, “Fetch Directed Instruction Prefetching,” in the *ACM/IEEE 32nd Annual Symposium on Microarchitecture (MICRO-32)*, November 1999.

Glenn Reinman, Brad Calder, Dean Tullsen, Gary Tyson, and Todd Austin, “Classifying Load and Store Instructions for Memory Renaming,” in the *ACM 13th International Conference on Supercomputing (ICS'99)*, August 1999.

Glenn Reinman, Todd Austin, and Brad Calder, “A Scalable Front-End Architecture for Fast Instruction Delivery,” in the *ACM/IEEE 26th Annual International Symposium on Computer Architecture (ISCA-26)*, May 1999.

Brad Calder, Simmi John, and Todd Austin, “Cache-Conscious Data Placement,” in the *ACM SIGPLAN 8th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VIII)*, October 1998.

Artur Klauser, Dirk Grunwald, Brad Calder and Todd Austin, “Dynamic Hammock Predication for Non-predicated Instruction Set Architectures,” in the *IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT '98)*, October 1998.

Gary S. Tyson and Todd M. Austin, “Improving the Accuracy and Performance of Memory Communication Through Renaming,” in the *ACM/IEEE 30th Annual Symposium on Microarchitecture (MICRO-30)*, December 1997.

Jude A. Rivers, Gary S. Tyson, Todd M. Austin and Edward S. Davidson, “On High-Bandwidth Data Cache Design for Multi-Issue Processors,” in the *ACM/IEEE 30th Annual Symposium on Microarchitecture (MICRO-30)*, December 1997.

Todd M. Austin and Gurindar S. Sohi, “High-Bandwidth Address Translation for Multiple-Issue Processors,” in the *ACM/IEEE 23rd Annual International Symposium on Computer Architecture (ISCA-23)*, May 1996.

Todd M. Austin and Gurindar S. Sohi, “Zero-Cycle Loads: Microarchitecture Support for Reducing Load Latency”, in the *ACM/IEEE 28th Annual International Symposium on Microarchitecture (MICRO-28)*, November 1995.

Todd M. Austin, Dionisios N. Pnevmatikatos, and Gurindar S. Sohi, "Streamlining Data Cache Access with Fast Address Calculation," in the *ACM/IEEE 22nd Annual International Symposium on Computer Architecture (ISCA-22)*, June 1995.

Todd M. Austin, Scott E. Breach, and Gurindar S. Sohi, "Efficient Detection of All Pointer and Array Access Errors," in the *ACM SIGPLAN 1994 Conference on Programming Language Design and Implementation (PLDI'94)*, June 1994.

Todd M. Austin and Gurindar S. Sohi, "Dynamic Dependency Analysis of Ordinary Programs," in the *ACM/IEEE 19th Annual International Symposium on Computer Architecture (ISCA-19)*, May 1992.

F. Refereed Workshop Papers

Joseph L. Greathouse and Todd Austin, "Position Paper: The Potential of Sampling for Dynamic Analysis," in the 6th ACM SIGPLAN Workshop on Programming Languages and Analysis for Security, June 2011.

Mojtaba Mehrara and Todd Austin, "Reliability-aware data placement for partial memory protection in embedded processors," in the Proceedings of the 2006 workshop on Memory system performance and correctness (MSPC'06), October 2006.

Kypros Constantinides, Stephen Plaza, Jason Blome, Bin Zhang, Valeria Bertacco, Scott Mahlke, Todd Austin, Michael Orshansky, "Assessing SEU Vulnerability via Circuit-Level Timing Analysis," in the 1st Workshop on Architectural Reliability (WAR-1), November 2005.

Jeff Ringenberg, David Oehmke, Todd Austin, and Trevor Mudge, "SimpleDSP: A Fast and Flexible DSP Processor Model," in the 5th Workshop on Media and Streaming Processors (MSP5) in the 36th Annual IEEE/ACM Symp. Microarchitecture (MICRO-36), Dec. 2003.

Dan Ernst and Todd Austin, "Practical Selective Replay for Reduced-Tag Schedulers," in the 2nd Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD-2003), held in conjunction with the 30th International Symposium on Computer Architecture (ISCA-30), June 2003.

Christopher Weaver, Eric Larson, and Todd Austin, "Effective support of simulation in computer architecture instruction," in the *2002 Workshop on Computer Architecture Education* (WCAE 2002), held in conjunction with the 29th International Symposium on Computer Architecture (ISCA-29), May 2002.

Nam Sung Kim, Todd Austin, and Trevor Mudge, "Low-Energy Data Cache Using Sign Compression and Cache Line Bisection," in the *ACM/IEEE 2nd Annual Workshop on Memory Performance Issues (WMPI 2002),* May 2002.

Rajeev Krishna, Todd Austin and Scott Mahlke, "Insights into the Memory Demands of Speech Recognition Algorithms," in the *ACM/IEEE 2nd Annual Workshop on Memory Performance Issues (WMPI 2002),* May 2002.

Matthew Guthaus, Jeff Ringenberg, Dan Ernst, Todd Austin, Trevor Mudge, and Richard Brown, "MiBench: A Free, Commercially Representative Embedded Benchmark Suite," in the *IEEE 4th Annual Workshop on Workload Characterization (WWC-4)*, December 2001.

Rajeev Krishna and Todd Austin, "Efficient Software Decoder Design", in the *2001 Workshop on Binary Translation,* September 2001.

G. Technical Reports

Chris Weaver, Fadi Gebara, Todd Austin, and Richard Brown, "Remora: A Dynamic Self-Tuning Processor," University of Michigan CSE Technical Report CSE-TR-460-02, July 2002.

Eric Larson, Saugata Chatterjee and Todd Austin, "MASE: A Novel Infrastructure for Detailed Microarchitectural Modeling," University of Michigan CSE Technical Report CSE-TR-442-01, July 2001.

Glenn Reinman, Brad Calder, and Todd Austin, "A Power Efficient Speculative Fetch Architecture," UC San Diego Technical Report CS2000-0657, June 2000.

Glenn Reinman, Brad Calder, and Todd Austin, "Building a Scalable Branch Predictor and an Instruction Prefetch Engine by Decoupling Branch Prediction from Instruction Fetch," UC San Diego Technical Report CS2000-0645, February 2000.

Glenn Reinman, Brad Calder, Dean Tullsen, Gary Tyson, and Todd Austin, "Profile-Guided Load Marking for Memory Renaming," University of California, San Diego, Technical Report UCSD-CS98-593, July 1998.

Douglas C. Burger and Todd M. Austin, "The SimpleScalar Tool Set, Version 2.0," UW Madison Computer Sciences Technical Report #1342, June 1997.

Doug Burger, Todd M. Austin and Steve Bennett, "Evaluating Future Microprocessors: The SimpleScalar Tool Set," UW Madison Technical Report #1308, July 1996.

Todd M. Austin, "Hardware and Software Mechanisms for Reducing Load Latency," Ph.D. Thesis, UW Madison Technical Report # 1311, April 1996.

Todd M. Austin, Scott E. Breach, and Gurindar S. Sohi, "Efficient Detection of All Pointer and Array Access Errors," UW Madison Technical Report #1197, December 1993.

Todd M. Austin, T.N. Vijaykumar, and Gurindar S. Sohi, "Knapsack: A Zero-Cycle Memory Hierarchy Component," UW Madison Technical Report #1189, November 1993.

Todd M. Austin and Gurindar S. Sohi, "Tetra: Evaluation of Serial Program Performance on Fine-Grain Parallel Processors," UW Madison Technical Report #1163, July 1993.

Todd M. Austin, "Exploiting Implicit Parallelism in SPARC Instruction Execution," M.S. Thesis, Rochester Institute of Technology, Wallace Library call number QA76.9.A73 A86 1990, August 1990.

H. Other Publications

Sharad Malik, Robert Rozploch, and Todd Austin, "The Gigascale Systems Research Center (GSRC) – Addressing the Information - System Platform Design Challenges for the Late- and Post-Silicon Era," DAC.com Knowledge Center Article, June 2010.

Douglas Burger, Todd Austin, and Steve Keckler, "Recent Extensions to the SimpleScalar Tool Suite," in the *ACM SIGMETRICS Performance Evaluation and Review*, March 2004.

Douglas C. Burger and Todd M. Austin, "The SimpleScalar Tool Set, Version 2.0," in the *Computer Architecture News*, Vol. 25, No. 3, June, 1997.

I. Patents Held

Kristian Flautner, Todd Austin, David Blaauw, Trevor Mudge, and David Bull, Error recovery within integrated circuit, U.S. Patent #9,164,842, issued October 20, 2015.

Kristian Flautner, Todd Austin, David Blaauw, Trevor Mudge, and David Bull, Error recovery within integrated circuit, U.S. Patent #8,650,470, issued February 11, 2014.

Kristian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error recover within processing stages of an integrated circuit, U.S. Patent #8,407,537, March 26, 2013.

Valeria Bertacco, Todd Austin, Smitha Shyam, Kypros Constantinides, Sujay Phadke, Microprocessor and method for detecting faults therein, U.S. Patent #8,341,473, issued December 25, 2012.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error recovery within processing stages of an integrated circuit, U.S. Patent #8,185,786, issued May 22, 2012.

David Blaauw, Shidhartha Das, and Todd Austin, Error recovery within processing stages of an integrated circuit, U.S. Patent #8,060,814, issued November 15, 2011.

Valeria Bertacco, Todd Austin, Smitha Shyam, Kypros Constantinides, and Sujay Phadke, Microprocessor and Method for Detecting Faults Therein, U.S. Patent #8,051,368, issued November 1, 2011.

Valeria Bertacco, Todd Austin, Smitha Shyam, Kypros Constantinides, and Sujay Phadke, Microprocessor and Method for Detecting Faults Therein, U.S. Patent #7,966,538, issued June 2019.

Krisztian Flautner, David Bull, Todd Austin, David Blaauw, and Trevor Mudge, Integrated circuit with error correction mechanisms to offset narrow tolerancing, U.S. Patent #7,701,240 issued April 2010.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error Detection and Recovery within Processing Stages of an Integrated Circuit, U.S. Patent #7,650,551 issued January 2010.

Martha Mercaldi Kim, Mark Oskin, John Davis, Todd Austin, and Mojtaba Mehrara, Customized Silicon Chips Produced Using Dynamically Configurable Polymorphic Network, U.S. Patent #7,598,766, issued October 2009.

Brad Calder, Todd Austin, Don Yang, and Timothy Sherwood, System and Method of Analyzing Interpreted Programs, U.S. Patent #7,475,394, issued January 2009.

Seokwoo Lee, and Todd Austin, Recovery From Errors in a Data Processing Apparatus, U.S. Patent #7,401,273, issued July 2008.

Dan Ernst and Todd Austin, Technique for Reduced-Tag Dynamic Scheduling, U.S. Patent #7,398,375, issued July 2008.

Trevor Mudge, Todd Austin, David Blaauw, and Krisztian Flautner, Systematic and Random Error Detection and Recovery within Processing Stages of an Integrated Circuit, U.S. Patent #7,337,356, issued February 2008.

Trevor Mudge, Todd Austin, David Blaauw, and Krisztian Flautner, Data Retention Latch Provision within Integrated Circuits, U.S. Patent #7,310,755, issued December 2007.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error Detection and Recovery within Processing Stages of an Integrated Circuit, U.S. Patent #7,278,080, issued October 2007.

Trevor Mudge, Todd Austin, David Blaauw, and Krisztian Flautner, Systematic and Random Error Detection and Recovery within Processing Stages of an Integrated Circuit, U.S. Patent #7,162,661, issued January 2007.

Todd Austin, David Blaauw, Trevor Mudge, Dennis Sylvester, and Krisztian Flautner, Memory system having fast and slow data reading mechanisms, U.S. Patent #7,072,229, issued July 2006.

Trevor Mudge, Todd Austin, David Blaauw, Dennis Sylvester, and Krisztian Flautner, Memory system having fast and slow data reading mechanisms, U.S. Patent #6,944,067, issued September 2005.

Todd Austin, Dionisios Pnevmatikatos, and Gurindar Sohi, Data Cache Fast Address Calculation System and Method, U.S. Patent Number 5,860,151, issued January 12, 1999.

Todd Austin, Method for Detecting Computer Memory Access Errors, U.S. Patent Number 5,644,709, issued July 1, 1997.

Donald Wegeng, Jeff Carter, Thomas Beaman, Gregory Sosinski, and Todd Austin, Image Data Transfer Architecture and Method for an Electronic Reprographic Machine, U.S. Patent Number 5,420,696, issued May 30, 1995.

J. Pending Patent Applications

Valeria Bertacco, Todd Austin, Smitha Shyam, Kypros Constantinides, and Sujay Phadke, Microprocessor and Method for Detecting Faults Therein, U.S. Patent Application #20120011422, submitted January 12, 2012.

Valeria Bertacco, Todd Austin, Smitha Shyam, Kypros Constantinides, and Sujay Phadke, Microprocessor and Method for Detecting Faults Therein, U.S. Patent Application #20110214014, submitted September 1, 2011.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error recover within processing stages of an integrated circuit, U.S. Patent Application #20110126051, submitted May 26, 2011.

Krisztian Flautner, Todd Austin, David Blaauw, Trevor Mudge, and David Bull, Error recovery within integrated circuit, U.S. Patent Application #20110107166, submitted May 5, 2011.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error recovery within processing stages of an integrated circuit, U.S. Patent Application #20110093737, submitted April 21, 2011.

Valeria Bertacco, Todd Austin, and Ilya Wagner, Field Repairable Logic, U.S. Patent Application #20090089615, submitted April 2009.

Martha Mercaldi Kim, Mark Oskin, John Davis, Todd Austin, and Mojtaba Mehrara, Customized Silicon Chips Produced Using Dynamically Configurable Polymorphic Network, U.S. Patent Application #20080164907, submitted July 2008.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error detection and recovery within processing stages of an integrated circuit, U.S. Patent Application #20070288798, submitted December 2007.

Krisztian Flautner, David Bull, Todd Austin, David Blaauw, and Trevor Mudge, Integrated circuit with error correction mechanisms to offset narrow tolerancing, U.S. Patent Application #20060200699, submitted September 2006.

Todd Austin, David Blaauw, Trevor Mudge, Dennis Sylvester, and Krisztian Flautner, Memory System Having Fast and Slow Data Reading Mechanisms, U.S. Patent Application #20060018171, filed January 2006.

Seokwoo Lee, and Todd Austin, Recovery From Errors in a Data Processing Apparatus, U.S. Patent Application #20050207521, filed September 2005.

Brad Calder, Todd Austin, Don Yang, and Timothy Sherwood, System and method of analyzing interpreted programs, U.S. Patent Application #20050125777, filed June 2005.

Trevor Mudge, Todd Austin, David Blaauw, and Krisztian Flautner, Systematic and random error detection and recovery within processing stages of an integrated circuit, U.S. Patent Application #20050022094, submitted January 2005.

Trevor Mudge, Todd Austin, David Blaauw, and Krisztian Flautner, Systematic and random error detection and recovery within processing stages of an integrated circuit, U.S. Patent Application #20040243893, submitted December 2004.

Trevor Mudge, Todd Austin, David Blaauw, and Krisztian Flautner, Data retention latch provision within integrated circuits, U.S. Patent Application #20040239397, issued December 2004.

Trevor Mudge, David Blaauw, Todd Austin, and Krisztian Flautner, Memory System Having Fast and Slow Data Reading Mechanisms, U.S. Patent Application #20040223386, filed November 2004.

Krisztian Flautner, Todd Austin, David Blaauw, and Trevor Mudge, Error Detection and Recovery within Processing Stages of an Integrated Circuit, U.S. Patent Application #20040199821, submitted October 2004.

Dan Ernst and Todd Austin, Technique for reduced-tag dynamic scheduling, U.S. Patent Application #20030191925, submitted October 2003.

K. Selected Press Reports

“New Center Focuses on Future Computers,” The Press-Enterprise, January 2013, http://markets.pe.com/pe/news/read?GUID=23316653

“DARPA shells out $194m for 'phase 6' of STARnet chip project,” The Register, January 2013, http://www.theregister.co.uk/2013/01/23/darpa_starnet_semiconductor_computing_funding

“STARnet Invests In Electronic Evolution”, Defense Electronics, February 2012, http://rfdesign.com/military_defense_electronics/starnet-invests-in-electronic-evolution-0213

“New $28M Center Will Develop Computers of 2025,” University of Michigan CSE News, http://www.ur.umich.edu/update/archives/130118/cfar

“Faculty Help Build Program, Relationship With Addis Ababa Institute of Technology in Ethiopia,” University of Michigan CSE News, August 2012, http://www.eecs.umich.edu/eecs/about/articles/2012/AAIT_program.html

“First a computer lab. Then an intercontinental collaboration.” Michigan Engineering LabLog, August 2011, http://lablog.engin.umich.edu/2011/08/first-computer-lab-then.html

“Programmable embedded processor optimizes feature-extraction algorithms”, Vision Systems Design, July 2011, http://www.vision-systems.com/articles/2011/07/programmable-embedded-processor-optimizes-feature-extraction-algorithms.html

“Researchers Find Way To Zap RSA Algorithm”, Slashdot.org, March 2010, http://linux.slashdot.org/story/10/03/04/1954259/Researchers-Find-Way-To-Zap-RSA-Algorithm

“1024-bit RSA encryption cracked by carefully starving CPU of electricity”, Engadget.com, March 2010, http://www.engadget.com/2010/03/09/1024-bit-rsa-encryption-cracked-by-carefully-starving-cpuof-ele

“Severe' OpenSSL vuln busts public key crypto”, The Register, March 2010, http://www.theregister.co.uk/2010/03/04/severe_openssl_vulnerability

“Researches Find RSA Security Hole”, Technorati, March 2010, http://technorati.com/technology/it/article/researches-find-rsa-security-hole

“Study finds weakness in security system”, United Press International, March 2010, http://www.upi.com/Science_News/2010/03/04/Study-finds-weakness-in-security-system/UPI-94551267718989

“Torturing the Secret out of a Secure Chip”, IEEE Spectrum, April 2010

“Chip, heal thyself”, Richard Goering, EETimes, 08/28/2006

“Self-healing Chips Advances Ensure Sustainability, Reliability of Computing Applications”, Kansas City infoZine, 07/27/2006

“Researchers Hope Self-Healing Semi-Conductor Chips Will Live Forever”, ASQ, 07/26/2006

“Michigan University selected to work on 'self-healing' chips”, Peter Clarke, EETimes, 07/25/2006

"Self-Healing Chips Will Live Forever, Researchers Hope", Natali delConte, ExtremeTech, 07/25/2006

"'Self-Healing' Chips to Result from SRC Teamwork with National Science Foundation, University of Michigan; Even the Weak Semiconductors Survive; Advances Ensure Sustainability, Reliability of Computing Applications", EDAcafe, 07/26/06

"Eluding your Buddies", The New York Times, February 14, 2002.

"From Enemies to Friends", Crain's Detroit Business, November 15, 2004.

VII Software Distributions

A. MEVBench Embedded Vision Benchmark Suite

The MEVBench Embedded Vision Benchmark Suite is a free benchmark suite that comprises a wide range of mobile computer vision processing activities. Described in "MEVBench: A Mobile Computer Vision Benchmarking Suite," by J. Clemons, H. Zhu, S. Savarese and T. Austin, in ISWC-2011, November 2011. Available from *http://www.eecs.umich.edu/mevbench.*

B. SenseBench Benchmark Suite

The SenseBench Benchmark Suite is a free benchmark suite that comprises a wide range of typical sensor processing activities. Described in "SenseBench: Toward an Accurate Evaluation of Sensor Network Processors," by L. Nazhandali, M. Minuth, and T. Austin, in the 2005 IEEE International Symposium on Workload Characterization (IISWC-2005), October 2005.

C. SimpleScalar Tool Set

The SimpleScalar tools are a collection of compiler, assembler, linker and simulator tools for SimpleScalar PISA and other popular architectures. The tool set provides researchers and educators with an easily extensible, portable, high-performance test bed for computer system design or instruction. The SimpleScalar tool set is in use at more than 75 universities and research centers, and it has been the simulation infrastructure used in more than 125 systems courses and 6,500 refereed publications. In 2007, almost 3 out of 10 papers published in top computer architecture conferences used the SimpleScalar tools to evaluate their designs. SimpleScalar is available at *http://www.simplescalar.com*.

D. The MiBench Embedded Benchmark Suite

The MiBench Benchmark Suite is a free, commercially representative embedded benchmark suite. Described in "MiBench: A free, commercially representative embedded benchmark suite," by M. R. Guthaus, J. Ringenberg, D. Ernst, T. Austin, T. Mudge, R. Brown, in the IEEE 4th Annual Workshop on Workload Characterization, Austin, TX, December 2001.

E. The Safe C Compiler

A C-to-C compiler which implements the extended pointer and array access semantics needed to provide efficient, reliable and immediate detection of memory access errors in unbridled C codes. Described in University of Wisconsin TR #1197.

F. Pointer-Intensive Benchmark Suite

A collection of six non-trivial pointer-intensive programs. The programs are described in University of Wisconsin TR #1197. Distribution is available from: http://www.cs.wisc.edu/~austin/ptr-dist.html.

G. Tetra Trace Analysis Tool

A multi-platform trace analysis tool for gauging parallelism in serial programs. Described and documented in University of Wisconsin TR #1163. Distribution is available from: http://www.cs.wisc.edu/~austin/tetra.html.

VIII Scholarly Addresses

A. Distinguished Lectures and Keynote Addresses

Preparing for a Post Moore's Law World
Distinguished Bradley Lecture at Virginia Tech University, November 2016.

Preparing for a Post Moore's Law World
Keynote Address at the 2015 International Symposium on Microarchitecture (MICRO-2015), December 2015.

Ending the Tyranny of Amdahl's Law
Keynote Address at the 2015 International Conference on Computer Design (ICCD-2015), October 2015.

On the Rules of Low Power Design (and How to Break Them)
Distinguished Lecture at Michigan Technilogical University, October 2015.

Bridging the Moore's Law Performance Gap with Innovation Scaling
Keynote Address at the 2015 International Conference on Performance Engineering (ICPE-2015), February 2015.

On the Rules of Robust Design (and Why You Should Break Them)
Distinguished Lecture at Duke University, April 2013.

The Upside of the Reliability Downtrend
Keynote Address of the Workshop on Resilient Architectures (WRA-2010), Atlanta, GA, December 2010.

On the Rules of Low Power Design (and How to Break Them)
Keynote Address of the International Symposium on Low Power Electronics and Design (ISLPED-2008), August 2008.

Why Tools Matter
Keynote Address of the International Symposium on Performance Analysis of Software and Systems (ISPASS-2008), April 2008.

New Directions in Speculative Execution
Distinguished Lecture at University of Virginia, Invited lecture as part of the Top Gun lecture series 2000-2001, Charlottesville, VA, March 2001.

B. Panel Presentations

Top Five Things about Resilient System Design that You Might Not Know
at the Verification and Test Symposium (VTS-2015), Napa, CA, April 2015.

Toward Affordable Customization
at the 2013 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES-2013), October 2013.

EDA 2.0
at the 2013 Design Automation Conference (DAC-2013), June 2013.

Embedding High Performance Computing:An Opportunity and A Challenge
at the 2013 Design, Automation and Test in Europe Conference (DATE-2013), March 2013.

Application-Driven Architectures: Future or Fantasy
at the Gigascale Systems Research Center Workshop on Application-Driven Architectural Design, July 2012

X-Stack Energy Optimization: Fact or Fiction
at the Workshop on Energy-Secure System Architectures (ESSA 2012), June 2012.

La Dolce Vita: Lamborghini, Dom Perignon, and Heterogeneous Computing
at the International Conference on Computer Design (ICCD-2011), October 2011.

Toward 10x Improvement in Data Center Efficiency
at the International Symposium on Low Power Electronics and Design (ISLPED-2008), August 2008.

C. Invited Talks

Preparing for a Post Moore's Law World
• ARM Ltd., Austin, TX, June 2016.

A Subtractive Approach to Hardware Security Research
• Intel Corporation, Portland, OR, April 2016.
• Texas Instruments, Dallas, TX, January 2016.

Mastering the Fine Art of the Pivot
• NOPE Workshop, Honolulu, HI, December 2015.

An Overview of the Center for Future Architectures Research (C-FAR)
• GOMACTech Conference, St. Louis, MO, April 2015.

Getting in Control of Your Control Flow: New Thinking in Secure System Design
• Texas Instruments, Dallas, TX, January 2016.
• IBM Corporation, Yorktown, NY, January 2014.

On the Rules of Low Power Design (and Why You Should Break Them)
• Arizona State University, Tempe, AZ, February 2015.
• Boston University, Boston, MA, October 2013.
• University of Washington, Seattle, WA, April 2013.
• UC-San Diego, San Diego, CA, April 2013.
• UC-Santa Barbara, Santa Barbara, CA, March 2013.

C-FAR: The Center for Future Architectures Research
• Texas Instruments, Dallas, TX, January 2016.
• GOMACTech Conference Panel, St. Louis, MO, March 2015.
• GLOBALFOUNDRIES, Santa Clara, CA, February 2015.
• IBM Corporation, Yorktown, NY, January 2014.
• Intel Corporation, Hudson, MA, October 2013.
• IBM Corporation, e-seminar, October 2013.

• DARPA, Arlington, VA, September 2013.
• Intel Corporation, Portland, OR, September 2013.
• Intel Corporation, e-seminar, August 2013.

Torturing OpenSSL
• University of California at Berkeley, Berkeley, CA, October 2012.

EFFEX: Next-Generation Platforms for Mobile Vision Computing
• University of California at Berkeley, Berkeley, CA, November 2011.
• Texas Instruments, Dallas, TX, August 2011.

Squash Your Security Bugs, Before They Squash You!
• FCRP Systems E-Seminar Series, December 2010.
• Microsoft Corporation, Seattle WA, November 2010.
• UC-Santa Barbara, Santa Barbara, CA, November 2010.
• Intel Corporation, Haifa, Israel, October 2010.

The Upside of the Reliability Downtrend
• International Workshop on Logic Synthesis (IWLS-2010), Irvine, CA, Jun. 2010.

Resilient Systems... New thinking in robust design
• Texas Instruments Corporation, Dallas, TX, June 2010.
• Xilinx Corporation, San Jose, CA, June 2010.

Using Introspective Software-Based Testing for Post-Silicon Debug and Repair
• Design Automation Conference (DAC-2010), Anaheim, CA, Jun. 2010.
• Asia and South Pacific Design Automation Conf. (ASPDAC-2010), Taipei, Taiwan, Jan. 2010.

On the Rules of Robust Design (and Why You Should Break Them)
• Florida State University, Tallahassee, FL, June 2011.
• University of Washington, Seattle, WA, November 2010.
• Princeton University, Princeton, NJ, April 2009.

On the Rules of Low Power Design (and How to Break Them)
• Georgia Technical University (GaTech), Atlanta, GA, December 2008.
• University of Illinois at Urbana-Champaign, Urbana, IL, October 2008.

Why Tools Matter
• UC-Santa Barbara, Santa Barbara, CA, October 2013.
• Technion University, Haifa, Israel, October 2010.
• University of Florida, Gainesville, FL, February 2009.
• University of Michigan, Ann Arbor, MI, May 2008.

Chip, Heal Thyself
• Chalmers University, Gothenburg, Sweden, October 2007.
• Intel Corporation, Boston, MA, October 2006.

Sidestepping Performance Bottlenecks with Better Than Worst-Case Design
• Microsoft Corporation, November 2006.
• Singapore National University, November 2006.
• SBCCI 2006, Brazil, August 2006.

• University of California - Santa Barbara, November 2005.
• GSRC E-Workshop, Ann Arbor, MI, April 2005.
• AMD, Santa Clara, CA, April 2005.

Deployment of Better Than Worst-Case Design: Solutions and Needs
• 2005 IEEE International Conference on Computer Design (ICCD-2005), October 2005.

Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation
• Sun Microsystems, Mountain View, CA, October 2003.
• KAIST, Daejeon, Korea, October 2003.
• Samsung Corporation, Suwon, Korea, October 2003.
• Intel Corporation, Santa Clara, CA, September 2003.

Building Buggy Chips - That Work!
• IBM Watson Research Center, Yorktown, NY, December 2002.
• University of California - Berkeley, CA, December 2002.
• University of Texas, Austin, TX, November 2001.
• Intel Corporation, Hillsboro, OR, March 2001.
• University of Washington, Seattle, WA, March 2001.
• University of Wisconsin, Madison, WI, March 2001.
• Carnegie Mellon University, Pittsburgh, PA, April 2000.

CryptoManiac: Application Specific Architectures for Cryptography
• Intel Corporation, Portland, OR, August 2002.
• University of Washington, Seattle, WA, March 2001.

New Directions in Speculative Execution
• Intel Corporation, Santa Clara, CA, May 2000.
• Compaq Computer Corporation, Boston, MA, May 2000.
• Stanford University, Palo Alto, CA, April 2000.
• Intel Corporation, Hillsboro, OR, February 2000.
• IBM Watson Research Center, Yorktown, NY, December 1999.
• Carnegie Mellon University, Pittsburgh, PA, October 1999.
• Northwestern University, Evanston, IL, September 1999.

Hardware Modeling Infrastructure: The SimpleScalar Experience
• UW/MSR Summer Institute, Seattle, WA, August 2000.

Scaling the Memory Wall: Technologies for Fast Memory Communication
• U-Colorado Department of Electrical Engineering, Boulder, CO, February 1999.
• U-Minnesota Electrical and Computer Engineering, Minneapolis, MN, January 1999.
• U-Michigan Electrical Engineering and Computer Science, Ann Arbor, MI, January 1999.

Memory Renaming: Dynamic Scheduling for Memory
• U-Michigan Computer Science and Engineering, Ann Arbor, MI, November 1997.

The SimpleScalar Architectural Research Tool Set
• KAIST, Daejeon, Korea, October 2003.
• Samsung Corporation, Suwon, Korea, October 2003.
• Portland State University Department of Electrical Engineering, Portland, OR, April 1997.

• U-Michigan Computer Science and Engineering, Ann Arbor, MI, April 1997.
• U-Minnesota Department of Computer Sciences, Minneapolis, MN, February 1997.
• Technion Department of Electrical Engineering, Haifa, Israel, December 1996.
• Intel Israel, Haifa, Israel, December 1996.
• Oregon State University Dept.of Electrical Engineering, Corvallis, OR, November 1996.
• Oregon Center for Advanced Technology Education, Hillsboro, OR, November 1996.

Cache-Conscious Data Placement
• UC-San Diego Department of Computer Sciences, San Diego, CA, April 1997.
• U-Minnesota Department of Computer Sciences, Minneapolis, MN, February 1997.
• UW-Madison Department of Computer Sciences, Madison, WI, February 1997.
• Technion Department of Electrical Engineering, Haifa, Israel, December 1996.
• Intel Israel, Haifa, Israel, December 1996.
• UC-Riverside Department of Computer Sciences, Riverside, CA, November 1996.

Hardware and Software Mechanisms for Reducing Load Latency
• Intel Santa Clara, Santa Clara, CA, October 1995.
• Intel Oregon, Hillsboro, OR, October 1995.
• Cyrix Corporation, Houston, TX, November 1995.
• IBM Watson Research Center, Yorktown, NY, December 1995.
• IBM Austin Research Labs, Austin, TX, December 1995.

Efficient and Reliable Detection of All Memory Access Errors
• Microsoft Research, Redmond, WA, December 1995.
• IBM Corporation, Rochester, MN, October 1994.
• Pure Software, Inc., Sunnyvale, CA, March 1994.

D. Conference and Workshop Presentations

"DVS for On-Chip Bus Designs Based on Timing Error Correction," in the *2005 Design, Automation and Test in Europe Conference (DATE-2005)*, March 2005.

"Opportunities and Challenges for Better Than Worst-Case Design," in the *2005 Asian South Pacific Design Automation Conference (ASPDAC-2005)*, January 2005.

"Self-Correcting Microprocessors", Workshop on Reliable System Design from Unreliable Components, Berkeley, CA, November 2002.

"Application Specific Architectures: A Recipe for Fast, Flexible and Power Efficient Designs," CASES'01, Atlanta, November 2001.

"Architectural Support for Fast Symmetric-Key Cryptograph," ASPLOS-IX, November 2000.

"DIVA: A Reliable Substrate for Deep Submicron Microarchitecture Design," MICRO-32, Haifa, Israel, November 1999, received **Best Presentation Award**.

"Performance Analysis Tools for PC-based Systems," CAECW'98, First Workshop on Computer Architecture Evaluation Using Commercial Workloads, Las Vegas, NV, February 1998.

"The SimpleScalar Tool Set as an Instructional Tool: Experiences and Future Directions," WCAE'98, Fourth Workshop on Computer Architecture Education, Las Vegas, NV, Jan 1998.

"High-Bandwidth Address Translation for Multiple-Issue Processors," IEEE/ACM ISCA-23, Philadelphia, Pennsylvania, June 1996.

"Zero-Cycle Loads: Microarchitecture Support for Reducing Load Latency," MICRO-28, Ann Arbor, MI, November 1995.

"The SimpleScalar Architectural Research Tool Set," PAID-I Workshop, IEEE/ACM ISCA-22, Santa Margherita Ligure, Italy, June 1995.

"Streamlining Data Cache Access with Fast Address Calculation," IEEE/ACM ISCA-22, Santa Margherita Ligure, Italy, June 1995.

"Efficient Detection of Pointer and Array Access Errors," ACM PLDI '94 Conference, Orlando, Florida, June 1994.

"Dynamic Dependency Analysis of Ordinary Programs," IEEE/ACM ISCA-19, Queensland, Australia, May 1992.

E. Tutorials Given

"Building Secure Hardware and Software," at the 2015 Eleventh International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES-2015), Fuiggi, Italy, July 2015.

"Building Secure Hardware and Software," at the 2015 Design Automation Conference (DAC-2015), with Jin Yang of Intel Corporation, June 2015.

"A (Mostly) Gentle Introduction to Computer Security," 2012 linux.conf.au Conference (LCA 2012), January 2012.

"Building Secure Hardware and Software," at the 2011 Seventh International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES-2011), Fuiggi, Italy, July 2011.

"Robust Low Power Computing in the Nanoscale Era," at the SBCCI 2006, Ouro Preto, Brazil, August 2006.

"Sidestepping Performance and Design Crises with Better Than Worst-Case Design," held in conjunction with the *2005 Design, Automation and Test in Europe Conference (DATE-2005)*, March 2005.

"Low-Power Robust Design," with David Blaauw, Krisztián Flautner, Nam Sung Kim, Trevor Mudge, and Dennis Sylvester, held in conjunction with the 37th International Symposium on Microarchitecture (MICRO-37), December 2004.

"Designing Robust Microarchitectures," with Ravi Iyer (UIUC), Nanni De Micheli (Stanford), and Naresh Shanbhag (UIUC), held in conjunction with the 2004 41st Design Automation Conference, June 2004.

"SimpleScalar Version 4.0 Release Tutorial," with Doug Burger and Trevor Mudge, held in conjunction with the 34th International Symposium on Microarchitecture (MICRO-34), December 2001.

"SimpleScalar Tool Set Tutorial," with Doug Burger, held in conjunction with the 30th International Symposium on Microarchitecture (MICRO-30), December 1997.

IX Professional Activities

A. Center Leadership Roles

- Director - The Center for Future Architectures Research (C-FAR), funded by STARnet, 2013-present.
- Associate Director - Gigascale Systems Research Center (GSRC), funded by MARCO, 2009-2012.
- Application Driver Theme Leader - Gigascale Systems Research Center (GSRC), funded by MARCO, 2009-2012.
- Robust Design Theme Leader - Gigascale Systems Research Center (GSRC), funded by MARCO, 2006-2009.

B. Professional Societies

- Member of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

C. Editor, Co-Editor, and Associate Editor Positions

- Co-guest Editor, IEEE MICRO Magazine, Special Issue on Hardware Security.Fall 2015
- Associate Editor, ACM Transactions on Architecture and Code Optimization (TACO), December 2002 - January 2007.
- Co-guest editor, IEEE Computer special issue on High Performance Computer System Simulation, February 2002.
- Co-guest editor, IEEE MICRO special issue on Performance Analysis and its Impact on Design, July/August 1999.

D. Panels

- Panel Member, NSF Computer Systems Architecture Panel, May 2015.
- Special Session Moderator, “Intelligent Compilation for Emulation and Acceleration,” at the 2013 International Conference on Computer-Aided Design (ICCAD-2013), November 2013.
- Panel Co-organizer and Moderator, “Hackers and Attackers: How Safe is Your Embedded Design?” at the 2011 Design Automation Conference (DAC-2011), June 2011.
- Panel Member and Co-organizer, Computing Community Consortium (CCC) Visioning Study on Cross-Layer Reliability, July 2009-2011.
- Panel Member, NSF Computer Systems Architecture Panel, April 2008.
- Panel Member, NSF Computer Systems Architecture Panel, August 2007.
- Panel Member, NSF Computer Systems Architecture Panel, October 2003.
- Panel Member, DARPA ISAT panel member, The Last Classical Computer program, June 2001.

E. Conference, Special Issue, and Workshop Organization

- Program Committee member, 2017 Design Automation Conference (DAC-2017), Hardware Security track, June 2017.
- Program Committee member, 2017 IEEE MICRO Top Picks Selection Committee, December 2016.
- Special Session Moderator, 2016 Design Automation Conference (DAC-2016), Special session: "The Rise of Heterogenous Architectures: from Embedded Systems to Data Centers", June 2016.
- Program Committee member, 2016 Design Automation Conference (DAC-2016), H/W and S/W System Co-Design track, June 2016.
- Track Co-Chair, 2015 Design and Test in Europe (DATE-2015, Microarchitecture Track), March 2015.
- Program Committee member, 2014 IEEE International Symposium on Computer Architecture (ISCA-2014), June 2014.
- Track Co-Chair, 2014 Design and Test in Europe (DATE-2014, Microarchitecture Track), March 2014.
- Program Committee member, 2014 International Symposium on High-Performance Computer Architecture (HPCA-2014), February 2014.
- Program Committee member, 2013 International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-2013), March 2013.
- Program Committee member, 2013 Design and Test in Europe (DATE-2013, Microarchitecture Track), March 2013.
- Program Committee member, 2013 International Symposium on Compiler Generation and Optimization (CGO-2013), February 2013.
- Program Committee member, 2012 International Symposium on Microarchitecture (MICRO-2012), December 2012.
- Program Committee member, 2012 Design and Test in Europe (DATE-2012, Microarchitecture Track), March 2012.
- Program Committee member, 2011 IEEE/ACM International Symposium on Microarchitecture (MICRO-44), December 2011.
- Program Committee member, 2011 Design Automation Conference (DAC), Technical Panels track, June 2011.
- Steering Committee member, International Symposium on Performance Analysis of Software and Systems (ISPASS), 2009-2011
- Program Committee member, 2011 Design and Test in Europe (DATE-2011, Microarchitecture Track), March 2011.
- Panel Co-organizer, 2010 Design Automation Conference (DAC), Technical Panel on "What Input Language is the Best Choice for High-Level Synthesis?", June 2010.
- Program Committee member, 2010 Design Automation Conference (DAC), Technical Panels track, June 2010.

- Program Committee member, 2010 IEEE International Symposium on Computer Architecture (ISCA-2010), June 2010.
- Program Committee member, 2010 Design and Test in Europe (DATE-2010, Microarchitecture Track), March 2010.
- Session Chair, 2010 Design and Test in Europe (DATE-2010), session on "Architectural Techniques for Robust Design", March 2010.
- Session Co-Chair, Session on "Wild and Crazy Ideas (WACI)", IEEE/ACM 2009 Design Automation Conference (DAC), July 2009.
- Panel Moderator, Session on "Computation in the Post-Turing Era", IEEE/ACM 2009 Design Automation Conference (DAC), July 2009.
- Session Chair, 2009 Design and Test in Europe (DATE-2009), Session on "Novel Microarchitecture and Simulation Techniques", April 2009.
- Session Chair, 2009 International Symposium on High-Performance Computer Architecture (HPCA-2009), Session on "Reliability", February 2009.
- Program Committee member, 2010 International Symposium on High-Performance Computer Architecture (HPCA-2010), February 2010.
- Program Committee member, 2009 IEEE International Symposium on Computer Architecture (ISCA-2009), June 2009.
- General co-chair, 2009 IEEE International Symposium on Performance Analysis of Software and Systems (ISPASS-2009), March 2009.
- Program Committee member, 2009 Design and Test in Europe (DATE-2009, Microarchitecture Track), March 2009.
- Program Committee member, 2009 International Symposium on High-Performance Computer Architecture (HPCA-2009), February 2009.
- Program Committee member, 2008 IEEE/ACM International Symposium on Microarchitecture (MICRO-41), November 2008.
- Program Committee member, 2008 Workshop on Dependable Architecture (WDA-2008), held in conjunction with the IEEE/ACM International Symposium on Microarchitecture (MICRO-41), November 2008.
- Program Committee member, 2008 Workshop on Compiler and Architectural Techniques (CATARS), held in conjunction with the IEEE International Conference on Dependable Systems and Networks (DSN), June 2008.
- Program Committee member, 2008 IEEE Micro: Micro's Top Picks from Computer Architecture Conferences, July 2008.
- Chair of organizing committee, 2008 Design and Test in Europe (DATE-2008, Microarchitecture Track), March 2008.
- Program Committee member, 2007 IEEE International Symposium on Computer Architecture (ISCA-2007), June 2007.
- Chair of organizing committee, 2007 Design and Test in Europe (DATE-2007, Microarchitecture Track), March 2007.
- Program Committee member, 2006 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2006), March 2006.

- Chair of organizing committee, 2006 Design and Test in Europe (DATE-2006, Microarchitecture Track), March 2006.
- Program Committee member, 2006 Workshop on Introspective Architectures (WISA-2006) held in conjunction with HPCA-12, February 2006.
- Program Committee member, 2006 ASPLOS Wild and Crazy Idea Session (WACI-2006), October 2006.
- Steering Committee member, 2005 CRA Grand Challenges Conference in Computer Architecture, December 2005.
- Program Committee member, The 38th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-38), November 2005.
- Program Committee member, The Sixth Workshop on Complexity-Effective Design (WCED'05), May 2005.
- Co-chair of organizing committee, 2005 Design and Test in Europe (DATE-2005, Microarchitecture Track), March 2005.
- Session Chair (Day #1 Recap and Open Discussion), Workshop on the System Effects of Logic Soft Errors (SELSE-1), April 2005.
- Program Committee member, The 2005 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2004), March 2005.
- Program Committee member, The 11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XI), October 2004.
- Program Committee member, The 31st International Symposium on Computer Architecture (ISCA-2004), June 2004.
- Program Committee member, The Second ACM SIGPLAN Workshop on Memory System Performance (MSP 2004), June 2004.
- Session Chair (Power and Energy Efficient Architectures), The 36th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-36), November 2003.
- Program Committee member, The 36th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-36), November 2003.
- Program Committee member, The 2003 ACM SIGPLAN Workshop on Interpreters, Virtual Machines and Emulators (IVME-2003), June 2003.
- Program Committee member, The 30th International Symposium on Computer Architecture (ISCA-2003), June 2003.
- Program Committee member, 2003 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2003), March 2003.
- Program Committee member, The Ninth International Symposium on High Performance Computer Architecture (HPCA-9), February 2003.
- Program Committee member, The 35th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-35), November 2002.
- Program Committee member, 2002 International Conference on Computer Design (ICCD'02), October 2002.
- Program Committee member, Workshop on Embedded System Codesign (ESCODES’02), September 24, 2002.

- Program Committee member, The Third Workshop on Complexity-Effective Design (WCED'02), May 2002.
- Program Committee member, The Sixth Workshop on Interaction Between Compilers and Computer Architectures (INTERACT-6), March 2002.
- Program Committee member, International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES-2001), November 2001.
- Program Committee member, 2001 International Conference on Computer Design (ICCD'01), October 2001.
- Program Committee member, The Second Workshop on Complexity-Effective Design (WCED'01), June 2001.
- Program Committee member, International Symposium on Performance Analysis of Systems and Software (ISPASS-2001), April 2001.
- Program Committee member, The Fifth Workshop on Interaction Between Compilers and Computer Architectures (INTERACT-5), March 2001.
- Program Committee member, 2000 International Conference on Computer Design (ICCD'00), October 2000.
- Program Committee member, The First Workshop on Complexity-Effective Design (WCED'00), June 2000.
- Program Committee member, The Fourth Workshop on Interaction Between Compilers and Computer Architectures (INTERACT-4), March 2000.
- Program Committee member, The 27th International Symposium on Computer Architecture (ISCA-2000), June 2000.
- Program Committee member, International Symposium on Performance Analysis of Systems and Software (ISPASS-2000), April 2000.
- Session Chair (Profile-Guided Optimizations), Second Workshop on Feedback-Directed Optimization, November 1999.
- Program Committee member, Second Workshop on Feedback-Directed Optimization, November 1999.
- Workshop chair, The 32nd International Symposium on Microarchitecture (MICRO-32), November 1999.
- Program Committee member, 1999 International Conference on Computer Design (ICCD'99), October 1999.
- Co-chair of organizing committee, Fifth Workshop on Performance Analysis and its Impact on Design (PAID-V), August 1999.
- Program Committee member, The 2nd Workshop on Multi-Threaded Execution, Architecture and Compilation (MTEAC'99), January 1999.
- Session Chair (Compilers I), The 31st International Symposium on Microarchitecture (MICRO-31), December 1998.
- Program Committee member, The 31st International Symposium on Microarchitecture (MICRO-31), November 1998.
- Co-chair of organizing committee, First Workshop on PC-based System Performance and Analysis, Held in conjunction with ASPLOS-VIII, October 1998.

- Program Committee member, The 25th International Symposium on Computer Architecture (ISCA-25), June 1998.

F. Refereeing and Reviewing

- Reviewer: McGraw-Hill Publishers, Morgan Kaufmann Publishers, NSF, ISCA, ASPLOS, MICRO, ICS, ICPP, HPCA, IEEE TOCS, IEEE TDPS, IEEE TOC, ACM TOPLAS, IEICE Transactions, PAID, ISLPED, DAC, DSN, IEEE TVLS, WCED, ISPASS.
- Awards Panel Judge, EECS HKN Student Scholarship Competition

G. Notable University Committee Work

- Committee Member, Rackham Predoctoral Fellowship Selection Committee, 2016-2017.
- Advisory Committee Member, Center for Entrepreneurship, UM College of Engineering, 2011-present.
- Committee Member, Mentoring Others Results in Excellence (MORE) Committee, 2010-2012.
- Member of the Rackham Executive Board, UM Rackham Graduate School, 2009-2012.
- Panel Member, Rackham Milestones Program, 2010.
- Faculty Reviewer, UM Faculty Research Grants panel, 2010.
- Faculty Reviewer, UM Rackham Merit Fellowship panel, 2008-2010.
- Committee Member, UM Engineering, Graduate Education Task Force, 2008-2009.
- Undergraduate Program Advisor, UM Computer Science and Engineering, 2006-2007.
- Internal Review Committee Member, UM EECS CSE Division, 2004-2005.
- Graduate Admissions Committee Member, UM EECS Computer Sciences and Engineering Division, 1999-2005.
- Graduate Admissions Committee Member, UW Madison Computer Sciences Department, Spring 1995.