

## EECS 373 F98 Sample Final Questions

1. How many address and data lines, respectively, will you find on a 4Kx8 SRAM device?
2. Using these 4Kx8 SRAM chips, design a 32 Kbyte memory module that interfaces to the MPC823 external bus. The memory should occupy 32K consecutive bytes starting at address 0x03C00000. Show how your design handles aligned word, halfword, and byte reads and writes.
3. Assume you implement your design from #2 using only an MPC823, the SRAM chips, and one Xilinx FPGA. Diagram the connections among the chips, and indicate the paths taken from the 823's address and control outputs to the SRAM  $\overline{CS}$ ,  $\overline{OE}$ , and address inputs.
4. Given the diagram from #3 and the parameters below, calculate the delay from the start of a read transaction (the clock edge where  $\overline{TS}$  is asserted) to data valid at the 823's data pins for each of the four combinations of fast/slow SRAM and fast/slow FPGA. (These parameter values are based on different speed grades of actual parts.) Recall that a Xilinx CLB can implement any *four-input* Boolean function with a constant delay. You must also add a delay of  $t_{IOB}$  each time a signal goes onto or off of the Xilinx chip.

Parameter	Description	Fast device	Slow device
$t_{AV}$	SRAM read access time from address valid	55 ns	70 ns
$t_{CS}$	SRAM read access time from $\overline{CS}$ asserted	55 ns	70 ns
$t_{OE}$	SRAM read access time from $\overline{OE}$ asserted	25 ns	30 ns
$t_{CLB}$	FPGA CLB delay	2 ns	5 ns
$t_{IOB}$	FPGA IOB delay	4 ns	8 ns

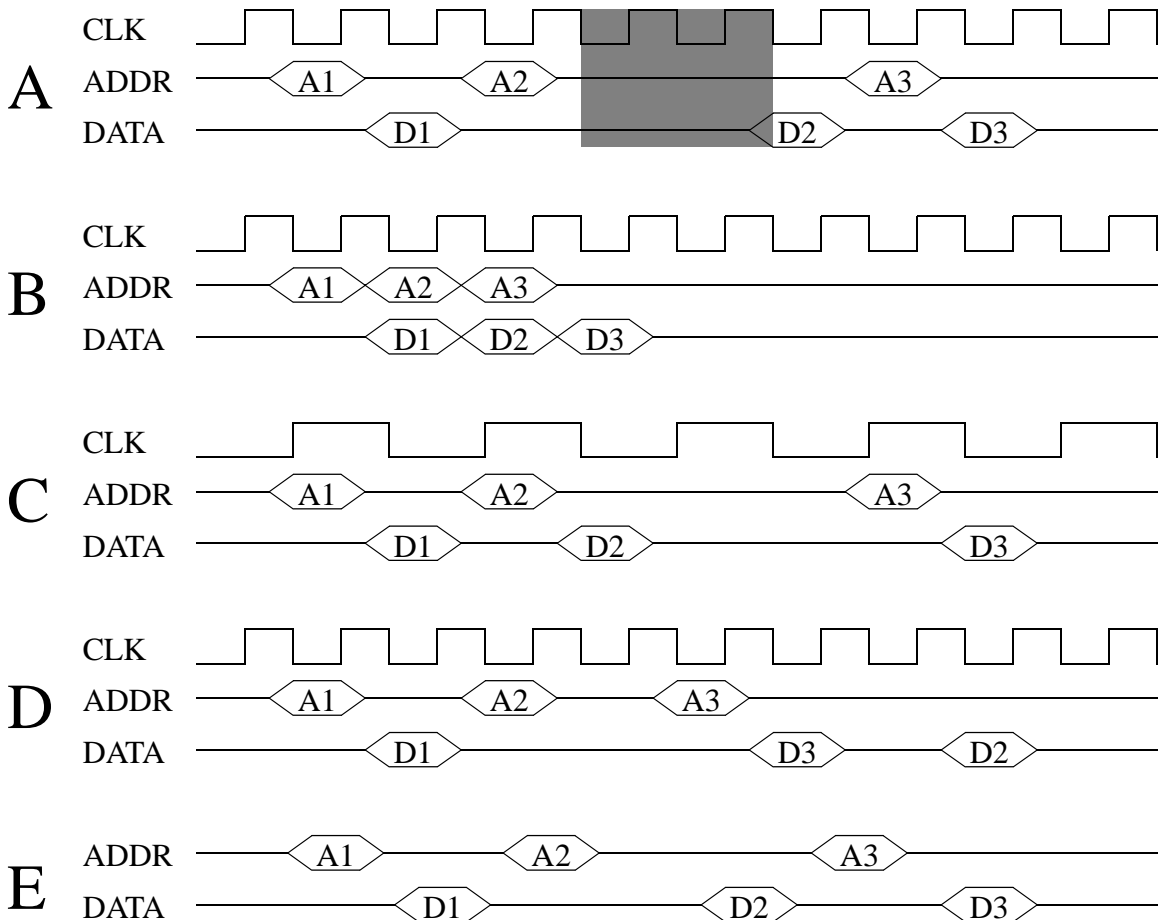
5. Regardless of the clock speed, the MPC823 data inputs require 6 ns of setup time before the clock edge where  $\overline{TA}$  is asserted. For each of the four device speed combinations, how many wait states are required for a read access at a bus speed of 20 MHz? 40 MHz? 50 MHz?
6. What type of memory device (discussed in class) is described by each phrase?
  - a. fast, volatile read/write memory; not very dense
  - b. dense non-volatile read/write memory; slow writes; erased in large blocks
  - c. dense volatile read/write memory
  - d. non-volatile read-only memory; erased by UV light
  - e. non-volatile read-only memory; programmed at the chip factory
  - f. multiplexed address lines
7. Analog-to-digital conversion.
  - a. Assume a perfectly accurate analog-to-digital converter. What is the range of possible

quantization error expressed in terms of LSBs?

- b. For each of the following analog-to-digital converter types, indicate (in terms of  $n$ ) the number of voltage comparators you would need to build an  $n$ -bit converter of that type and the number of sequential voltage comparisons that the converter would require to perform each conversion.

Converter type	Number of comparators	Sequential comparisons
Flash		
Successive approximation		

8. In each of the following timing diagrams, the bus master performs read transactions to addresses A1, A2, and A3, and a slave responds to each transaction with the data values D1, D2, and D3 respectively.



- a. For each of the five timing diagrams, indicate the type of bus illustrated.
- b. (2 pts) What term is used to refer to the shaded cycles in diagram A?
- c. Of the bus types you listed in part a, which ones preclude the use of a bus with multiplexed address/data lines? List all that apply, or write "none" if none.