

More Notes & Hints For Lab 6 (And Xilinx in General)

1. **Always** check the Xilinx logfile for unconnected nets. Pay special attention to nets & components that have been “optimized” (removed).
2. **Always** name your major nets. It is safe to leave intermediate nets unnamed.
3. When placing components on the schematic the following keystrokes will prove useful:
 - CTRL-R rotates the component
 - CTRL-M mirrors the component (horizontally)
4. Move the “UNC” (unconnected) ball off of a pin and then back on to the end of the pin in order to make connection to the component.
5. Drag wires and busses by their connection dots.
6. Be sure that your busses are named, either with a port symbol, or a net name. Busses use the format:
busname [7 : 0]