

# Saurabh Adya

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- Education:** **University of Michigan, Ann Arbor, MI**  
**Ph.D, Computer Science and Engineering,** 09/2000-06/2004  
**Ph.D Thesis Title:** Unification of VLSI Placement and Floorplanning  
**Master of Science, Computer Science and Engineering,** 09/2000-05/2002  
CGPA: 7.1/8.0  
**National Institute of Technology, Karnataka, (NITK), Surathkal, India** 09/1995-08/1999  
**Bachelor of Engineering, Electronics & Communication**  
Aggregate%: 83% Equivalent CGPA: 4.0/4.0
- Specialities** Algorithm design and implementation, numerical mathematics, large scale optimization, combinatorial optimization, iterative linear/non-linear solvers, parallel computing, large scale software architecture, FPGA, ASIC
- Research Interests:** Improving state of the art algorithms in EDA  
Physical Design/Physical Synthesis for VLSI  
Algorithms and methodologies for large scale VLSI placement  
ASIC/FPGA Physical Synthesis  
VLSI Floorplanning techniques
- Technical Skills:** **Computer Languages:** C/C++/STL, PERL, Python, Verilog, VHDL, Assembly(DSP(TMSc54x)/80\*86)  
**EDA Tools:** Magma Talus, Cadence SEDSM, Synopsys Design Compiler / IC Compiler / Primitime / Synplify / Premier  
**Operating Systems:** Linux, Unix, Windows
- Experience:** **Magma Design Automation (Acquired by Synopsys) , USA, Software Architect,** 06/2010-02/2012  
Responsible for placement team, engaged in research and development of technology for VLSI physical design and physical synthesis.  
**Synopsys Inc., Synplicity Group, USA, Staff R&D Engineer,** 05/2008-06/2010  
Primary owner of global placement technology for FPGA physical synthesis tool. Responsible for placement engine, physical synthesis optimizations, overall placement flow. Delivered a novel global placement based FPGA physical synthesis tool that beat the competing FPGA vendor tools by a large margin.  
**Synplicity Inc. (Acquired by Synopsys), USA, Sr. R&D Engineer,** 07/2004-05/2008  
**04/2006-05/2008:** Part of the Central Technology Group supporting common technologies for various products at Synplicity. Co-developed the next generation analytical global placer. Primary developer of physical synthesis tool for a major FPGA OEM partner. Responsible for an advanced research project aimed at architectural level physical synthesis.  
**07/2004-04/2006:** Primary owner of the global placement technology for the ASIC division. Responsible for placement engines, floorplanning and interactions of high level synthesis with physical optimizations in Synplicity's physical synthesis tool for ASIC's. Work involves timing driven placement, detail placement, floorplanning, handling physical constraints in layout tools, netlist partitioning and physical synthesis optimizations.  
**University of Michigan, Graduate Student Research Assistant,** 09/2000-06/2004  
Research Advisor: Professor Igor L. Markov  
CAD for VLSI physical design. Research involves **large-scale hierarchical floorplanning, mixed-size placement, physical synthesis, timing-driven placement** and **detail placement** techniques for VLSI.  
**Synplicity Inc., Sunnyvale, USA, Intern,** 06/2003-09/2003  
Implemented physical constraints handling in the global placement tool. Improved the ASIC physical synthesis flow of Synplicity to achieve better timing.

**IBM, Austin Research Labs, USA, Intern,** 06/2002-08/2002  
Improved analytical techniques for large-scale placement of VLSI chips. Worked on multi-level methods for analytical VLSI placement. Proposed techniques were incorporated into the Physical Driven Synthesis flow of IBM micro-electronics division.

**IBM, Austin Research Labs, USA, Intern,** 05/2001-07/2001  
Improved run-time of a linear equations solver used in IBM's analytical VLSI placement engine.

**Texas Instruments, Bangalore, India, Integrated Circuit Design Engineer,** 08/1999-08/2000  
Architecture specification and RTL design of a "Common Bus Interface" protocol for TI's test chip around DSP core TMS 320c28x. Verified an "On chip Emulation" hardware module. Used functional verification techniques to verify dual processor instruction stream execution architectures.

**Siemens Communication Software, Bangalore, India, Intern,** 06/1998-07/1998  
Tested "Directory Assistance" software for the Siemens' digital switch (EWSD).

**Patents:** S. N. Adya, G. Paul and K. McElvain, "Methods and apparatuses for circuit design and optimization", Filed in 2009.

**Publications:**

**Books:** D. A. Papa, J. A. Roy, S. N. Adya and I. L. Markov, "A Course in Physical Design of Integrated Circuits", Springer, To appear in 2011.

S. N. Adya, "Unification of VLSI Partitioning, Placement and Floorplanning", LAP Lambert Academic Publishing, ISBN-13: 978-3-8443-0506-7, 2011.

S. N. Adya and X. Yang, "Congestion Driven Physical Design", chapter in *Physical Design Handbook*, editors: C. Alpert, D. Mehta and S. Sapatnekar, CRC Press, 2008.

**Journals:** S. N. Adya, I. L. Markov and P. G. Villarrubia, "On Whitespace and Stability in Physical Synthesis", in *Trans. of Integration, the VLSI Journal*, vol 39, 2006, pp 340-362.

J. A. Roy, S. N. Adya, S. Chaturvedi, D. Papa and I. L. Markov, "Min-cut Floorplacement", in *IEEE Trans. on CAD*, vol 25(7), 2006, pp 1313-1327.

S. N. Adya and I. L. Markov, "Combinatorial Techniques for Mixed-size Placement", in *ACM Trans. on Design Automation of Electronic Systems*, vol. 10(5), January, 2005.

S. N. Adya, M. Yildiz, I. L. Markov, P. G. Villarrubia, P. N. Parakh and P. H. Madden, "Benchmarking for Large-scale Placement and Beyond", *IEEE Trans. on CAD*, vol. 23(4), April, 2004, pp. 472-487

S. N. Adya and I. L. Markov, "Fixed-outline Floorplanning : Enabling Hierarchical Design", *IEEE Trans. on VLSI*, vol. 11(6), Dec 2003, pp. 1120-1135.

**Conferences:** A. Crews and S. N. Adya, "Evolution of a multi-platform thread pool package", presentation in *Synopsys Terascale Summit V*, Mountain View, 2010

J. A. Roy, D. A. Papa, S. N. Adya, H. H. Chan, J. F. Lu, A. N. Ng and I. L. Markov, "Capo: Robust and Scalable Open-Source Min-cut Floorplacer", in *International Symposium on Physical Design (ISPD)*, San Francisco, 2005, pp. 224-226.

H. H. Chan, S. N. Adya, and I. L. Markov, "Are Floorplan Representations Useful in Digital Design?", in *International Symposium on Physical Design (ISPD)*, San Francisco, 2005, pp. 129-136.

S. N. Adya, S. Chaturvedi, J. A. Roy, D. Papa and I. L. Markov, "Unification of Partitioning, Placement and Floorplanning", in *International Conference of Computer Aided Design (ICCAD)*, San Jose, 2004, pp. 550-557

D. Papa, S. N. Adya and I. L. Markov, "Constructive Benchmarking for Placement", *Great Lakes Symposium on VLSI (GLSVLSI)*, 2004, pp. 113-118.

S. N. Adya, I. L. Markov and P. G. Villarrubia, "On Whitespace and Stability in Mixed-size Placement and Physical Synthesis", *International Conference on Computer Aided Design (ICCAD)*, San Jose, 2003, pp. 311-318.

S. N. Adya, I. L. Markov and P. G. Villarrubia, "Improving Min-cut Placement for VLSI Using Analytical Techniques", *IBM ACAS Conference*, Austin, 2003, pp. 55-62.

S. N. Adya, M. Yildiz, I. L. Markov, P. G. Villarrubia, P. N. Parakh and P. H. Madden, "Benchmarking for Large-scale Placement and Beyond", *International Symposium on Physical Design (ISPD)*, Monterey, 2003, pp. 95-103 (invited).

S. N. Adya and I. L. Markov, "Consistent Placement of Macro-Blocks using Floorplanning and Standard-Cell Placement", in Proc. *International Symposium on Physical Design (ISPD)*, San Diego, 2002, pp. 12-17.

S. N. Adya and I. L. Markov, "Fixed Outline Floorplanning Through Better Local Search", *International Conference on Computer Design (ICCD)*, Austin, September 2001, pp. 328-334

**Academic Projects:**

**Advanced VLSI Design:** Low Power micro-controller design for use in Wireless Integrated Microsystem (WIMS) project. Project involved architecture definition, micro-architecture design, simulation, developing the verification framework and physical design of the chip. A mixed-signal chip based on this micro-controller secured 1<sup>st</sup> place in the **DAC Conceptual Design Contest, 2003**.

**CAD For VLSI:** Novel detailed-placement techniques for a large-scale VLSI placement.

**Parallel Algorithms:** Parallel Iterative Linear Solvers in the VLSI CAD context.

**Computer Architecture:** Design of a router engine on the Simple Scalar micro-architectural simulator.

**Parallel Computer Architecture:** Study of Coherent Network Interfaces.

**Real-Time Systems:** Modelling of real-time communication protocols using Ptolemy simulator.

**Undergraduate Thesis:** General purpose DSP system based on DSP TMS 320c542. Digital Multimeter based on DSP algorithms.

**Professional Service:**

Technical session chair of International Conference on Computer Aided Design, 2011

Technical program committee member of International Symposium on Physical Design, 2012

Technical session chair of International Conference on Computer Aided Design, 2009

Technical program committee member of International Conference on Computer Design, 2006

Technical session chair of International Conference on Computer Design, 2006

Technical program committee member of International Conference on Computer Design, 2005

Technical session chair of International Conference on Computer Design, 2005

Technical program committee member of Conference on Information Technology, 2006

Reviewer for conferences DATE, DATE, DAC, ISPD, ICCAD, GLSVLSI, ICCD, CIT, VLSI Design

Reviewer for technical journals *IEEE Transactions on CAD*, *IEE Proceedings on Circuits, Devices and Systems*, *Integration*, *the VLSI Journal*, *IEEE Transactions on Computers*, *Annals of OR*

**Awards:**

Synplicity Founder's Award for Outstanding Innovation: FPGA Physical Synthesis Flow and FPGA Global Placement, 2007.

Synplicity Engineering Outstanding Achievement Award: ASIC Macro Placement, 2005.

Synplicity Engineering "Rookie of the year" Award: ASIC Global Placement, 2005.

Synplicity Engineering Team Award: ASIC Design Planning/Floorplanning Tool, 2004.

University of Michigan College of Engineering's Research Mentor Award, 2004.

IEEE/ACM Design Automation Conference fellowship for graduate students, 2001.

Third prize in "Technofest 2000", an all India level project exposition contest, 2000.

First prize in All India Inter College Hardware design contest held under the auspices of IETE, 1998.

Second prize in All India Inter College Software design contest held under the auspices of IETE, 1998.

Awarded "Cincinnati Prize" for overall meritorious performance in high school, 1994.