EECS 373
Design of Microprocessor-Based Systems
http://web.eecs.umich.edu/~prabal/teaching/eecs373

Prabal Dutta
University of Michigan

100 cm³
[IPSN'12]

50 cm³
[Sensys'12]

1 cm³
[IPSN'12]

1 mm³
[ISSCC'12]

Lecture 1: Introduction
January 8, 2015

1

What is an embedded system?

2

- Has MPU
- Is app-specific
- Has no OS
- Real-time
- Integrated in device
- Fixed I/O / not expandable
- Worry about memory mgmt

- Peripherals
- Low power
- Small
- Mobile / networked
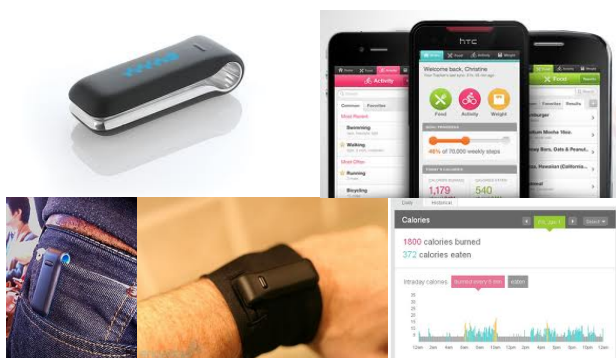- Cost constrained
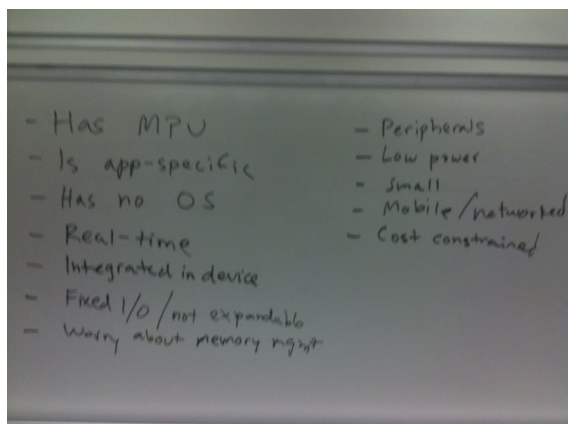
3

Embedded, Everywhere

4

Embedded, Everywhere - Fitbit

5

Embedded, Everywhere – WattVision on Kickstarter

6

**What is driving the
embedded everywhere explosion?**

Outline

Technology Trends

Design Questions

Course Administrivia

Tools Overview/ISA Start

**Moore's Law (a statement about economics):
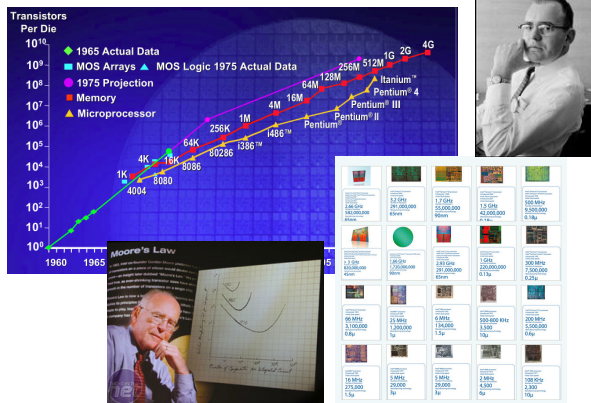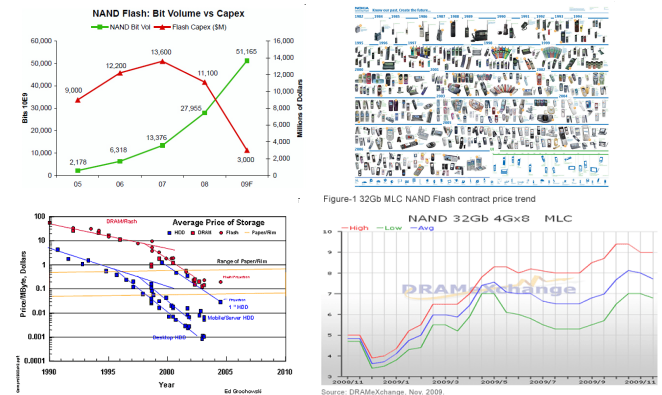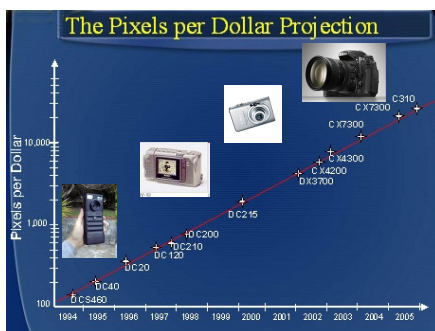IC transistor count doubles every 18-24 mo**

Photo Credit: Intel

**Flash memory scaling:
Rise of density & volumes; Fall (and rise) of prices**

Figure-1 32Gb MLC NAND Flash contract price trend

Source: DRAMeXchange, Nov. 2009.

**Hendy's "Law":
Pixels per dollar doubles annually**

Credit: Barry Hendy/Wikipedia

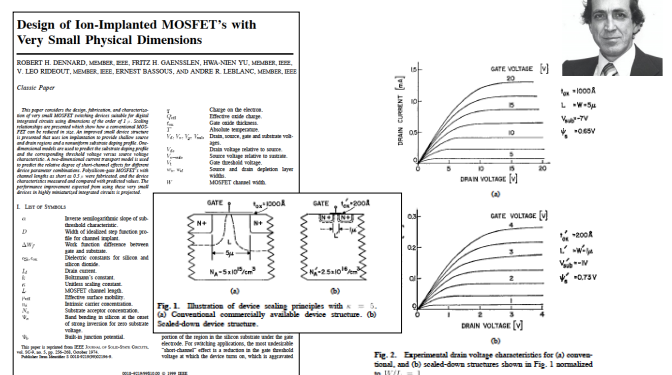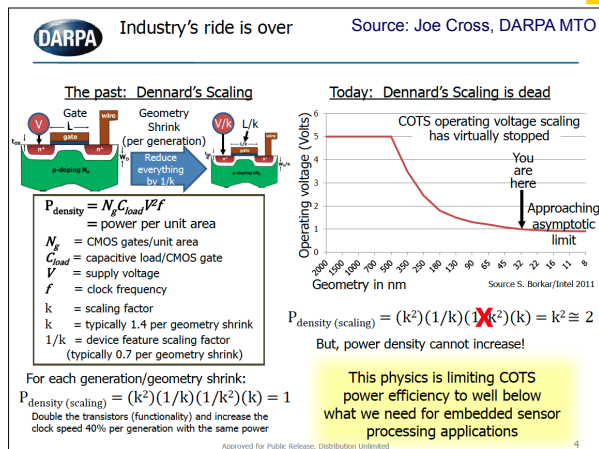**Dennard Scaling made transistors fast and low-power:
So everything got better!**

Dennard Scaling...is Dead

Industry's ride is over — Source: Joe Cross, DARPA MTO

The past: Dennard's Scaling / Today: Dennard's Scaling is dead

$$P_{density} = N_g C_{load} V^2 f$$
= power per unit area

N_g = CMOS gates/unit area
C_{load} = capacitive load/CMOS gate
V = supply voltage
f = clock frequency
k = scaling factor
k = typically 1.4 per geometry shrink
$1/k$ = device feature scaling factor
(typically 0.7 per geometry shrink)

For each generation/geometry shrink:
$$P_{density (scaling)} = (k^2)(1/k)(1/k^2)(k) = 1$$
Double the transistors (functionality) and increase the clock speed 40% per generation with the same power

COTS operating voltage scaling has virtually stopped
You are here
Approaching asymptotic limit
Geometry in nm
Source S. Borkar/Intel 2011

$$P_{density (scaling)} = (k^2)(1/k)(1 ✗ k^2)(k) = k^2 \cong 2$$
But, power density cannot increase!

This physics is limiting COTS power efficiency to well below what we need for embedded sensor processing applications

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And the Party's Over...

Decades of exponential performance growth stalled in 2004

Source: NRC, The Future of Computing Performance, Game Over or Next Level?
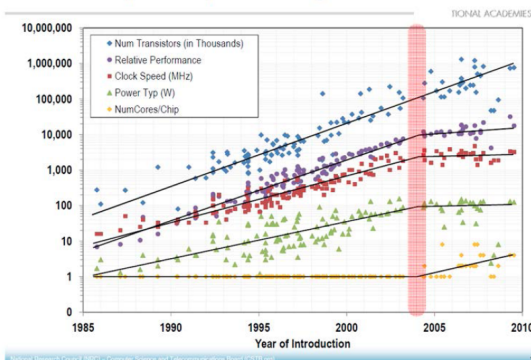
Not so fast! Bell's Law of Computer Classes: A new computing class roughly every decade

log (people per computer)

Number Crunching Data Storage

Mainframe

Minicomputer

Workstation

PC

Laptop

CPSD

productivity interactive

streaming information to/from physical world

year

"Roughly every decade a new, lower priced computer class forms based on a new programming platform, network, and interface resulting in new usage and the establishment of a new industry."

Adapted from D. Culler
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MEMS Accelerometers: Rapidly falling price and power

O(mA)

Price Power

25 μA @ 25 Hz

ADXL345 [Analog Devices, 2009]

24g
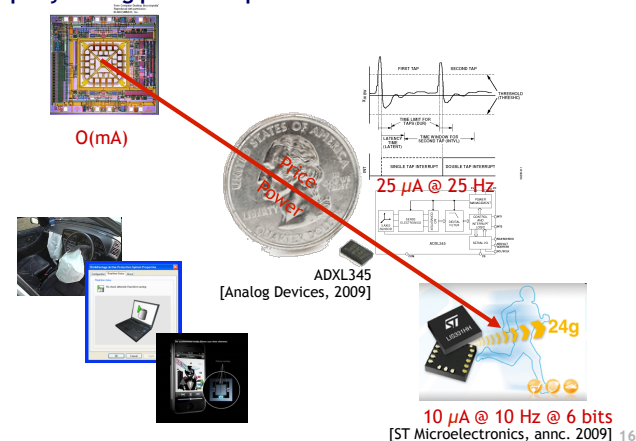
10 μA @ 10 Hz @ 6 bits
[ST Microelectronics, annc. 2009] 16

MEMS Accelerometer in 2012

Industry's Lowest Power MEMS Accelerometer
• 2 μA @ 100 Hz
• 300 nA wake-up mode
ADXL362 MEMS Accelerometer
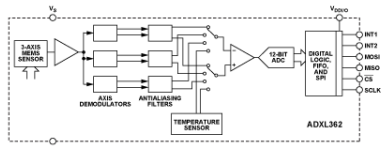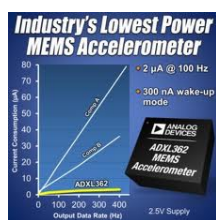
1.8 μA @ 100 Hz @ 2V supply!

ADXL362
[Analog Devices, 2012]

MEMS Gyroscope Chip

4.5mm
X-Dir Driver
Y-Dir
1μm Drive
0.01Å Sense
700μm Gyro Mass
Sense
ΣΔ
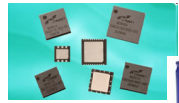20KV X1000   0001   10.0U MSME
Clock & Control Logic
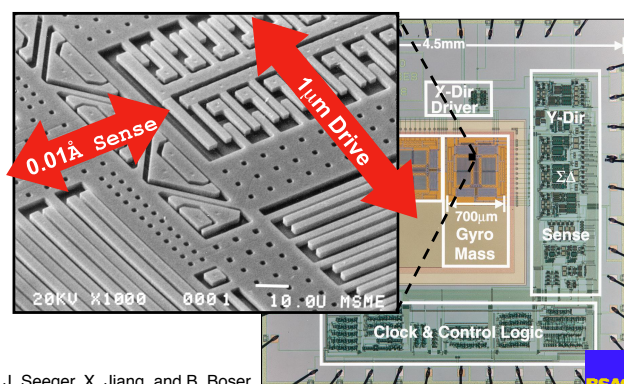
J. Seeger, X. Jiang, and B. Boser

BSAC

Energy harvesting and storage: Small doesn't mean powerless…

1st Annual Workshop on
MICRO POWER TECHNOLOGIES
Radisson Hotel, San Jose, CA   October 22, 2009

RF [Intel]

Clare Solar Cell

Thin-film batteries

Shock Energy Harvesting
CEDRAT Technologies

Piezoelectric
[Holst/IMEC]
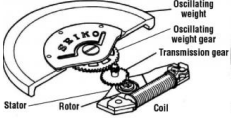
Electrostatic Energy
Harvester [ICL]

10mm

Oscillating
weight
Oscillating
weight gear
Transmission gear

Stator   Rotor   Coil

High-Temperature
Heatsink
Thermocouple
Assembly

Sensor

Sensor   Sensor

Annular Electronics
& Power Conditioning
Compartment

Low-Temperature
Heatsink

Thermoelectric Ambient
Energy Harvester [PNNL]
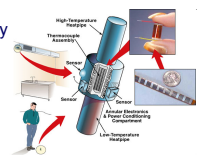
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Bell's Law, Take 2: Corollary to the Laws of Scale

Intel® 4004 processor
Introduced 1971
Initial clock speed
108 KHz
Number of transistors
2,300
Manufacturing technology
10µ

15x size decrease
40x transistors
55x smaller λ

Quad-Core Intel® Xeon® processor
Quad-Core Intel® Core™2 Extreme processor
Introduced 2006
Intel® Core™2 Quad processors
Introduced 2007
Initial clock speed
2.66 GHz
Number of transistors
582,000,000
Manufacturing technology
65nm
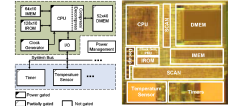
UMich Phoenix Processor
Introduced 2008
Initial clock speed
106 kHz @ 0.5V Vdd
Number of transistors
92,499
Manufacturing technology
0.18 µ

Photo credits: Intel, U. Michigan

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Why study 32-bit MCUs and FPGAs?
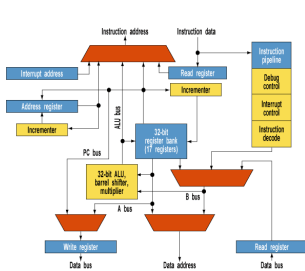
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MCU-32 and PLDs are tied in embedded market share

Year

Device (group)
PLD
32 Bit MCU

% of Total Sum of DATA

Source: iSuppli
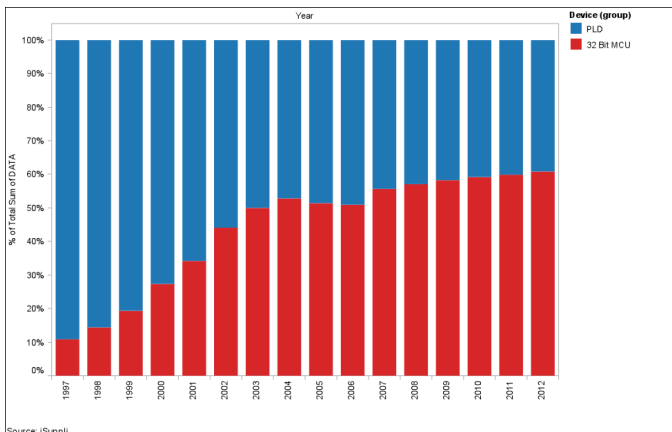
23

What distinguishes
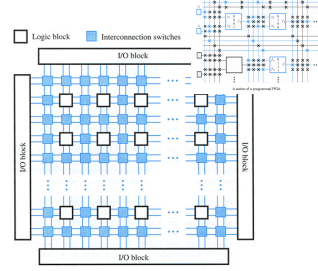a Microprocessor from an FPGA?

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Slide 25

MPU

The Cortex M3's Thumbnail architecture looks like a conventional Arm processor. The differences are found in the Harvard architecture and the instruction decode that handles only Thumb and Thumb 2 instructions.
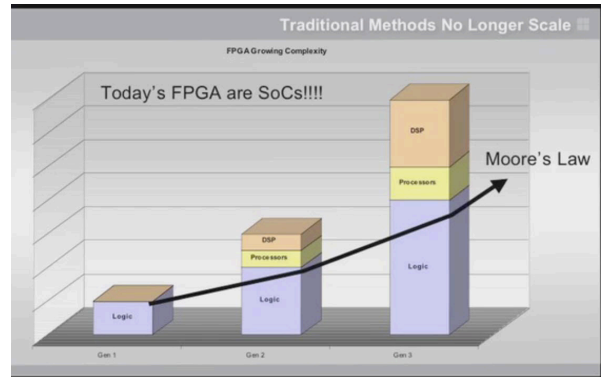
FPGA

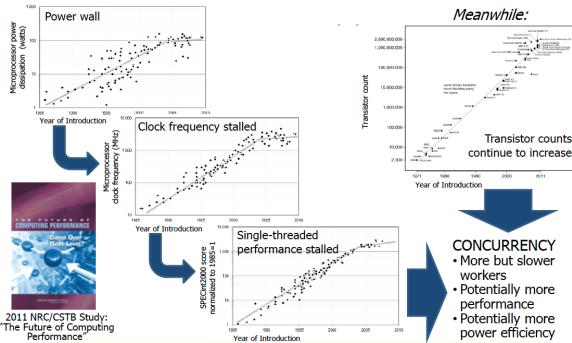General structure of an FPGA

Slide 26

Modern FPGAs: best of both worlds!

Traditional Methods No Longer Scale

FPGA Growing Complexity

Today's FPGA are SoCs!!!!

Moore's Law

Slide 27

Is the party really over?

DARPA Technology landscape: move past power limitations, effectively utilize concurrency

Power wall

Meanwhile:

Clock frequency stalled

Transistor counts continue to increase

2011 NRC/CSTB Study: "The Future of Computing Performance"

Single-threaded performance stalled

CONCURRENCY
• More but slower workers
• Potentially more performance
• Potentially more power efficiency

Concurrency only path left – National Academy of Science report

Approved for Public Release, Distribution Unlimited

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Slide 28

Why study the ARM architecture
(and the Cortex-M3 in particular)?

Slide 29

Lots of manufacturers ship ARM products

Slide 30

ARM is *the* big player

• ARM has a huge market share
  – As of 2011 ARM has chips in about 90% of the world's mobile handsets
  – As of 2010 ARM has chips in 95% of the smartphone market, 10% of the notebook market
    • Expected to hit 40% of the notebook market in 2015.
  – Heavy use in general embedded systems.
    • Cheap to use
      – ARM appears to get an average of 8¢ per device (averaged over cheap and expensive chips).
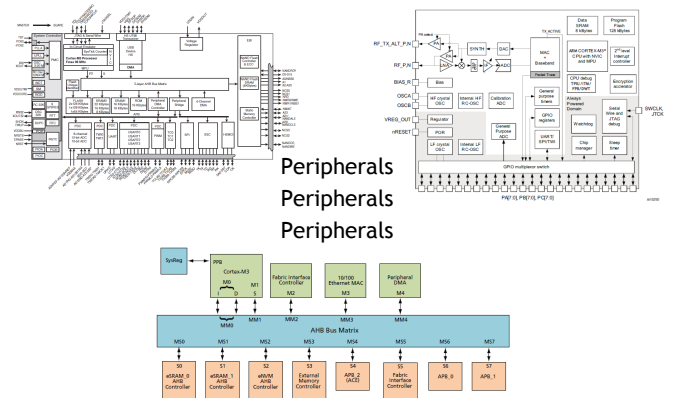   • Flexible
      – Spin your own designs.

Slide 31

What differentiates these products from one another?

Slide 32

The difference is…

Peripherals
Peripherals
Peripherals

Slide 33

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Slide 34

**W'15 Instructional Staff
(see homepage for contact info, office hours)**

Matt Smith
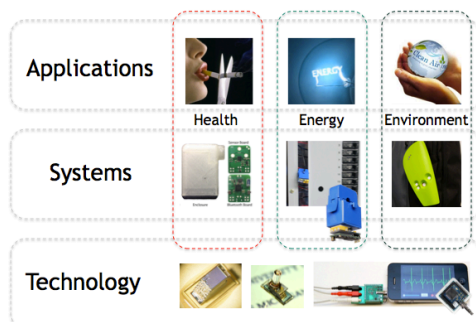*Lab Instructor*

Prabal Dutta
Instructor

Pat Pannuto
GSI

John Connolly
IA

Chris Fulara
IA

Alex Laberge
IA

Ryan Wooster
IA

Slide 35

My research interests

Applications — Health, Energy, Environment

Systems

Technology

Slide 36

Course goals

- *Learn to implement* embedded systems including hardware/software interfacing.

- *Learn to design* embedded systems and how to think about embedded software and hardware.

- *Design and build* non-trivial projects involving both hardware and software.

Prerequisites

- EECS 270: Introduction to Logic Design
  - Combinational and sequential logic design
  - Logic minimization, propagation delays, timing

- EECS 280: Programming and Intro Data Structures
  - C programming
  - Algorithms (e.g. sort) and data structures (e.g. lists)

- EECS 370: Introduction to Computer Organization
  - Basic computer architecture
  - CPU control/datapath, memory, I/O
 - Compiler, assembler

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Topics

- Memory-mapped I/O
  - The idea of using memory addressed to talk to input and output devices.
    - Switches, LEDs, hard drives, keyboards, motors

- Interrupts
  - How to get the processor to become "event driven" and react to things as they happen.

- Working with analog signals
  - The real world isn't digital!

- Common peripheral devices and interfaces
 - Serial buses, timers, etc.

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Example: Memory-mapped I/O
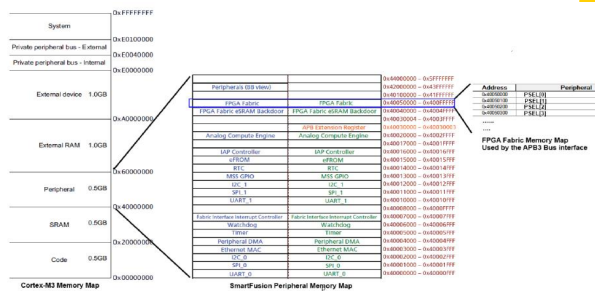
- This is *important*.
  - It means our software can tell the hardware what to do.
    - In lab 3 you'll design hardware on an FPGA which will control a motor.
      - But more importantly, that hardware will be designed so the software can tell the hardware exactly what to do with the motor. All by simply writing to certain memory locations!
  - In the same way, the software can read memory locations to access data from sensors etc...

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Example: Anatomy of a timer system
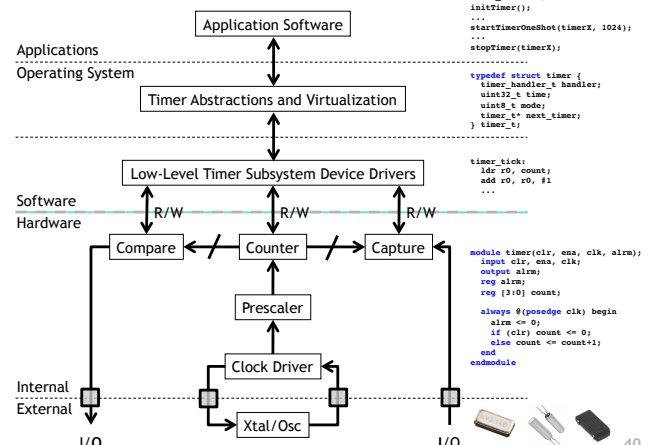
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Grades

Item	Weight
======	=========
Labs (7)	25%
Project	25%
Exams	35% (15% midterm; 20% final)
HW/Guest talks	10%
Oral presentation	4%
Course Evaluation	1%

- Project & Exams tend to be the differentiators
- Class median is generally a B+

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Time

- Assume you are going to spend a lot of time in this class.
  - 2-3 hours/week in lecture (we cancel a few classes during project time)
  - 8-12 hours/week working in lab
    - *Expect more during project time; some labs are a bit shorter.*
  - ~20 hours (total) working on homework
  - ~20 hours (total) studying for exams.
  - ~8 hour (total) on your oral presentation
- Averages out to about 15-20 hours/week pre-project and about 20 during the project...
  - This is more than we'd like, but we've chosen to go with state-of-the-art tools, and those generally have a steep learning curve.

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Labs

- Start next week.
- 7 labs, 8 weeks, groups of 2
  1. FPGA + Hardware Tools
  2. MCU + Software Tools
  3. Memory + Memory-Mapped I/O
  4. Interrupts
  5. Timers and Counters
  6. Serial Bus Interfacing
  7. Data Converters (e.g. ADCs/DACs)

- Labs are very time consuming.
  - As noted, students estimated 8-12 hours per lab with one lab (which varied by group) taking longer.

Open-Ended Project

- Goal: <u>learn how to build embedded systems</u>
  - By <u>building</u> an embedded system
  - Work in teams of 2 to 4
  - You design your own project

- The major focus of the last third of the class.
  - Labs will be done and we will cancel some lectures and generally try to keep you focused

- Important to start early.
  - After all the effort in the labs, it's tempting to slack for a bit. The best projects are those that get going right away (or even earlier)

- Some project lead to undergraduate research

Sample projects from F'10 and their results

- Energy-harvesting sensors →
  Sensys demo, IPSN paper, TI project, Master's thesis

- Wireless AC Power Meter →
  SURE, IPSN demo, NSF GRFP, SenSys paper, Grad School
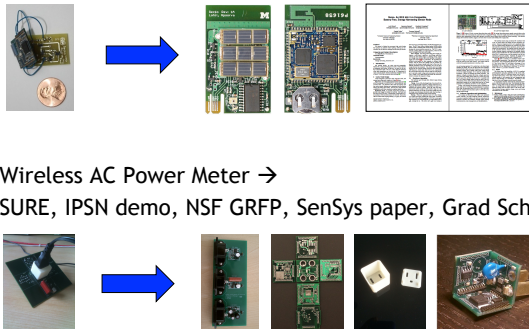
Letters of recommendation for graduate school

- Grad school apps will require supporting letters
- Faculty write letters and read "coded" letters

- Strong letters give evidence of research ability
- Strong letters can really help your case

- Weak letters are vague and give class standing
- Weak letters are useless (or even worse)

- Want a strong letter?
  - Do well in this class
  - Pull off an impressive project
  - Continue class project as independent research in W'15

Homework

- Start TODAY!
- 4-5 assignments
  - A few "mini" assignments
    - Mainly to get you up to speed on lab topics
  - A few "standard" assignments
    - Hit material we can't do in lab.
- Also a small part is for showing up to guest lectures

Midterm and Final Exams

- Midterm (Tue, Feb 25, 2015 from 1:30pm-3:00pm)
  - Emphasize problem solving fundamentals

- Final (Tue, Apr 28, 2015 from 4:00-6:00pm)
  - Cumulative topics w/ experience of projects
  - Some small amount of material from presentations

Looking for me?

- Nominal Office Hours
  - Time TBD in 4773 BBB
  - Sometimes in lab sections
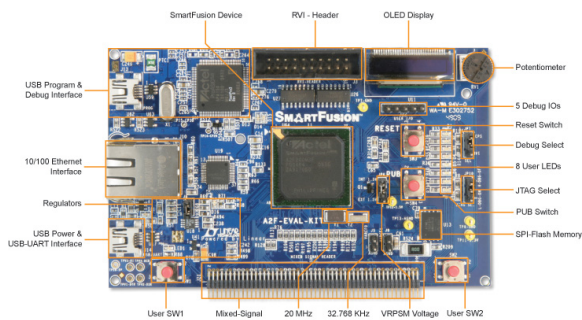
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## We are using Actel's SmartFusion Evaluation Kit

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A2F200M3F-FGG484ES
- 200,000 System FPGA gates, 256 KB flash memory, 64 KB SRAM, and additional distributed SRAM in the FPGA fabric and external memory controller
- Peripherals include Ethernet, DMAs, I²Cs, UARTs, timers, ADCs, DACs and additional analog resources
- USB connection for programming and debug from Actel's design tools
- USB to UART connection to UART_0 for HyperTerminal examples
- 10/100 Ethernet interface with on-chip MAC and external PHY
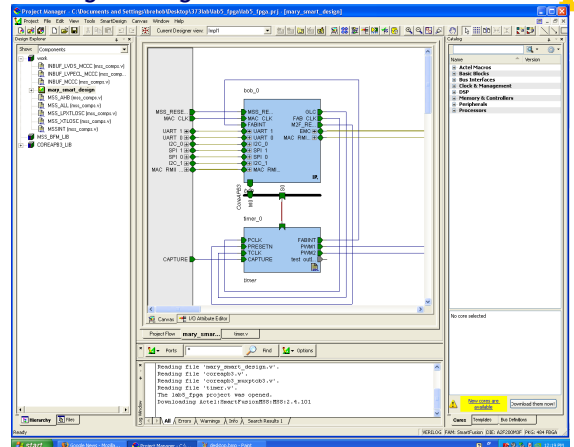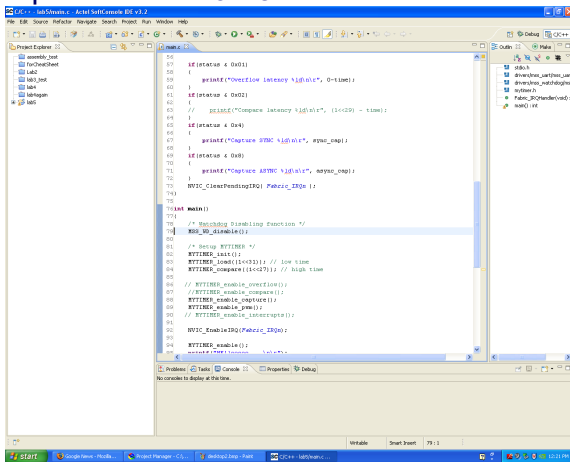- Mixed-signal header for daughter card support
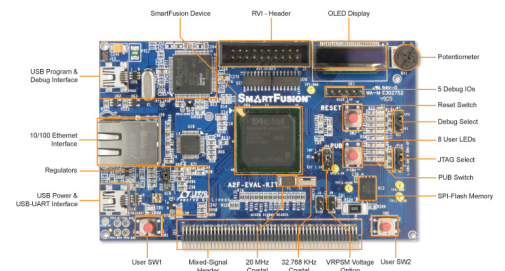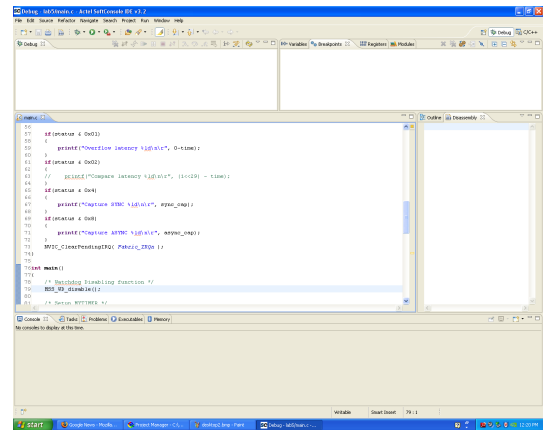

FPGA work
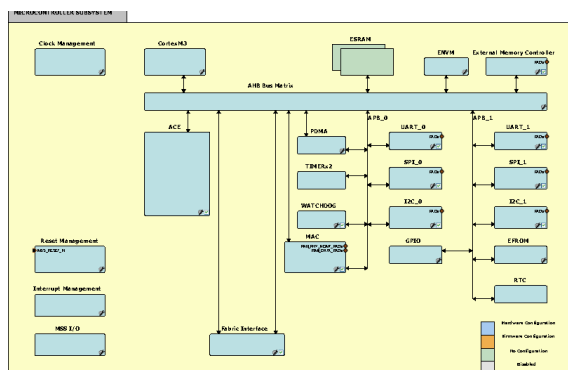
53
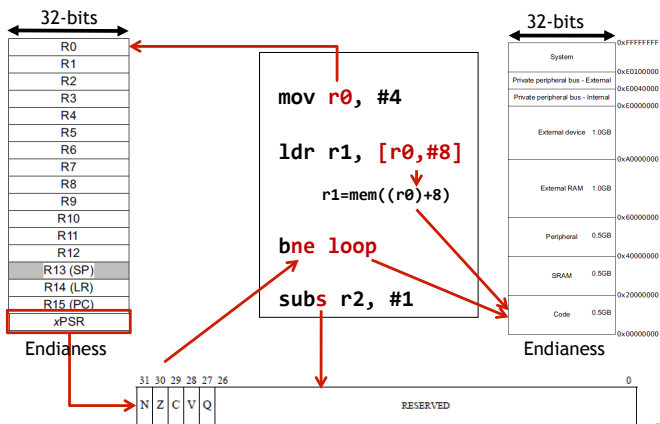
"Smart Design" configurator

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Debugger is GDB-based. Includes command line.
Works really quite well.

ARM ISA: Elements of an Instruction Set Architecture
(registers, memory, word size, endianess, conditions, instructions, addressing modes)

32-bits

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13 (SP)
R14 (LR)
R15 (PC)
xPSR

Endianess

```
mov r0, #4

ldr r1, [r0,#8]

  r1=mem((r0)+8)

bne loop

subs r2, #1
```

32-bits

System	0xFFFFFFFF
Private peripheral bus - External	0xE0100000
Private peripheral bus - Internal	0xE0040000
	0xE0000000
External device 1.0GB	
	0xA0000000
External RAM 1.0GB	
	0x60000000
Peripheral 0.5GB	
	0x40000000
SRAM 0.5GB	
	0x20000000
Code 0.5GB	
	0x00000000

Endianess

31 30 29 28 27 26						0
N	Z	C	V	Q	RESERVED	

Assembly example:
Work through on your own. We'll discuss next time

```
data:
    .byte 0x12, 20, 0x20, -1
func:
        mov r0, #0
        mov r4, #0
        movw    r1, #:lower16:data
        movt    r1, #:upper16:data
top:    ldrb    r2, [r1],#1
        add r4, r4, r2
        add r0, r0, #1
        cmp r0, #4
        bne top
```

Questions?

Comments?

Discussion?