

Exam #:

EECS 373 Practice Midterm & Homework #2

Fall 2012

Name: _____ Uniquename: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

Scores:

Problem #	Points
1	/20
2	/15
3	/10
4	/15
5	/10
6	/10
7	/10
8	/10
Total	/100

NOTES:

- **PUT YOU NAME/UNIQUENAME ON EVERY PAGE TO ENSURE CREDIT!**
- Can refer to the ARM Assembly Quick Reference Guide
- Can use a basic/scientific calculator (but not a phone, PDA, or computer)
- Don't spend too much time on any one problem.
- You have 80 minutes for the exam.
- The exam is 7 pages long, including the cover sheet.
- Show your work and explain what you're doing. Partial credit w/o this is rare.

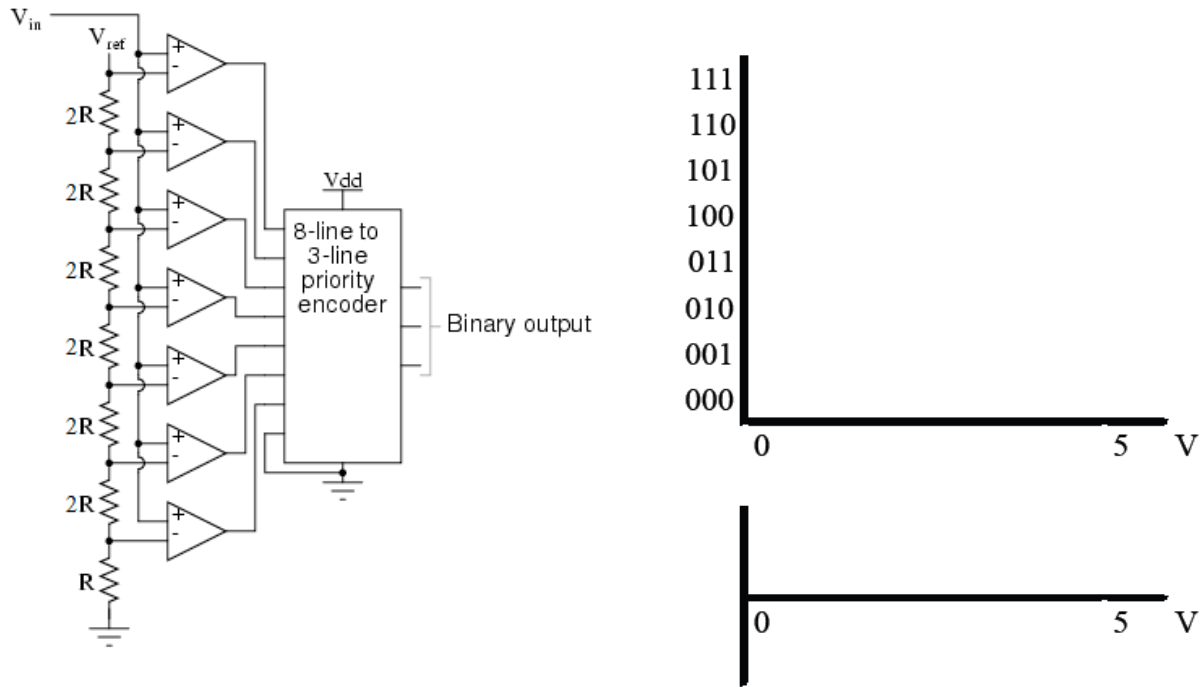
Name: _____ Username: _____

1) Fill-in-the-blank or circle the *best* answer. [20 points, -2 per wrong or blank answer]

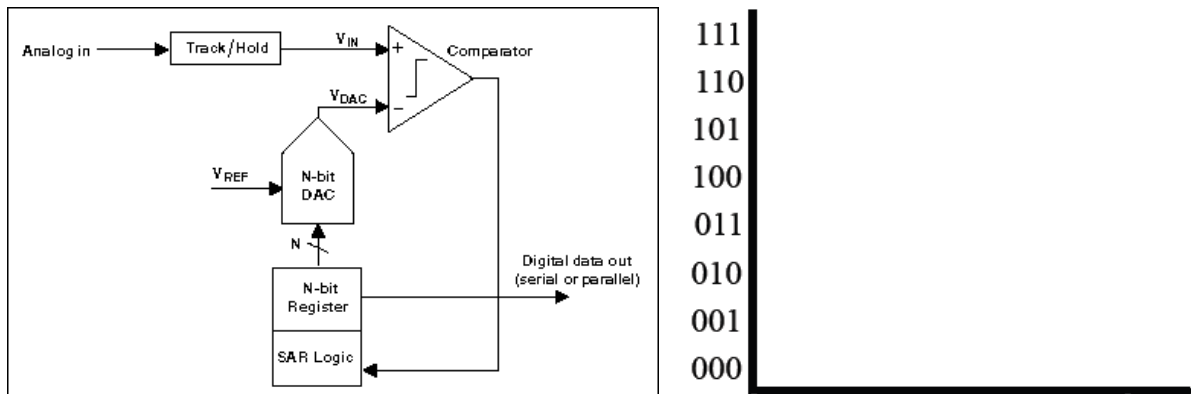
- a) An N-bit SAR ADC requires $\frac{1}{\lg(N)} / N$ approximation cycles to produce a result.
- b) A ***DRAM / SRAM / PROM*** is non-volatile. DRAM most commonly uses a ***1T / 4T / 6T*** cell. SRAM most commonly uses a ***1T / 4T / 6T*** cell.
- c) A 100 MHz clock with a duty cycle of 25% is high for _____ ns per cycle.
- d) An EABI-compliant procedure could use ***registers / stack / both / neither*** to receive arguments from the caller, and the callee should ***never / sometimes / always*** save and restore the registers it uses.
- e) The I2C bus is *most commonly* used to connect ***chips on a board / devices in a rack / computers and modems***.
- f) The SPI bus is *most commonly* used to connect ***one / two / many*** master device(s) to ***one / two / many*** slave device(s).
- g) You would expect that ***I2C / SPI*** would be able to support the higher data rate.
- h) Differential signaling over a twisted pair of wires is used in a number of modern buses to ***reduce the impact of external noise / make it easier to not have a shared clock / implement Manchester encoding / increase the speed of the data lines***.
- i) Multiple devices can usually share an ***edge / level*** triggered interrupt line.
- j) The RESET interrupt is ***maskable / non-maskable***.

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- 2) Consider the following 3-bit ADC. Draw the conversion transfer function (binary output vs input voltage) on the top graph. Draw the quantization error transfer function (error voltage vs input voltage) on the bottom graph. Make sure the transition points are clear. Assume V_{ref} is 5V. [15]



- 3) Assume you have a 3-bit SAR ADC. The analog input is 0.35 V and the V_{ref} is 1V. Show how the SAR would approximate the analog input over three cycles. Label the cycles on the x-axis and show the approximation as a meandering stair-step line on the graph. [10]



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4) ARM assembly [15]

- a) Write ARM assembly code that sets bits 4, 5, and 6 of register r0 to “1s” without changing any other bits in that register. Use as few lines of assembly as you can. [5]

- b) After running the following code snippet, the value of r2 at done is _____. Show how you arrived at this conclusion. [5]

```
...
start:
    movs r0, #1
    movs r1, #1
    movs r2, #1
    subs r0, r1
    bne done
    movs r2, #2
done:
    b done
...
```

- c) Write an ARM assembly language procedure that implements the following function in an EABI-compliant manner and conforms to the following signature. Identify which register holds which argument. [5]

```
f(x,y,z) = x+y-z
int32_t func(int32_t x, int32_t y, int32_t z);
```


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- 7) Imagine that you want to attach an LED to the ARM Advanced Peripheral Bus (APB). Sketch out the glue logic needed to interface a D flip-flop (DFF) to the APB. Assume that the PSEL line is the peripheral select (i.e. it goes high when the processor is addressing the DFF) and that the DFF will be attached to data bits (PWDATA[0] and PRDATA[0]), perhaps through tri-state drivers. You should be able to change the value of the DFF by writing the memory location corresponding to the PSEL and read the current value of the DFFs by reading the location. Assume that the DFF has an enable (ENA) line that, when not asserted, ignores any inputs (e.g. D and CLK) but continues to drive Q and Q#. The APB signals available to you are: PCLK, PADDR, PWRITE, PSEL, PENABLE, PWDATA, and PRDATA. **[10]**

