Cortex-M3

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Release Information

The following changes have been made to this book.

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<th>Issue</th>
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Product Status

The information in this document is Final (information on a developed product).

Web Address

http://www.arm.com
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Preface

This preface introduces the *Cortex-M3 Technical Reference Manual* (TRM). It contains the following sections:

- *About this book* on page x
- *Feedback* on page xiii.
About this book

This book is for the Cortex-M3 processor.

Product revision status

The rnpn identifier indicates the revision status of the product described in this manual, where:
- \textit{rn} Identifies the major revision of the product.
- \textit{pn} Identifies the minor revision or modification status of the product.

Intended audience

This manual is written to help system designers, system integrators, verification engineers, and software programmers who are implementing a \textit{System-on-Chip} (SoC) device based on the Cortex-M3 processor.

Using this book

This book is organized into the following chapters:

- \textbf{Chapter 1 Introduction}
  Read this for a description of the components of the processor, and of the product documentation.

- \textbf{Chapter 2 Functional Description}
  Read this for a description of the functionality of the processor.

- \textbf{Chapter 3 Programmers Model}
  Read this for a description of the processor register set, modes of operation, and other information for programming the processor.

- \textbf{Chapter 4 System Control}
  Read this for a description of the registers and programmers model for system control.

- \textbf{Chapter 5 Memory Protection Unit}
  Read this for a description of the Memory Protection Unit (MPU).

- \textbf{Chapter 6 Nested Vectored Interrupt Controller}
  Read this for a description of the interrupt processing and control.

- \textbf{Chapter 7 Debug}
  Read this for information about debugging and testing the processor core.

- \textbf{Chapter 8 Data Watchpoint and Trace Unit}
  Read this for a description of the Data Watchpoint and Trace (DWT) unit.

- \textbf{Chapter 9 Instrumentation Trace Macrocell Unit}
  Read this for a description of the Instrumentation Trace Macrocell (ITM) unit.

- \textbf{Chapter 10 Embedded Trace Macrocell}
  Read this for a description of the processor Embedded Trace Macrocell (ETM).

- \textbf{Chapter 11 Trace Port Interface Unit}
  Read this for a description of the Trace Port Interface Unit (TPIU).
Appendix A Revisions
Read this for a description of the technical changes between released issues of this book.

Glossary Read this for definitions of terms used in this book.

Conventions
Conventions that this book can use are described in:

• Typographical

Typographical
The typographical conventions are:

italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace Italic Denotes arguments to monospace text where the argument is to be replaced by a specific value.

< and > Enclose replaceable terms for assembler syntax where they appear in code or code fragments. For example:

\texttt{ADD \texttt{Rd, Rn, <op2>}}

Additional reading
This section lists publications by ARM and by third parties.


ARM publications
This book contains information that is specific to this product. See the following documents for other relevant information:

• ARMv7-M Architecture Reference Manual (ARM DDI 0403)
• ARM Cortex-M3 Integration and Implementation Manual (ARM DII 0240)
• ARM AMBA® 3 AHB-Lite Protocol (v1.0) (ARM IHI 0033)
• ARM AMBA™ 3 APB Protocol Specification (ARM IHI 0024)
• AMBA® 3 ATB Protocol Specification (ARM IHI 0032)
• ARM CoreSight™ Components Technical Reference Manual (ARM DDI 0314)
• ARM Debug Interface v5 Architecture Specification (ARM IHI 0031)
• ARM Embedded Trace Macrocell Architecture Specification (ARM IHI 0014).
Other publications

This section lists relevant documents published by third parties:

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on this manual

If you have comments on content then send e-mail to errata@arm.com. Give:

- the title
- the number, ARM DDI 0337I
- the page number(s) to which your comments refer
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.
Chapter 1
Introduction

This chapter introduces the processor and instruction set. It contains the following sections:

- About the processor on page 1-2
- Features on page 1-3
- Interfaces on page 1-4
- Configurable options on page 1-5
- Product documentation on page 1-6
- Product revisions on page 1-9.
1.1 About the processor

The Cortex-M3 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require optimal interrupt response features.
1.2 Features

The Cortex-M3 processor incorporates:

- a processor core
- a Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing
- multiple high-performance bus interfaces
- a low-cost debug solution with the optional ability to:
  - implement breakpoints and code patches
  - implement watchpoints, tracing, and system profiling
  - support printf() style debugging.
  - bridge to a Trace Port Analyzer (TPA).
- an optional Memory Protection Unit (MPU).
1.3 Interfaces

The processor has the following external interfaces:

- multiple memory and device bus interfaces
- ETM interface
- trace port interface
- debug port interface
- if the implementation includes an ETM, a *Cross Trigger Interface* (CTI).
1.4 Configurable options

You can configure your Cortex-M3 implementation to include the following optional components:

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**Note**

You can only configure trace functionality in the following combinations:

- no trace functionality
- ITM and DWT
- ITM, DWT, and ETM
- ITM, DWT, ETM, and HTM.

You can configure the debug features provided in the DWT independently.
1.5 Product documentation

This section describes the processor books, how they relate to the design flow, and the relevant architectural standards and protocols.

See Additional reading on page xi for more information about the books described in this section.

1.5.1 Documentation

The Cortex-M3 documentation is as follows:


The Technical Reference Manual (TRM) describes the functionality and the effects of functional options on the behavior of the Cortex-M3 processor. It is required at all stages of the design flow. Some behavior described in the TRM might not be relevant because of the way that the Cortex-M3 processor is implemented and integrated. If you are programming the Cortex-M3 processor then contact:

• the implementer to determine:
  — the build configuration of the implementation
  — what integration, if any, was performed before implementing the processor.
• the integrator to determine the pin configuration of the SoC that you are using.

Integration and Implementation Manual

The Integration and Implementation Manual (IIM) describes:

• The available build configuration options and related issues in selecting them.
• How to configure the Register Transfer Level (RTL) with the build configuration options.
• How to integrate the processor into a SoC. This includes a description of the integration kit and describes the pins that the integrator must tie off to configure the macrocell for the required integration.
• How to implement the processor into your design. This includes floorplanning guidelines, Design for Test (DFT) information, and how to perform netlist dynamic verification on the processor.
• The processes to sign off the integration and implementation of the design.

The ARM product deliverables include reference scripts and information about using them to implement your design.

Reference methodology documentation from your EDA tools vendor complements the IIM.

The IIM is a confidential book that is only available to licensees.

Cortex-M3 User Guide Reference Material

This document provides reference material that ARM partners can configure and include in a User Guide for an ARM Cortex-M3 processor. Typically:

• each chapter in this reference material might correspond to a section in the User Guide
1.5.2 Design Flow

The processor is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following process:

**Implementation**

The implementer configures the RTL and may synthesize it to produce a hard macrocell or may synthesize the whole design after implementation.

**Integration**

The integrator connects the implemented design into a SoC. This includes connecting it to a memory system and peripherals.

**Programming**

The system programmer develops the software required to configure and initialize the processor, and tests the required application software.

Each stage in the process can be performed by a different party. Implementation and integration choices affect the behavior and features of the processor.

For MCUs, often a single design team integrates the processor before synthesizing the complete design. Alternatively, the team can synthesise the processor on its own or partially integrated, to produce a macrocell that is then integrated, possibly by a separate team.

The operation of the final device depends on:

**Build configuration**

The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

**Configuration inputs**

The integrator configures some features of the processor by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

**Software configuration**

The programmer configures the processor by programming particular values into registers. This affects the behavior of the processor.

---

**Note**

This manual refers to implementation-defined features that are applicable to build configuration options. Reference to a feature that is included means that the appropriate build and pin configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

1.5.3 Architecture and protocol information

The processor complies with, or implements, the specifications described in:

- *ARM architecture* on page 1-8
• **Bus architecture**
• **Debug**
• **Embedded Trace Macrocell.**

This book complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

**ARM architecture**

The processor implements the ARMv7-M architecture profile. See the *ARMv7-M Architecture Reference Manual.*

For more information about architectural compliance, see Architecture and protocol information on page 1-9.

**Bus architecture**

The processor provides three primary bus interfaces implementing a variant of the AMBA 3 AHB-Lite protocol. The processor implements an interface for CoreSight and other debug components using the AMBA 3 APB protocol. See:

- the *ARM AMBA 3 AHB-Lite Protocol (v1.0)*
- the *ARM AMBA 3 APB Protocol Specification.*

**Debug**

The debug features of the processor implement the ARM debug interface architecture. See the *ARM Debug Interface v5 Architecture Specification.* The processor also implements debug features defined by the ARMv7-M. See the *ARMv7-M Architecture Reference Manual.*

**Embedded Trace Macrocell**

The trace features of the processor implement version 3.4 of the ARM Embedded Trace Macrocell architecture. See the *ARM Embedded Trace Macrocell Architecture Specification.*
1.6 Product revisions

This section summarizes the differences in functionality between the different releases of this processor:

- Differences in functionality between r0p0 and r1p0
- Differences in functionality between r1p0 and r1p1
- Differences in functionality between r1p1 and r2p0 on page 1-10
- Differences in functionality between r2p0 and r2p1 on page 1-10.

1.6.1 Differences in functionality between r0p0 and r1p0

In summary, the differences in functionality include:

- Addition of configurable data value comparison to the DWT module.
- Addition of a MATCHED bit to DWT_FUNCTION.
- Addition of configurable ETMFIFOFULL stalling functionality to the processor and the ETM.
- Addition of SWV Mode to the ITM.
- CPUID Base Register VARIANT field changed to indicate Rev1.
- Cortex-M3 Rev0 Bit-band accesses in BE8 mode required access sizes to be byte. Cortex-M3 Rev1 has been changed so that BE8 bit-band accesses function with any access size.
- Addition of a configuration bit called STKALIGN to ensure that all exceptions have eight-byte stack alignment.
- Addition of the Auxiliary Fault Status Register at address 0xE000ED3C. To set this register, a 32-bit input bus called AUXFAULT has been added.
- Addition of HTM support.
- ICode and DCode cacheable and bufferable HPROT values permanently tied to write-through.
- Addition of the SWJ-DP. This is the standard CoreSight™ debug port that combines JTAG-DP and SW-DP.
- Addition of DWT_PCSR Register at address 0xE000101C.
- Errata fixes to the r0p0 release.

1.6.2 Differences in functionality between r1p0 and r1p1

In summary, the differences in functionality include:

- Data value matching for watchpoint generation has been made implementation time configurable.
- Architectural clock gating in the ETM is configurable at implementation.
- DAPCLKEN was required to be a static signal in r0p0 and r1p0. This requirement has been removed for r1p1.
- SLEEPING signal now suppressed until current outstanding instruction fetch has completed.
• Errata fixes to the r1p0 release.

1.6.3 Differences in functionality between r1p1 and r2p0

In summary, the differences in functionality include:

• Implementation time options have been added to select between different levels of debug and trace support. This has replaced the previous TIEOFF_FPBEN and TIEOFF_TRCENA options.

• New implementation option to enable the resetting of all registers within the processor.

• Architectural clock gating inclusion is now controlled using one implementation option.

• DBGRESTART input and DBGRESTARTED output have been added for use in debugging multi-core systems. See the ARMv7-M Architecture Reference Manual for more information.

• SLEEPHOLDREQn input and SLEEPHOLDACKn have been added to enable the extension of SLEEPING.

• The APB interface has been upgraded from v2.0 to v3.0.

• A new output signal called INTERNALSTATE has been added that enables observation of some of the internal state of the core if the OBSERVATION implementation option is used.

• Added support for fault-robust implementations.

• An Auxiliary Control Register has been added with new functionality disable bits to:
  — stop interruption of load/store multiples, divides and multiplies
  — stop IT folding
  — disable the write buffers in Cortex-M3 for default memory map accesses.

• The STKALIGN bit reset value in the Configuration and Control Register at address 0xE000ED14 has been inverted. The reset value is now 1, which means that the stack frame is 8-byte aligned by default.

• Addition of a Wake-up Interrupt Controller to minimize logic in the always clocked domain during sleep.

• Addition of FIXHMASTERTYPE pin to prevent debugger marking AHB transactions as core data side if required.

• Improved sequential information for data accesses. Before r2p0 HPROT for sequential data accesses would change from SEQ to NSEQ if wait-states were inserted for the previous access. r2p0 maintains the SEQ information.

• Errata fixes to the r1p1 release.

1.6.4 Differences in functionality between r2p0 and r2p1

In summary, the differences in functionality include:

• New implementation option to ensure constant AHB control during wait-stated transfers.

• New implementation option to remove the bit-banding logic.

• MPUDISABLE input added to disable the MPU via hardware.
- **DBGEN** input added as master debug enable. If de-asserted then debug is disabled.
- ETM upgraded from ARM ETM architecture v3.4 to 3.5 to include global time-stamping.
- The Vector Table Offset Register located at address 0xE000ED08 has been increased by two bits from 29:7 to 31:7.
- ROM table identification registers have been updated. See Cortex-M3 ROM table identification and entries on page 7-3.
- Verilog file and module names have been modified. The top module names for Cortex-M3 and the integration layer are now in capitals: CORTEXM3 and CORTEXM3INTEGRATION.
- The ETM license define name has changed to ARM_CM3_ETM_LICENSE and is now defined in cm3_lic_defs.v rather than in the integration level.
- Watchpoints no longer occur if the transaction is aborted by the MPU.
- Errata fixes to the r2p0 release.
Chapter 2
Functional Description

This chapter introduces the processor and its external interfaces. It contains the following sections:

- About the functions on page 2-2
- Interfaces on page 2-4.
2.1 About the functions

Figure 2-1 shows the structure of the Cortex-M3 processor.

The Cortex-M3 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - Banked Stack Pointer (SP).
  - Hardware integer divide instructions, SDIV and UDIV.
  - Handler and Thread modes.
  - Thumb and Debug states.
  - Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency.
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit.
  - Support for ARMv6 big-endian byte-invariant or little-endian accesses.
  - Support for ARMv6 unaligned accesses.
• **Nested Vectored Interrupt Controller** (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  — External interrupts, configurable from 1 to 240.
  — Bits of priority, configurable from 3 to 8.
  — Dynamic reprioritization of interrupts.
  — Priority grouping. This enables selection of preempting interrupt levels and non preempting interrupt levels.
  — Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  — Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.
  — Optional **Wake-up Interrupt Controller** (WIC), providing ultra-low power sleep mode support.

• **Memory Protection Unit** (MPU). An optional MPU for memory protection, including:
  — Eight memory regions.
  — **Sub Region Disable** (SRD), enabling efficient use of memory regions.
  — The ability to enable a background region that implements the default memory map attributes.

• Bus interfaces:
  — Three **Advanced High-performance Bus-Lite** (AHB-Lite) interfaces: ICode, DCode, and System bus interfaces.
  — **Private Peripheral Bus** (PPB) based on **Advanced Peripheral Bus** (APB) interface.
  — Bit-band support that includes atomic bit-band write and read operations.
  — Memory access alignment.
  — Write buffer for buffering of write data.
  — Exclusive access transfers for multiprocessor systems.

• Low-cost debug solution that features:
  — Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while **SYSRESETn** is asserted.
  — **Serial Wire Debug Port** (SW-DP) or **Serial Wire JTAG Debug Port** (SWJ-DP) debug access.
  — Optional **Flash Patch and Breakpoint** (FPB) unit for implementing breakpoints and code patches.
  — Optional **Data Watchpoint and Trace** (DWT) unit for implementing watchpoints, data tracing, and system profiling.
  — Optional **Instrumentation Trace Macrocell** (ITM) for support of **printf()** style debugging.
  — Optional **Trace Port Interface Unit** (TPIU) for bridging to a **Trace Port Analyzer** (TPA), including **Single Wire Output** (SWO) mode.
  — Optional **Embedded Trace Macrocell** (ETM) for instruction trace.
2.2 Interfaces

The processor contains the following external interfaces:

- Bus interfaces
- ETM interface on page 2-6
- AHB Trace Macrocell interface on page 2-6
- Debug Port AHB-AP interface on page 2-6.

2.2.1 Bus interfaces

The processor contains three external Advanced High-performance Bus (AHB)-Lite bus interfaces and one Advanced Peripheral Bus (APB) interface:

- ICode memory interface
- DCode memory interface on page 2-5
- System interface on page 2-5
- Private Peripheral Bus (PPB) on page 2-5.

The processor matches the AMBA 3 specification except for maintaining control information during waited transfers. The AMBA 3 AHB-Lite Protocol states that when the slave is requesting wait states the master must not change the transfer type, except for the following cases:

- On an IDLE transfer, the master can change the transfer type from IDLE to NONSEQ.
- On a BUSY transfer with a fixed length burst, the master can change the transfer type from BUSY to SEQ.
- On a BUSY transfer with an undefined length burst, the master can change the transfer type from BUSY to any other transfer type.

The processor does not match this definition because it might change the access type from SEQ or NONSEQ to IDLE during a waited transfer. The processor might also change the address or other control information and therefore request an access to a new location. The original address that was retracted might not be requested again. This cancels the outstanding transfer that has not occurred because the previous access is wait-stated and awaiting completion. This is done so that the processor can have a lower interrupt latency and higher performance in wait-stated systems by retracting accesses that are no longer required.

To achieve complete compliance with the AMBA 3 specification you can implement the design with the AHB_CONST_CTRL parameter set to 1. This ensures that once transfers are issued during a wait-stated response they are never retracted or modified and the original transfer is honoured. The consequence of setting this parameter is that the performance of the core might decrease for wait-stated systems as a result of the interrupt and branch latency increasing.

ICode memory interface

Instruction fetches from Code memory space, $0x00000000$ to $0xFFFFFFFF$, are performed over this 32-bit AHB-Lite bus.

The Debugger cannot access this interface. All fetches are word-wide. The number of instructions fetched per word depends on the code running and the alignment of the code in memory.
DCode memory interface

Data and debug accesses to Code memory space, \(0x00000000\) to \(0xFFFFFFFF\), are performed over this 32-bit AHB-Lite bus. Core data accesses have a higher priority than debug accesses on this bus. This means that debug accesses are waited until core accesses have completed when there are simultaneous core and debug access to this bus.

Control logic in this interface converts unaligned data and debug accesses into two or three aligned accesses, depending on the size and alignment of the unaligned access. This stalls any subsequent data or debug access until the unaligned access has completed.

Note

ARM strongly recommends that any external arbitration between the ICode and DCode AHB bus interfaces ensures that DCode has a higher priority than ICode.

System interface

Instruction fetches, and data and debug accesses, to address ranges \(0x20000000\) to \(0x2FFFFFFF\) and \(0xE0100000\) to \(0xFFFFFFFF\) are performed over this 32-bit AHB-Lite bus.

For simultaneous accesses to this bus, the arbitration order in decreasing priority is:

- data accesses
- instruction and vector fetches
- debug.

The system bus interface contains control logic to handle unaligned accesses, FPB remapped accesses, bit-band accesses, and pipelined instruction fetches.

Private Peripheral Bus (PPB)

Data and debug accesses to external PPB space, \(0xE0040000\) to \(0xE00FFFFF\), are performed over this 32-bit Advanced Peripheral Bus (APB) bus. The Trace Port Interface Unit (TPIU) and vendor specific peripherals are on this bus.

Core data accesses have higher priority than debug accesses, so debug accesses are waited until core accesses have completed when there are simultaneous core and debug access to this bus. Only the address bits necessary to decode the External PPB space are supported on this interface.

The External PPB (EPPB) space, \(0xE0040000\) up to \(0xE0100000\), is intended for CoreSight-compatible debug and trace components, and has a number of irregular limitations which make it less useful for regular system peripherals. ARM recommends that system peripherals are placed in suitable Device type areas of the System bus address space, with use of an AHB2APB protocol converter for APB-based devices.

Limitations of the EPPB space are:

- it is accessible in privileged mode only
- it is accessed in little-endian fashion irrespective of the data endianness setting of the processor
- accesses behave as Strongly Ordered
- no bit-band function is available
- unaligned accesses have Unpredictable results
• only 32-bit data accesses are supported
• it is accessible from the Debug Port and the local processor, but not from any other processor in the system.

2.2.2 ETM interface

The ETM interface enables simple connection of an ETM to the processor. It provides a channel for instruction trace to the ETM. See the *ARM Embedded Trace Macrocell Architecture Specification*.

2.2.3 AHB Trace Macrocell interface

The *AHB Trace Macrocell* (HTM) interface enables a simple connection of the AHB trace macrocell to the processor. It provides a channel for the data trace to the HTM.

Your implementation must include this interface to use the HTM interface. You must set TRCENA to 1 in the Debug Exception and Monitor Control Register (DEMCR) before you enable the HTM port to supply trace data. See the *ARMv7-M Architecture Reference Manual*.

2.2.4 Debug Port AHB-AP interface

The processor contains an *Advanced High-performance Bus Access Port* (AHB-AP) interface for debug accesses. An external *Debug Port* (DP) component accesses this interface. The Cortex-M3 system supports three possible DP implementations:

- The *Serial Wire JTAG Debug Port* (SWJ-DP). The SWJ-DP is a standard CoreSight debug port that combines JTAG-DP and *Serial Wire Debug Port* (SW-DP).
- The SW-DP. This provides a two-pin interface to the AHB-AP port.
- No DP present. If no debug functionality is present within the processor, a DP is not required.

The two DP implementations provide different mechanisms for debug access to the processor. Your implementation must contain only one of these components.

________ Note ________

Your implementation might contain an alternative implementer-specific DP instead of SW-DP or SWJ-DP. See your implementer for details.

For more detailed information on the DP components, see the *CoreSight Components Technical Reference manual*.

For more information on the AHB-AP, see Chapter 7 *Debug*.

The DP and AP together are referred to as the *Debug Access Port* (DAP).

For more detailed information on the debug interface, see the *ARM Debug Interface v5 Architecture Specification*. 
Chapter 3
Programmers Model

This chapter describes the processor programmers model. It contains the following sections:

• About the programmers model on page 3-2
• Modes of operation and execution on page 3-3
• Instruction set summary on page 3-4
• System address map on page 3-11
• Write buffer on page 3-14
• Bit-banding on page 3-16
• Processor core register summary on page 3-18
• Exceptions on page 3-20.
3.1 About the programmers model

The *ARMv7-M Architecture Reference Manual* provides a complete description of the programmers model. This chapter gives an overview of the Cortex-M3 processor programmers model that describes the implementation-defined options. It also contains the ARMv7-M Thumb instructions the model uses, and their cycle counts for the processor. In addition:

- Chapter 4 summarizes the system control features of the programmers model
- Chapter 5 summarizes the MPU features of the programmers model
- Chapter 6 summarizes the NVIC features of the programmers model
- Chapter 7 summarizes the Debug features of the programmers model
- Chapter 8 summarizes the DWT features of the programmers model
- Chapter 9 summarizes the ITM features of the programmers model
- Chapter 10 summarizes the ETM features of the programmers model
- Chapter 11 summarizes the TPIU features of the programmers model.
3.2 Modes of operation and execution

This section briefly describes the modes of operation and execution of the Cortex-M3 processor. See the *ARMv7-M Architecture Reference Manual* for more information.

3.2.1 Operating modes

The processor supports two modes of operation, Thread mode and Handler mode:

- The processor enters Thread mode on Reset, or as a result of an exception return. Privileged and Unprivileged code can run in Thread mode.
- The processor enters Handler mode as a result of an exception. All code is privileged in Handler mode.

3.2.2 Operating states

The processor can operate in one of two operating states:

- Thumb state. This is normal execution running 16-bit and 32-bit halfword aligned Thumb instructions.
- Debug State. This is the state when the processor is in halting debug.

3.2.3 Privileged access and user access

Code can execute as privileged or unprivileged. Unprivileged execution limits or excludes access to some resources. Privileged execution has access to all resources. Handler mode is always privileged. Thread mode can be privileged or unprivileged.
3.3 Instruction set summary

This section provides information on:

- Cortex-M3 instructions
- Load/store timings on page 3-8
- Binary compatibility with other Cortex processors on page 3-9.

3.3.1 Cortex-M3 instructions

The processor implements the ARMv7-M Thumb instruction set. Table 3-1 shows the Cortex-M3 instructions and their cycle counts. The cycle counts are based on a system with zero wait states.

Within the assembler syntax, depending on the operation, the <op2> field can be replaced with one of the following options:

- a simple register specifier, for example Rm
- an immediate shifted register, for example Rm, LSL #4
- a register shifted register, for example Rm, LSL Rs
- an immediate value, for example #0xE000E000.

For brevity, not all load and store addressing modes are shown. See the ARMv7-M Architecture Reference Manual for more information.

Table 3-1 uses the following abbreviations in the Cycles column:

- **P** The number of cycles required for a pipeline refill. This ranges from 1 to 3 depending on the alignment and width of the target instruction, and whether the processor manages to speculate the address early.
- **B** The number of cycles required to perform the barrier operation. For DSB and DMB, the minimum number of cycles is zero. For ISB, the minimum number of cycles is equivalent to the number required for a pipeline refill.
- **N** The number of registers in the register list to be loaded or stored, including PC or LR.
- **W** The number of cycles spent waiting for an appropriate event.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Description</th>
<th>Assembler</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Move</td>
<td>Register</td>
<td>MOV Rd, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>16-bit immediate</td>
<td>MOVW Rd, #&lt;imm&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Immediate into top</td>
<td>MOVT Rd, #&lt;imm&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>To PC</td>
<td>MOV PC, Rm</td>
<td>1 + P</td>
</tr>
<tr>
<td>Add</td>
<td>Add</td>
<td>ADD Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Add to PC</td>
<td>ADD PC, PC, Rn</td>
<td>1 + P</td>
</tr>
<tr>
<td></td>
<td>Add with carry</td>
<td>ADC Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Form address</td>
<td>ADR Rd, &lt;label&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Operation</td>
<td>Description</td>
<td>Assembler</td>
<td>Cycles</td>
</tr>
<tr>
<td>----------------------------</td>
<td>---------------------------</td>
<td>----------------</td>
<td>--------</td>
</tr>
<tr>
<td>Subtract</td>
<td>Subtract</td>
<td>SUB Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Subtract with borrow</td>
<td>SBC Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Reverse</td>
<td>RSB Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Multiply</td>
<td>Multiply</td>
<td>MUL Rd, Rn, Rm</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Multiply accumulate</td>
<td>MLA Rd, Rn, Rm</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>Multiply subtract</td>
<td>MLS Rd, Rn, Rm</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>Long signed</td>
<td>SMULL RdLo, RdHi, Rn, Rm</td>
<td>3 to 5&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>Long unsigned</td>
<td>UMULL RdLo, RdHi, Rn, Rm</td>
<td>3 to 5&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>Long signed accumulate</td>
<td>SMLAL RdLo, RdHi, Rn, Rm</td>
<td>4 to 7&lt;sup&gt;a&lt;/sup&gt;</td>
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<td>Long unsigned accumulate</td>
<td>UMLAL RdLo, RdHi, Rn, Rm</td>
<td>4 to 7&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td>Divide</td>
<td>Signed</td>
<td>SDIV Rd, Rn, Rm</td>
<td>2 to 12&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>Unsigned</td>
<td>UDIV Rd, Rn, Rm</td>
<td>2 to 12&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td>Saturate</td>
<td>Signed</td>
<td>SSAT Rd, #&lt;imm&gt;, &lt;op2&gt;</td>
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</tr>
<tr>
<td></td>
<td>Unsigned</td>
<td>USAT Rd, #&lt;imm&gt;, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Compare</td>
<td>Compare</td>
<td>CMP Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Negative</td>
<td>CMN Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Logical</td>
<td>AND</td>
<td>AND Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Exclusive OR</td>
<td>EOR Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
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<td></td>
<td>OR</td>
<td>ORR Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
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<td></td>
<td>OR NOT</td>
<td>ORN Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
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<td></td>
<td>Bit clear</td>
<td>BIC Rd, Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Move NOT</td>
<td>MVN Rd, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>AND test</td>
<td>TST Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Exclusive OR test</td>
<td>TEQ Rn, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Shift</td>
<td>Logical shift left</td>
<td>LSL Rd, Rn, #&lt;imm&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Logical shift left</td>
<td>LSL Rd, Rn, Rs</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Logical shift right</td>
<td>LSR Rd, Rn, #&lt;imm&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Logical shift right</td>
<td>LSR Rd, Rn, Rs</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Arithmetic shift right</td>
<td>ASR Rd, Rn, #&lt;imm&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Arithmetic shift right</td>
<td>ASR Rd, Rn, Rs</td>
<td>1</td>
</tr>
<tr>
<td>Operation</td>
<td>Description</td>
<td>Assembler</td>
<td>Cycles</td>
</tr>
<tr>
<td>-----------------</td>
<td>---------------------</td>
<td>-------------</td>
<td>--------</td>
</tr>
<tr>
<td>Rotate</td>
<td>Rotate right</td>
<td>ROR Rd, Rn, #&lt;imm&gt;</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Rotate right</td>
<td>ROR Rd, Rn, Rs</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>With extension</td>
<td>RX Rd, Rn</td>
<td>1</td>
</tr>
<tr>
<td>Count</td>
<td>Leading zeroes</td>
<td>CLZ Rd, Rn</td>
<td>1</td>
</tr>
<tr>
<td>Load</td>
<td>Word</td>
<td>LDR Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>To PC</td>
<td>LDR PC, [Rn, &lt;op2&gt;]</td>
<td>2c + P</td>
</tr>
<tr>
<td></td>
<td>Halfword</td>
<td>LDRH Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Byte</td>
<td>LDRB Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Signed halfword</td>
<td>LDRSH Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Signed byte</td>
<td>LDRSB Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User word</td>
<td>LDRT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User halfword</td>
<td>LDRHT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User byte</td>
<td>LDRBT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User signed halfword</td>
<td>LDRSHT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User signed byte</td>
<td>LDRSBT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>PC relative</td>
<td>LDR [PC, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Doubleword</td>
<td>LDRD Rd, Rd, [Rn, #&lt;imm&gt;]</td>
<td>1 + N</td>
</tr>
<tr>
<td></td>
<td>Multiple</td>
<td>LDM Rn, {&lt;reglist&gt;}</td>
<td>1 + N</td>
</tr>
<tr>
<td></td>
<td>Multiple including PC</td>
<td>LDM Rn, {&lt;reglist&gt;, PC}</td>
<td>1 + N + P</td>
</tr>
<tr>
<td>Store</td>
<td>Word</td>
<td>STR Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Halfword</td>
<td>STRH Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Byte</td>
<td>STRB Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Signed halfword</td>
<td>STRSH Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Signed byte</td>
<td>STRSB Rd, [Rn, &lt;op2&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User word</td>
<td>STRT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User halfword</td>
<td>STRHT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User byte</td>
<td>STRBT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User signed halfword</td>
<td>STRSHT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>User signed byte</td>
<td>STRSBT Rd, [Rn, #&lt;imm&gt;]</td>
<td>2c</td>
</tr>
<tr>
<td></td>
<td>Doubleword</td>
<td>STRD Rd, Rd, [Rn, #&lt;imm&gt;]</td>
<td>1 + N</td>
</tr>
<tr>
<td></td>
<td>Multiple</td>
<td>STM Rn, {&lt;reglist&gt;}</td>
<td>1 + N</td>
</tr>
</tbody>
</table>
### Table 3-1 Cortex-M3 instruction set summary (continued)

<table>
<thead>
<tr>
<th>Operation</th>
<th>Description</th>
<th>Assembler</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push</td>
<td>Push</td>
<td>PUSH {&lt;reglist&gt;}</td>
<td>1 + N</td>
</tr>
<tr>
<td>Push</td>
<td>Push with link register</td>
<td>PUSH {&lt;reglist&gt;, LR}</td>
<td>1 + N</td>
</tr>
<tr>
<td>Pop</td>
<td>Pop</td>
<td>POP {&lt;reglist&gt;}</td>
<td>1 + N</td>
</tr>
<tr>
<td>Pop</td>
<td>Pop and return</td>
<td>POP {&lt;reglist&gt;, PC}</td>
<td>1 + N + P</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Load exclusive</td>
<td>LDREX Rd, [Rn, #&lt;imm&gt;]</td>
<td>2</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Load exclusive half</td>
<td>LDREXH Rd, [Rn]</td>
<td>2</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Load exclusive byte</td>
<td>LDREXB Rd, [Rn]</td>
<td>2</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Store exclusive</td>
<td>STREX Rd, Rt, [Rn, #&lt;imm&gt;]</td>
<td>2</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Store exclusive half</td>
<td>STREXH Rd, Rt, [Rn]</td>
<td>2</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Store exclusive byte</td>
<td>STREXB Rd, Rt, [Rn]</td>
<td>2</td>
</tr>
<tr>
<td>Semaphore</td>
<td>Clear exclusive monitor</td>
<td>CLREX</td>
<td>1</td>
</tr>
<tr>
<td>Branch</td>
<td>Conditional</td>
<td>B&lt;cc&gt; &lt;label&gt;</td>
<td>1 or 1 + Pd</td>
</tr>
<tr>
<td>Branch</td>
<td>Unconditional</td>
<td>B &lt;label&gt;</td>
<td>1 + P</td>
</tr>
<tr>
<td>Branch</td>
<td>With link</td>
<td>BL &lt;label&gt;</td>
<td>1 + P</td>
</tr>
<tr>
<td>Branch</td>
<td>With exchange</td>
<td>BX Rm</td>
<td>1 + P</td>
</tr>
<tr>
<td>Branch</td>
<td>With link and exchange</td>
<td>BLX Rm</td>
<td>1 + P</td>
</tr>
<tr>
<td>Branch</td>
<td>Branch if zero</td>
<td>CBZ Rn, &lt;label&gt;</td>
<td>1 or 1 + Pd</td>
</tr>
<tr>
<td>Branch</td>
<td>Branch if non-zero</td>
<td>CBNZ Rn, &lt;label&gt;</td>
<td>1 or 1 + Pd</td>
</tr>
<tr>
<td>Branch</td>
<td>Byte table branch</td>
<td>TBB [Rn, Rm]</td>
<td>2 + P</td>
</tr>
<tr>
<td>Branch</td>
<td>Halfword table branch</td>
<td>THB [Rn, Rm, LSL#1]</td>
<td>2 + P</td>
</tr>
<tr>
<td>State change</td>
<td>Supervisor call</td>
<td>SVC #&lt;imm&gt;</td>
<td>-</td>
</tr>
<tr>
<td>State change</td>
<td>If-then-else</td>
<td>IT... &lt;cond&gt;</td>
<td>1e</td>
</tr>
<tr>
<td>State change</td>
<td>Disable interrupts</td>
<td>CPSID &lt;Flags&gt;</td>
<td>1 or 2</td>
</tr>
<tr>
<td>State change</td>
<td>Enable interrupts</td>
<td>CPSIE &lt;Flags&gt;</td>
<td>1 or 2</td>
</tr>
<tr>
<td>State change</td>
<td>Read special register</td>
<td>MRS Rd, &lt;specreg&gt;</td>
<td>1 or 2</td>
</tr>
<tr>
<td>State change</td>
<td>Write special register</td>
<td>MSR &lt;specreg&gt;, Rn</td>
<td>1 or 2</td>
</tr>
<tr>
<td>State change</td>
<td>Breakpoint</td>
<td>BKPT #&lt;imm&gt;</td>
<td>-</td>
</tr>
<tr>
<td>Extend</td>
<td>Signed halfword to word</td>
<td>SXTH Rd, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Extend</td>
<td>Signed byte to word</td>
<td>SXTB Rd, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Extend</td>
<td>Unsigned halfword</td>
<td>UXTH Rd, &lt;op2&gt;</td>
<td>1</td>
</tr>
<tr>
<td>Extend</td>
<td>Unsigned byte</td>
<td>UXTB Rd, &lt;op2&gt;</td>
<td>1</td>
</tr>
</tbody>
</table>
3.3.2 Load/store timings

This section describes how best to pair instructions to achieve more reductions in timing.

- STR Rx, [Ry, #imm] is always one cycle. This is because the address generation is performed in the initial cycle, and the data store is performed at the same time as the next instruction is executing. If the store is to the write buffer, and the write buffer is full or not enabled, the next instruction is delayed until the store can complete. If the store is not to the write buffer, for example to the Code segment, and that transaction stalls, the impact on timing is only felt if another load or store operation is executed before completion.

- Any load with a base update is not normally pipelined. That is, base update load is generally at least a two-cycle operation (more if stalled). However, if the next instruction does not require to read from a register, the load is reduced to one cycle. Non register writing instructions include CMP, TST, NOP, and non-taken IT controlled instructions.

- LDR PC, [any] is always a blocking operation. This means at least two cycles for the load, and three cycles for the pipeline reload. So this operation takes at least five cycles, or more if stalled on the load or the fetch.
• Any load or store that generates an address dependent on the result of a proceeding data processing operation will stall the pipeline for an additional cycle whilst the register bank is updated. There is no forwarding path for this scenario.

• \texttt{LDR Rx,[PC,#imm]} might add a cycle because of contention with the fetch unit.

• \texttt{TBB} and \texttt{TBH} are also blocking operations. These are at least two cycles for the load, one cycle for the add, and three cycles for the pipeline reload. This means at least six cycles, or more if stalled on the load or the fetch.

• \texttt{LDR [any]} are pipelined when possible. This means that if the next instruction is an \texttt{LDR} or \texttt{STR}, and the destination of the first \texttt{LDR} is not used to compute the address for the next instruction, then one cycle is removed from the cost of the next instruction. So, an \texttt{LDR} might be followed by an \texttt{STR}, so that the \texttt{STR} writes out what the \texttt{LDR} loaded. More multiple \texttt{LDR}s can be pipelined together. Some optimized examples are:
  
  — \texttt{LDR R0,[R1]; LDR R1,[R2]} - normally three cycles total
  
  — \texttt{LDR R0,[R1,R2]; STR R0,[R3,#20]} - normally three cycles total
  
  — \texttt{LDR R0,[R1,R2]; STR R1,[R3,R2]} - normally three cycles total
  
  — \texttt{LDR R0,[R1,R5]; LDR R1,[R2]; LDR R2,[R3,#4]} - normally four cycles total.

• Other instructions cannot be pipelined after \texttt{STR} with register offset. \texttt{STR} can only be pipelined when it follows an \texttt{LDR}, but nothing can be pipelined after the store. Even a stalled \texttt{STR} normally only takes two cycles, because of the write buffer.

• \texttt{LDREX} and \texttt{STREX} can be pipelined exactly as \texttt{LDR}. Because \texttt{STREX} is treated more like an \texttt{LDR}, it can be pipelined as explained for \texttt{LDR}. Equally \texttt{LDREX} is treated exactly as an \texttt{LDR} and so can be pipelined.

• \texttt{LDRD} and \texttt{STRD} cannot be pipelined with preceding or following instructions. However, the two words are pipelined together. So, this operation requires three cycles when not stalled.

• \texttt{LDM} and \texttt{STM} cannot be pipelined with preceding or following instructions. However, all elements after the first are pipelined together. So, a three element \texttt{LDM} takes \(2+1+1\) or 5 cycles when not stalled. Similarly, an eight element store takes nine cycles when not stalled. When interrupted, \texttt{LDM} and \texttt{STM} instructions continue from where they left off when returned to. The continue operation adds one or two cycles to the first element when started.

• Unaligned word or halfword loads or stores add penalty cycles. A byte aligned halfword load or store adds one extra cycle to perform the operation as two bytes. A halfword aligned word load or store adds one extra cycle to perform the operation as two halfwords. A byte-aligned word load or store adds two extra cycles to perform the operation as a byte, a halfword, and a byte. These numbers increase if the memory stalls. A \texttt{STR} or \texttt{STRH} cannot delay the processor because of the write buffer.

### 3.3.3 Binary compatibility with other Cortex processors

The processor implements a binary compatible subset of the instruction set and features provided by other Cortex-M profile processors. You can move software, including system level software, from the Cortex-M3 processor to other Cortex-M profile processors.

To ensure a smooth transition, ARM recommends that code designed to operate on other Cortex-M profile processor architectures obey the following rules and configure the \textit{Configuration and Control Register (CCR)} appropriately:

• use word transfers only to access registers in the NVIC and \textit{System Control Space (SCS)}.

• treat all unused SCS registers and register fields on the processor as Do-Not-Modify.
• configure the following fields in the CCR:
  — STKALIGN bit to 1
  — UNALIGN_TRP bit to 1
  — Leave all other bits in the CCR register as their original value.
3.4 System address map

The processor contains a bus matrix that arbitrates the processor core and optional *Debug Access Port* (DAP) memory accesses to both the external memory system and to the internal *System Control Space* (SCS) and debug components.

Priority is always given to the processor to ensure that any debug accesses are as non-intrusive as possible. For a zero wait state system, all debug accesses to system memory, SCS, and debug resources are completely non-intrusive.

Figure 3-1 shows the system address map.

Table 3-2 shows the processor interfaces that are addressed by the different memory map regions.

**Table 3-2 Memory regions**

<table>
<thead>
<tr>
<th>Memory Map</th>
<th>Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Instruction fetches are performed over the ICode bus. Data accesses are performed over the DCode bus.</td>
</tr>
<tr>
<td>SRAM</td>
<td>Instruction fetches and data accesses are performed over the system bus.</td>
</tr>
<tr>
<td>SRAM bit-band</td>
<td>Alias region. Data accesses are aliases. Instruction accesses are not aliases.</td>
</tr>
<tr>
<td>Peripheral</td>
<td>Instruction fetches and data accesses are performed over the system bus.</td>
</tr>
</tbody>
</table>
3.4.1 Private peripheral bus

The internal Private Peripheral Bus (PPB) interface provides access to:

- the Instrumentation Trace Macrocell (ITM)
- the Data Watchpoint and Trace (DWT)
- the Flashpatch and Breakpoint (FPB)
- the System Control Space (SCS), including the MPU and the NVIC.

The external PPB interface provides access to:

- the TPIU
- the ETM
- the ROM table
- implementation-specific areas of the PPB memory map.

3.4.2 Unaligned accesses that cross regions

The Cortex-M3 processor supports ARMv7 unaligned accesses, and performs all accesses as single, unaligned accesses. They are converted into two or more aligned accesses by the DCode and System bus interfaces.

--- Note ---

All Cortex-M3 external accesses are aligned.

Unaligned support is only available for load/store singles (LDR, LDRH, STR, STRH). Load/store double already supports word aligned accesses, but does not permit other unaligned accesses, and generates a fault if this is attempted.

Unaligned accesses that cross memory map boundaries are architecturally Unpredictable. The processor behavior is boundary dependent, as follows:

- DCode accesses wrap within the region. For example, an unaligned halfword access to the last byte of Code space (0x1FFFFFFF) is converted by the DCode interface into a byte access to 0x1FFFFFFF followed by a byte access to 0x00000000.
- System accesses that cross into PPB space do not wrap within System space. For example, an unaligned halfword access to the last byte of System space (0xFFFFFFFF) is converted by the System interface into a byte access to 0xFFFFFFFF followed by a byte access to 0xE0000000. 0xE0000000 is not a valid address on the System bus.

- System accesses that cross into Code space do not wrap within System space. For example, an unaligned halfword access to the last byte of System space (0xFFFFFFFF) is converted by the System interface into a byte access to 0xFFFFFFFF followed by a byte access to 0x00000000. 0x00000000 is not a valid address on the System bus.

- Unaligned accesses are not supported to PPB space, and so there are no boundary crossing cases for PPB accesses.

Unaligned accesses that cross into the bit-band alias regions are also architecturally Unpredictable. The processor performs the access to the bit-band alias address, but this does not result in a bit-band operation. For example, an unaligned halfword access to 0x21FFFFFF is performed as a byte access to 0x21FFFFFF followed by a byte access to 0x22000000 (the first byte of the bit-band alias).

Unaligned loads that match against a literal comparator in the FPB are not remapped. FPB only remaps aligned addresses.
3.5 Write buffer

To prevent bus wait cycles from stalling the processor during data stores, buffered stores to the DCode and System buses go through a one-entry write buffer. If the write buffer is full, subsequent accesses to the bus stall until the write buffer has drained. The write buffer is only used if the bus waits the data phase of the buffered store, otherwise the transaction completes on the bus.

DMB and DSB instructions wait for the write buffer to drain before completing. If an interrupt comes in while DMB or DSB is waiting for the write buffer to drain, the processor returns to the instruction following the DMB or DSB after the interrupt completes. This is because interrupt processing acts as a memory barrier operation.
3.6 Exclusive monitor

The Cortex-M3 processor implements a local exclusive monitor. For more information about semaphores and the local exclusive monitor, see the *ARMv7M ARM Architecture Reference Manual*.

The local monitor within the processor has been constructed so that it does not hold any physical address, but instead treats any access as matching the address of the previous LDREX. This means that the implemented exclusives reservation granule is the entire memory address range.

The Cortex-M3 processor does not support exclusive accesses to bit-band regions.
### 3.7 Bit-banding

Bit-banding maps a complete word of memory onto a single bit in the bit-band region. For example, writing to one of the alias words sets or clears the corresponding bit in the bit-band region. This enables every individual bit in the bit-banding region to be directly accessible from a word-aligned address using a single `LDR` instruction. It also enables individual bits to be toggled without performing a read-modify-write sequence of instructions.

The processor memory map includes two bit-band regions. These occupy the lowest 1MB of the SRAM and Peripheral memory regions respectively. These bit-band regions map each word in an alias region of memory to a bit in a bit-band region of memory.

The System bus interface contains logic that controls bit-band accesses as follows:

- It remaps bit-band alias addresses to the bit-band region.
- For reads, it extracts the requested bit from the read byte, and returns this in the Least Significant Bit (LSB) of the read data returned to the core.
- For writes, it converts the write to an atomic read-modify-write operation.
- The processor does not stall during bit-band operations unless it attempts to access the System bus while the bit-band operation is being carried out.

The memory map has two 32-MB alias regions that map to two 1-MB bit-band regions:

- Accesses to the 32-MB SRAM alias region map to the 1-MB SRAM bit-band region.
- Accesses to the 32-MB peripheral alias region map to the 1-MB peripheral bit-band region.

A mapping formula shows how to reference each word in the alias region to a corresponding bit, or target bit, in the bit-band region. The mapping formula is:

\[
\text{bit\_word\_offset} = (\text{byte\_offset} \times 32) + (\text{bit\_number} \times 4) \\
\text{bit\_word\_addr} = \text{bit\_band\_base} + \text{bit\_word\_offset}
\]

where:

- `bit\_word\_offset` is the position of the target bit in the bit-band memory region.
- `bit\_word\_addr` is the address of the word in the alias memory region that maps to the targeted bit.
- `bit\_band\_base` is the starting address of the alias region.
- `byte\_offset` is the number of the byte in the bit-band region that contains the targeted bit.
- `bit\_number` is the bit position, 0 to 7, of the targeted bit.

Figure 3-2 on page 3-17 shows examples of bit-band mapping between the SRAM bit-band alias region and the SRAM bit-band region:

- The alias word at 0x23FFFFFFE0 maps to bit [0] of the bit-band byte at 0x20000000: 0x23FFFFFFE0 = 0x22000000 + (0xFFFFF*32) + 0*4.
- The alias word at 0x23FFFFFFF0 maps to bit [7] of the bit-band byte at 0x20000000: 0x23FFFFFFF0 = 0x22000000 + (0xFFFFF*32) + 7*4.
- The alias word at 0x22000000 maps to bit [0] of the bit-band byte at 0x20000000: 0x22000000 = 0x22000000 + (0*32) + 0*4.
• The alias word at 0x2200001C maps to bit [7] of the bit-band byte at 0x20000000: 0x2200001C = 0x20000000 + (0*32) + 7*4.

![Figure 3-2 Bit-band mapping](image)

### 3.7.1 Directly accessing an alias region

Writing to a word in the alias region has the same effect as a read-modify-write operation on the targeted bit in the bit-band region.

Bit [0] of the value written to a word in the alias region determines the value written to the targeted bit in the bit-band region. Writing a value with bit [0] set writes a 1 to the bit-band bit, and writing a value with bit [0] cleared writes a 0 to the bit-band bit.

Bits [31:1] of the alias word have no effect on the bit-band bit. Writing 0x01 has the same effect as writing 0xFF. Writing 0x00 has the same effect as writing 0x0E.

Reading a word in the alias region returns either 0x01 or 0x00. A value of 0x01 indicates that the targeted bit in the bit-band region is set. A value of 0x00 indicates that the targeted bit is clear. Bits [31:1] are zero.

### 3.7.2 Directly accessing a bit-band region

You can directly access the bit-band region with normal reads and writes to that region.
3.8 Processor core register summary

The processor has the following 32-bit registers:
- 13 general-purpose registers, R0-R12
- Stack Pointer (SP), R13 alias of banked registers, SP_process and SP_main
- Link Register (LR), R14
- Program Counter (PC), R15
- Special-purpose Program Status Registers, (xPSR).

Figure 3-3 shows the processor register set.

The general-purpose registers R0-R12 have no special architecturally-defined uses. Most instructions that can specify a general-purpose register can specify R0-R12.

Low registers
- Registers R0-R7 are accessible by all instructions that specify a general-purpose register.

High registers
- Registers R8-R12 are accessible by all 32-bit instructions that specify a general-purpose register.
- Registers R8-R12 are not accessible by any 16-bit instructions.

Registers R13, R14, and R15 have the following special functions:

Stack pointer
- Register R13 is used as the Stack Pointer (SP). Because the SP ignores writes to bits [1:0], it is autoaligned to a word, four-byte boundary.
- Handler mode always uses SP_main, but you can configure Thread mode to use either SP_main or SP_process.

Link register
- Register R14 is the subroutine Link Register (LR).
- The LR receives the return address from PC when a Branch and Link (BL) or Branch and Link with Exchange (BLX) instruction is executed.
- The LR is also used for exception return.
- At all other times, you can treat R14 as a general-purpose register.

Program counter
- Register R15 is the Program Counter (PC).
Bit [0] is always 0, so instructions are always aligned to word or halfword boundaries.

See the *ARMv7-M Architecture Reference Manual* for more information.
3.9 Exceptions

The processor and the Nested Vectored Interrupt Controller (NVIC) prioritize and handle all exceptions. When handling exceptions:

- All exceptions are handled in Handler mode.
- Processor state is automatically stored to the stack on an exception, and automatically restored from the stack at the end of the Interrupt Service Routine (ISR).
- The vector is fetched in parallel to the state saving, enabling efficient interrupt entry.

The processor supports tail-chaining that enables back-to-back interrupts without the overhead of state saving and restoration.

You configure the number of interrupts, and bits of interrupt priority, during implementation. Software can choose only to enable a subset of the configured number of interrupts, and can choose how many bits of the configured priorities to use.

Note

Vector table entries are compatible with interworking between ARM and Thumb instructions. This causes bit [0] of the vector value to load into the Execution Program Status Register (EPSR) T-bit on exception entry. All populated vectors in the vector table entries must have bit [0] set. Creating a table entry with bit [0] clear generates an INVSTATE fault on the first instruction of the handler corresponding to this vector.

3.9.1 Exception handling

The processor implements advanced exception and interrupt handling, as described in the ARMv7-M Architecture Reference Manual.

To reduce interrupt latency, the processor implements both interrupt late-arrival and interrupt tail-chaining mechanisms, as defined by the ARMv7-M architecture:

- There is a maximum of a twelve cycle latency from asserting the interrupt to execution of the first instruction of the ISR when the memory being accessed has no wait states being applied. The first instruction to be executed is fetched in parallel to the stack push.
- Returns from interrupts similarly take twelve cycles where the instruction being returned to is fetched in parallel to the stack pop.
- Tail chaining requires six cycles when using zero wait state memory. No stack pushes or pops are performed and only the instruction for the next ISR is fetched.

The processor exception model has the following implementation-defined behavior in addition to the architecturally defined behavior:

- exceptions on stacking from HardFault to NMI lockup at NMI priority
- exceptions on unstacking from NMI to HardFault lockup at HardFault priority.

To minimize interrupt latency, the processor abandons any divide instruction to take any pending interrupt. On return from the interrupt handler, the processor restarts the divide instruction from the beginning. The processor implements the Interruptible-continuable Instruction field. Load multiple (LDM) operations and store multiple (STM) operations are interruptible. The EPSR holds the information required to continue the load or store multiple from the point where the interrupt occurred.
This means that software must not use load-multiple or store-multiple instructions to access a device or access a memory region that is read-sensitive or sensitive to repeated writes. The software must not use these instructions in any case where repeated reads or writes might cause inconsistent results or unwanted side-effects.

**Base register update in LDM and STM operations**

There are cases when an LDM or STM updates the base register:

- When the instruction specifies base register write-back, the base register changes to the updated address. An abort restores the original base value.
- When the base register is in the register list of an LDM, and is not the last register in the list, the base register changes to the loaded value.

An LDM or STM is restarted rather than continued if:

- the instruction faults
- the instruction is inside an IT.

If an LDM has completed a base load, it is continued from before the base load.
Chapter 4
System Control

This chapter describes the registers that program the processor. It contains the following sections:

• About system control on page 4-2
• Register summary on page 4-3
• Register descriptions on page 4-5.
4.1 About system control

This chapter describes the registers that control the operation of the processor.
### 4.2 Register summary

Table 4-1 shows the system control registers. Registers not described in this chapter are described in the *ARMv7-M Architecture Reference Manual*

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000E008</td>
<td>ACTLR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>Auxiliary Control Register, ACTLR</em> on page 4-5</td>
</tr>
<tr>
<td>0xE000E010</td>
<td>STCSR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>SysTick Control and Status Register</em></td>
</tr>
<tr>
<td>0xE000E014</td>
<td>STRVR</td>
<td>RW</td>
<td>Unknown</td>
<td><em>SysTick Reload Value Register</em></td>
</tr>
<tr>
<td>0xE000E018</td>
<td>STCVR</td>
<td>RW</td>
<td>Unknown</td>
<td><em>SysTick Current Value Register</em></td>
</tr>
<tr>
<td>0xE000E01C</td>
<td>STCR</td>
<td>RO</td>
<td>Implementation specific</td>
<td><em>SysTick Calibration Value Register</em></td>
</tr>
<tr>
<td>0xE000E00</td>
<td>CPUID</td>
<td>RO</td>
<td>0x412FC231</td>
<td><em>CPUID Base Register, CPUID</em> on page 4-5</td>
</tr>
<tr>
<td>0xE000E08</td>
<td>ICSR</td>
<td>RW or RO</td>
<td>0x00000000</td>
<td><em>Interrupt Control and State Register</em></td>
</tr>
<tr>
<td>0xE000E0C</td>
<td>IARCR</td>
<td>RW</td>
<td>0x00000000a</td>
<td><em>Application Interrupt and Reset Control Register</em></td>
</tr>
<tr>
<td>0xE000E10</td>
<td>SCR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>System Control Register</em></td>
</tr>
<tr>
<td>0xE000E14</td>
<td>CCR</td>
<td>RW</td>
<td>0x00000200</td>
<td><em>Configuration and Control Register.</em></td>
</tr>
<tr>
<td>0xE000E18</td>
<td>SHPR1</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>System Handler Priority Register 1</em></td>
</tr>
<tr>
<td>0xE000E1C</td>
<td>SHPR2</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>System Handler Priority Register 2</em></td>
</tr>
<tr>
<td>0xE000E20</td>
<td>SHPR3</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>System Handler Priority Register 3</em></td>
</tr>
<tr>
<td>0xE000E24</td>
<td>SHCSR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>System Handler Control and State Register</em></td>
</tr>
<tr>
<td>0xE000E28</td>
<td>CFSR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>Configurable Fault Status Registers</em></td>
</tr>
<tr>
<td>0xE000E2C</td>
<td>HFSR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>HardFault Status Register</em></td>
</tr>
<tr>
<td>0xE000E30</td>
<td>DFSR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>Debug Fault Status Register</em></td>
</tr>
<tr>
<td>0xE000E34</td>
<td>MMFAR</td>
<td>RW</td>
<td>Unknown</td>
<td><em>MemManage Fault Address Register</em></td>
</tr>
<tr>
<td>0xE000E38</td>
<td>BFAR</td>
<td>RW</td>
<td>Unknown</td>
<td><em>BusFault Address Register</em></td>
</tr>
<tr>
<td>0xE000E3C</td>
<td>AFSR</td>
<td>RW</td>
<td>0x00000000</td>
<td><em>Auxiliary Fault Status Register, AFSR</em> on page 4-6</td>
</tr>
<tr>
<td>0xE000E40</td>
<td>ID_PFR0</td>
<td>RO</td>
<td>0x00000030</td>
<td><em>Processor Feature Register 0</em></td>
</tr>
<tr>
<td>0xE000E44</td>
<td>ID_PFR1</td>
<td>RO</td>
<td>0x00000200</td>
<td><em>Processor Feature Register 1</em></td>
</tr>
<tr>
<td>0xE000E48</td>
<td>ID_DFR0</td>
<td>RO</td>
<td>0x00100000</td>
<td><em>Debug Features Register 0</em></td>
</tr>
<tr>
<td>0xE000E4C</td>
<td>ID_AFR0</td>
<td>RO</td>
<td>0x00000000</td>
<td><em>Auxiliary Features Register 0</em></td>
</tr>
<tr>
<td>0xE000E50</td>
<td>ID_MMFR0</td>
<td>RO</td>
<td>0x00100030</td>
<td><em>Memory Model Feature Register 0</em></td>
</tr>
<tr>
<td>0xE000E54</td>
<td>ID_MMFR1</td>
<td>RO</td>
<td>0x00000000</td>
<td><em>Memory Model Feature Register 1</em></td>
</tr>
<tr>
<td>0xE000E58</td>
<td>ID_MMFR2</td>
<td>RO</td>
<td>0x01000000</td>
<td><em>Memory Model Feature Register 2</em></td>
</tr>
<tr>
<td>0xE000E5C</td>
<td>ID_MMFR3</td>
<td>RO</td>
<td>0x00000000</td>
<td><em>Memory Model Feature Register 3</em></td>
</tr>
<tr>
<td>0xE000E60</td>
<td>ID_ISAR0</td>
<td>RO</td>
<td>0x01100120</td>
<td><em>Instruction Set Attributes Register 0</em></td>
</tr>
</tbody>
</table>
### Table 4-1 System control registers (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000ED64</td>
<td>ID_ISAR1</td>
<td>RO</td>
<td>0x02111000</td>
<td>Instruction Set Attributes Register 1</td>
</tr>
<tr>
<td>0xE000ED68</td>
<td>ID_ISAR2</td>
<td>RO</td>
<td>0x21112231</td>
<td>Instruction Set Attributes Register 2</td>
</tr>
<tr>
<td>0xE000ED6C</td>
<td>ID_ISAR3</td>
<td>RO</td>
<td>0x01111110</td>
<td>Instruction Set Attributes Register 3</td>
</tr>
<tr>
<td>0xE000ED70</td>
<td>ID_ISAR4</td>
<td>RO</td>
<td>0x01310132</td>
<td>Instruction Set Attributes Register 4</td>
</tr>
<tr>
<td>0xE000ED88</td>
<td>CPACR</td>
<td>RW</td>
<td>0x00000000</td>
<td>Coprocessor Access Control Register</td>
</tr>
<tr>
<td>0xE000EF00</td>
<td>STIR</td>
<td>WO</td>
<td>0x00000000</td>
<td>Software Triggered Interrupt Register</td>
</tr>
</tbody>
</table>

a. Bits [10:8] are reset to zero. The ENDIANNESS bit, bit [15], can reset to either state, depending on the implementation.

b. BFAR and MMFAR are the same physical register. Because of this, the BFARVALID and MMFARVALID bits are mutually exclusive.

c. ID_DFR0 will read as 0 if no debug support is implemented.
4.3 Register descriptions

This section describes the system control registers whose implementation is specific to this processor.

4.3.1 Auxiliary Control Register, ACTLR

The ACTLR characteristics are:

**Purpose**
Disables certain aspects of functionality within the processor.

**Usage Constraints**
There are no usage constraints.

**Configurations**
This register is available in all processor configurations.

**Attributes**
See the register summary in Table 4-1 on page 4-3.

Figure 4-1 shows the ACTLR bit assignments.

![Figure 4-1 ACTLR bit assignments](image)

Table 4-2 shows the ACTLR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:3]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[1]</td>
<td>DISDEFWBUF</td>
<td>Disables write buffer use during default memory map accesses. This causes all bus faults to be precise, but decreases the performance of the processor because stores to memory must complete before the next instruction can be executed.</td>
</tr>
<tr>
<td>[0]</td>
<td>DISMCYCINT</td>
<td>Disables interruption of multi-cycle instructions. This increases the interrupt latency of the processor because load/store and multiply/divide operations complete before interrupt stacking occurs.</td>
</tr>
</tbody>
</table>

4.3.2 CPUID Base Register, CPUID

The CPUID characteristics are:

**Purpose**
Specifies:

- the ID number of the processor core
- the version number of the processor core
- the implementation details of the processor core.

**Usage Constraints**
There are no usage constraints.

**Configurations**
This register is available in all processor configurations.

**Attributes**
See the register summary in Table 4-1 on page 4-3.
Figure 4-2 shows the CPUID bit assignments.

<table>
<thead>
<tr>
<th>31</th>
<th>24</th>
<th>20</th>
<th>16</th>
<th>15</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMPLEMENTER</td>
<td>VARIANT</td>
<td>(Constant)</td>
<td>PARTNO</td>
<td>REVISION</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 4-2 CPUID bit assignments

Table 4-3 shows the CPUID bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>NAME</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:24] IMPLEMENTER</td>
<td>Indicates implementer: 0x41 = ARM</td>
<td></td>
</tr>
<tr>
<td>[23:20] VARIANT</td>
<td>Indicates processor revision: 0x2 = Revision 2</td>
<td></td>
</tr>
<tr>
<td>[19:16] (Constant)</td>
<td>Reads as 0xF</td>
<td></td>
</tr>
<tr>
<td>[15:4] PARTNO</td>
<td>Indicates part number: 0xC23 = Cortex-M3</td>
<td></td>
</tr>
<tr>
<td>[3:0] REVISION</td>
<td>Indicates patch release: 0x1 = Patch 1.</td>
<td></td>
</tr>
</tbody>
</table>

### 4.3.3 Auxiliary Fault Status Register, AFSR

The AFSR characteristics are:

**Purpose**
- Specifies additional system fault information to software.

**Usage Constraints**
- The AFSR flags map directly onto the AUXFAULT inputs of the processor, and a single-cycle high level on an external pin causes the corresponding AFSR bit to become latched as one. The bit can only be cleared by writing a one to the corresponding AFSR bit.
- When an AFSR bit is written or latched as one, an exception does not occur. To make use of AUXFAULT input signals, software must poll the AFSR.

**Configurations**
- This register is available in all processor configurations.

**Attributes**
- See the register summary in Table 4-1 on page 4-3.

Figure 4-3 shows the AFSR bit assignments.

<table>
<thead>
<tr>
<th>31</th>
<th>24</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUXFAULT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 4-3 AFSR bit assignments

Table 4-4 shows the AFSR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:0] AUXFAULT</td>
<td>Latched version of the AUXFAULT inputs.</td>
<td></td>
</tr>
</tbody>
</table>
Chapter 5
Memory Protection Unit

This chapter describes the processor Memory Protection Unit (MPU). It contains the following sections:

- *About the MPU* on page 5-2
- *MPU functional description* on page 5-3
- *MPU programmers model* on page 5-4.
5.1 About the MPU

The MPU is an optional component for memory protection. The processor supports the standard ARMv7 Protected Memory System Architecture model. The MPU provides full support for:

- protection regions
- overlapping protection regions, with ascending region priority:
  - 7 = highest priority
  - 0 = lowest priority.
- access permissions
- exporting memory attributes to the system.

MPU mismatches and permission violations invoke the programmable-priority MemManage fault handler. See the ARMv7-M Architecture Reference Manual for more information.

You can use the MPU to:

- enforce privilege rules
- separate processes
- enforce access rules.
5.2 MPU functional description

The attribute bits, TEX, C, B, AP, and XN, of the Region Access Control Register control access to the corresponding memory region. If an access is made to an area of memory without the required permissions, then a permission fault is raised. For more information, see the ARMv7-M Architecture Reference Manual.
5.3 MPU programmers model

Table 5-5 shows the MPU registers. These registers are described in the *ARMv7-M Architecture Reference Manual*.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000ED90</td>
<td>MPU_TYPE</td>
<td>RO</td>
<td>0x00000000a</td>
<td>MPU Type Register</td>
</tr>
<tr>
<td>0xE000ED94</td>
<td>MPU_CTRL</td>
<td>RW</td>
<td>0x00000000</td>
<td>MPU Control Register</td>
</tr>
<tr>
<td>0xE000ED98</td>
<td>MPU_RNR</td>
<td>RW</td>
<td>0x00000000</td>
<td>MPU Region Number Register</td>
</tr>
<tr>
<td>0xE000ED9C</td>
<td>MPU_RBAR</td>
<td>RW</td>
<td>0x00000000</td>
<td>MPU Region Base Address Register</td>
</tr>
<tr>
<td>0xE000EDA0</td>
<td>MPU_RASR</td>
<td>RW</td>
<td>0x00000000</td>
<td>MPU Region Attribute and Size Register</td>
</tr>
<tr>
<td>0xE000EDA4</td>
<td>MPU_RBAR_A1</td>
<td>RO</td>
<td>0x00000000</td>
<td>MPU alias registers</td>
</tr>
<tr>
<td>0xE000EDA8</td>
<td>MPU_RASR_A1</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE000EDAC</td>
<td>MPU_RBAR_A2</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE000EDB0</td>
<td>MPU_RASR_A2</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE000EDB4</td>
<td>MPU_RBAR_A3</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE000EDB8</td>
<td>MPU_RASR_A3</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
</tbody>
</table>

a. If the MPU is not present in the implementation, then this register reads as zero.
Chapter 6
Nested Vectored Interrupt Controller

This chapter describes the *Nested Vectored Interrupt Controller* (NVIC). It contains the following sections:

- *About the NVIC* on page 6-2
- *NVIC functional description* on page 6-3
- *NVIC programmers model* on page 6-4.
6.1 About the NVIC

The NVIC provides configurable interrupt handling abilities to the processor. It:

- facilitates low-latency exception and interrupt handling
- controls power management.
6.2 NVIC functional description

The NVIC supports up to 240 interrupts each with up to 256 levels of priority. You can change the priority of an interrupt dynamically. The NVIC and the processor core interface are closely coupled, to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts.

You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault.

You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS.

All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

Processor exception handling is described in *Exceptions* on page 3-20.

6.2.1 Low power modes

Your implementation can include a *Wake-up Interrupt Controller* (WIC). This enables the processor and NVIC to be put into a very low-power sleep mode leaving the WIC to identify and prioritize interrupts.

The processor fully implements the *Wait For Interrupt* (WFI), *Wait For Event* (WFE) and the *Send Event* (SEV) instructions. In addition, the processor also supports the use of SLEEPONEXIT, that causes the processor core to enter sleep mode when it returns from an exception handler to Thread mode. See the *ARMv7-M Architecture Reference Manual* for more information.

6.2.2 Level versus pulse interrupts

The processor supports both level and pulse interrupts. A level interrupt is held asserted until it is cleared by the ISR accessing the device. A pulse interrupt is a variant of an edge model. You must ensure that the pulse is sampled on the rising edge of the Cortex-M3 clock, FCLK, instead of being asynchronous.

For level interrupts, if the signal is not deasserted before the return from the interrupt routine, the interrupt again enters the pending state and re-activates. This is particularly useful for FIFO and buffer-based devices because it ensures that they drain either by a single ISR or by repeated invocations, with no extra work. This means that the device holds the signal in assert until the device is empty.

A pulse interrupt can be reasserted during the ISR so that the interrupt can be in the pending state and active at the same time. If another pulse arrives while the interrupt is still pending, the interrupt will remain pending and the ISR will run only once.

Pulse interrupts are mostly used for external signals and for rate or repeat signals.
6.3 NVIC programmers model

Table 6-1 shows the NVIC registers.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000E004</td>
<td>ICTR</td>
<td>RO</td>
<td>-</td>
<td>Interrupt Controller Type Register, ICTR</td>
</tr>
<tr>
<td>0xE000E100 - 0xE000E11C</td>
<td>NVIC_ISER0 - NVIC_ISER7</td>
<td>RW</td>
<td>0x00000000</td>
<td>Interrupt Set-Enable Registers</td>
</tr>
<tr>
<td>0xE000E180 - 0xE000E19C</td>
<td>NVIC_ICER0 - NVIC_ICER7</td>
<td>RW</td>
<td>0x00000000</td>
<td>Interrupt Clear-Enable Registers</td>
</tr>
<tr>
<td>0xE000E200 - 0xE000E21C</td>
<td>NVIC_ISPR0 - NVIC_ISPR7</td>
<td>RW</td>
<td>0x00000000</td>
<td>Interrupt Set-Pending Registers</td>
</tr>
<tr>
<td>0xE000E280 - 0xE000E29C</td>
<td>NVIC_ICPR0 - NVIC_ICPR7</td>
<td>RW</td>
<td>0x00000000</td>
<td>Interrupt Clear-Pending Registers</td>
</tr>
<tr>
<td>0xE000E300 - 0xE000E31C</td>
<td>NVIC_IABR0 - NVIC_IABR7</td>
<td>RO</td>
<td>0x00000000</td>
<td>Interrupt Active Bit Register</td>
</tr>
<tr>
<td>0xE000E400 - 0xE000E4EC</td>
<td>NVIC_IPR0 - NVIC_IPR59</td>
<td>RW</td>
<td>0x00000000</td>
<td>Interrupt Priority Register</td>
</tr>
</tbody>
</table>

The following sections describe the NVIC registers whose implementation is specific to this processor. Other registers are described in the ARMv7M Architecture Reference Manual.

6.3.1 Interrupt Controller Type Register, ICTR

The ICTR characteristics are:

**Purpose**
Shows the number of interrupt lines that the NVIC supports.

**Usage Constraints**
There are no usage constraints.

**Configurations**
This register is available in all processor configurations.

**Attributes**
See the register summary in Table 6-1.

Figure 6-1 shows the ICTR bit assignments.
Table 6-2 shows the ICTR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3:0]</td>
<td>INTLINESNUM</td>
<td>Total number of interrupt lines in groups of 32:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0000 = 0...32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0001 = 33...64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0010 = 65...96</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0011 = 97...128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0100 = 129...160</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0101 = 161...192</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0110 = 193...224</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0111 = 225...256a</td>
</tr>
</tbody>
</table>

a. The processor supports a maximum of 240 external interrupts.
Chapter 7
Debug

This chapter describes how to debug and test software running on the processor. It contains the following sections:

- About debug on page 7-2
- About the AHB-AP on page 7-6
- About the Flash Patch and Breakpoint Unit (FPB) on page 7-9.
7.1 About debug

The processor implementation determines the debug configuration, including whether debug is implemented. If the processor does not implement debug, no ROM table is present and the halt, breakpoint, and watchpoint functionality is not present.

Basic debug functionality includes processor halt, single-step, processor core register access, Vector Catch, unlimited software breakpoints, and full system memory access. See the \textit{ARMv7-M Architectural Reference Manual} for more information.

The debug option might include:

- a breakpoint unit supporting two literal comparators and six instruction comparators, or only two instruction comparators
- a watchpoint unit supporting one or four watchpoints.

For processors that implement debug, ARM recommends that a debugger identify and connect to the debug components using the CoreSight debug infrastructure.

Figure 7-1 shows the recommended flow that a debugger can follow to discover the components in the CoreSight debug infrastructure. In this case a debugger reads the peripheral and component ID registers for each CoreSight component in the CoreSight system.

```
Figure 7-1 CoreSight discovery
```

To identify the Cortex-M3 processor within the CoreSight system, ARM recommends that a debugger perform the following actions:

1. Locate and identify the Cortex-M3 ROM table using its CoreSight identification. See Table 7-1 on page 7-3 for more information.
2. Follow the pointers in that Cortex-M3 ROM table:
   a. *System Control Space* (SCS)
   b. *Breakpoint unit* (BPU)
   c. *Data watchpoint unit* (DWT).

   See Table 7-2 on page 7-4 for more information.

When a debugger identifies the SCS from its CoreSight identification, it can identify the processor and its revision number from the CPUID register in the SCS at address \(0xE000ED00\).

A debugger cannot rely on the Cortex-M3 ROM table being the first ROM table encountered. One or more system ROM tables are required between the access port and the Cortex-M3 ROM table if other CoreSight components are in the system. If a system ROM table is present, this can include a unique identifier for the implementation.

### 7.1.1 Cortex-M3 ROM table identification and entries

Table 7-1 shows the ROM table identification registers and values for debugger detection. This permits debuggers to identify the processor and its debug capabilities.

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE00FFFD0</td>
<td>Peripheral ID4</td>
<td>0x00000004</td>
<td><em>Component and Peripheral ID register formats</em> in the <em>ARMv7-M Architectural Reference Manual</em></td>
</tr>
<tr>
<td>0xE00FFFD4</td>
<td>Peripheral ID5</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFD8</td>
<td>Peripheral ID6</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFD0</td>
<td>Peripheral ID7</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFE0</td>
<td>Peripheral ID0</td>
<td>0x000000C3</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFE4</td>
<td>Peripheral ID1</td>
<td>0x00000084</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFE8</td>
<td>Peripheral ID2</td>
<td>0x00000084</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFE0</td>
<td>Component ID0</td>
<td>0x0000000D</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFF4</td>
<td>Component ID1</td>
<td>0x00000010</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFF8</td>
<td>Component ID2</td>
<td>0x00000005</td>
<td></td>
</tr>
<tr>
<td>0xE00FFFC</td>
<td>Component ID3</td>
<td>0x000000B1</td>
<td></td>
</tr>
</tbody>
</table>

These are the default values for the Peripheral ID registers if the ROM table has not been configured at implementation. Your implementation might use these registers to identify the manufacturer and part number for the device.

The Component ID registers identify this as a CoreSight ROM table.

--- **Note** ---

The Cortex-M3 ROM table only supports word size transactions.
Table 7-2 shows the CoreSight components that the Cortex-M3 ROM table points to. The values depend on the implemented debug configuration.

<table>
<thead>
<tr>
<th>Address</th>
<th>Component</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE00FF000</td>
<td>SCS</td>
<td>0xFFF0F003</td>
<td>See System Control Space</td>
</tr>
<tr>
<td>0xE00FF004</td>
<td>DWT</td>
<td>0xFFF02003^a</td>
<td>See Table 8-1 on page 8-4</td>
</tr>
<tr>
<td>0xE00FF008</td>
<td>FPB</td>
<td>0xFFF03003^b</td>
<td>See Table 7-7 on page 7-10</td>
</tr>
<tr>
<td>0xE00FF00C</td>
<td>ITM</td>
<td>0xFFF01003^c</td>
<td>See Table 9-1 on page 9-4</td>
</tr>
<tr>
<td>0xE00FF010</td>
<td>TPIU</td>
<td>0xFFF41003^d</td>
<td>See Table 11-1 on page 11-5.</td>
</tr>
<tr>
<td>0xE00FF014</td>
<td>ETM</td>
<td>0xFFF42003^e</td>
<td>See Chapter 10 Embedded Trace Macrocell.</td>
</tr>
<tr>
<td>0xE00FF018</td>
<td>End marker</td>
<td>0x00000000</td>
<td>See DAP accessible ROM table in the ARMv7-M Architectural Reference Manual.</td>
</tr>
<tr>
<td>0xE00FFFC</td>
<td>SYSTEM ACCESS</td>
<td>0x00000001</td>
<td></td>
</tr>
</tbody>
</table>

The ROM table entries point to the debug components of the processor. The offset for each entry is the offset of that component from the ROM table base address, 0xE00FF000.

See the ARMv7-M Architectural Reference Manual and the ARM CoreSight Components Technical Reference Manual for more information about the ROM table ID and component registers, and their addresses and access types.

### 7.1.2 System Control Space

If debug is implemented, the processor provides debug through registers in the SCS. See:

- *Debug register summary* on page 7-5
- *System address map* on page 3-11.
**SCS CoreSight identification**

Table 7-3 shows the SCS CoreSight identification registers and values for debugger detection. Final debugger identification of the Cortex-M3 processor is through the CPUID register in the SCS. See *CPUID Base Register, CPUID* on page 4-5.

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000EFD0</td>
<td>Peripheral ID4</td>
<td>0x00000004</td>
<td>Component and Peripheral ID register formats in the <em>ARMv7-M Architectural Reference Manual</em>.</td>
</tr>
<tr>
<td>0xE000EFE0</td>
<td>Peripheral ID0</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE000EFE4</td>
<td>Peripheral ID1</td>
<td>0x00000080</td>
<td></td>
</tr>
<tr>
<td>0xE000EFE8</td>
<td>Peripheral ID2</td>
<td>0x00000088</td>
<td></td>
</tr>
<tr>
<td>0xE000EFE0C</td>
<td>Peripheral ID3</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE000EFF0</td>
<td>Component ID0</td>
<td>0x0000000D</td>
<td></td>
</tr>
<tr>
<td>0xE000EFF4</td>
<td>Component ID1</td>
<td>0x000000EF</td>
<td></td>
</tr>
<tr>
<td>0xE000EFF8</td>
<td>Component ID2</td>
<td>0x00000005</td>
<td></td>
</tr>
<tr>
<td>0xE000EFFC</td>
<td>Component ID3</td>
<td>0x00000081</td>
<td></td>
</tr>
</tbody>
</table>

See the *ARMv7-M Architectural Reference Manual* and the *ARM CoreSight Components Technical Reference Manual* for more information about the SCS CoreSight identification registers, and their addresses and access types.

### 7.1.3 Debug register summary

Table 7-4 shows the debug registers. Each of these registers is 32 bits wide and is described in the *ARMv7-M Architectural Reference Manual*.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000ED30</td>
<td>DFSR</td>
<td>RW</td>
<td>0x000000000a</td>
<td>Debug Fault Status Register</td>
</tr>
<tr>
<td>0xE000ED50</td>
<td>DHCSR</td>
<td>RW</td>
<td>0x0000000000</td>
<td>Debug Halting Control and Status Register</td>
</tr>
<tr>
<td>0xE000EDF4</td>
<td>DCRSR</td>
<td>WO</td>
<td></td>
<td>Debug Core Register Selector Register</td>
</tr>
<tr>
<td>0xE000EDF8</td>
<td>DCRDR</td>
<td>RW</td>
<td></td>
<td>Debug Core Register Data Register</td>
</tr>
<tr>
<td>0xE000EDFC</td>
<td>DEMCR</td>
<td>RW</td>
<td>0x0000000000</td>
<td>Debug Exception and Monitor Control Register</td>
</tr>
</tbody>
</table>

a. Power-on reset only

Core debug is an optional component. If core debug is removed then halt mode debugging is not supported, and there is no halt, stepping, or register transfer functionality. Debug monitor mode is still supported.
7.2 About the AHB-AP

The AHB-AP is a Memory Access Port (MEM-AP) as defined in the ARM Debug Interface v5 Architecture Specification. The AHB-AP is an optional debug access port into the Cortex-M3 system, and provides access to all memory and registers in the system, including processor registers through the SCS. System access is independent of the processor status. Either SW-DP or SWJ-DP is used to access the AHB-AP.

The AHB-AP is a master into the Bus Matrix. Transactions are made using the AHB-AP programmers model, which generates AHB-Lite transactions into the Bus Matrix.

7.2.1 AHB-AP transaction types

The AHB-AP does not perform back-to-back transactions on the bus, and so all transactions are non-sequential. The AHB-AP can perform unaligned and bit-band transactions. The Bus Matrix handles these. The AHB-AP transactions are not subject to MPU lookups. AHB-AP transactions bypass the FPB, and so the FPB cannot remap AHB-AP transactions.

AHB-AP transactions are little-endian.

7.2.2 AHB-AP programmers model

Table 7-5 shows the AHB-AP registers. If the AHB-AP is not present, these registers read as zero. Any register that is not specified in this table reads as zero.

<table>
<thead>
<tr>
<th>Offseta</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>CSW</td>
<td>RW</td>
<td>See register</td>
<td><em>AHB-AP Control and Status Word Register, CSW</em></td>
</tr>
<tr>
<td>0x04</td>
<td>TAR</td>
<td>RW</td>
<td>-</td>
<td>AHB-AP Transfer Address Register</td>
</tr>
<tr>
<td>0x0C</td>
<td>DRW</td>
<td>RW</td>
<td>-</td>
<td>AHB-AP Data Read/Write Register</td>
</tr>
<tr>
<td>0x10</td>
<td>BD0</td>
<td>RW</td>
<td>-</td>
<td>AHB-AP Banked Data Register0</td>
</tr>
<tr>
<td>0x14</td>
<td>BD1</td>
<td>RW</td>
<td>-</td>
<td>AHB-AP Banked Data Register1</td>
</tr>
<tr>
<td>0x18</td>
<td>BD2</td>
<td>RW</td>
<td>-</td>
<td>AHB-AP Banked Data Register2</td>
</tr>
<tr>
<td>0x1C</td>
<td>BD3</td>
<td>RW</td>
<td>-</td>
<td>AHB-AP Banked Data Register3</td>
</tr>
<tr>
<td>0xF8</td>
<td>DBGDRAR</td>
<td>RO</td>
<td>0xEEEFF03</td>
<td>AHB-AP ROM Address Register</td>
</tr>
<tr>
<td>0xFC</td>
<td>IDR</td>
<td>RO</td>
<td>0x24770011</td>
<td>AHB-AP Identification Register</td>
</tr>
</tbody>
</table>

- The offset given in this table is relative to the location of the AHB-AP in the DAP memory space. This space is only visible from the access port. It is not part of the processor memory map.

The following sections describe the AHB-AP registers whose implementation is specific to this processor. Other registers are described in the CoreSight Components Technical Reference Manual.

**AHB-AP Control and Status Word Register, CSW**

The CSW characteristics are:

**Purpose** Configures and controls transfers through the AHB interface.

**Usage constraints** There are no usage constraints.
Configurations  This register is available in all processor configurations.

Attributes  See the register summary in Table 7-5 on page 7-6.

Figure 7-2 shows the CSW bit assignments.

Table 7-6 shows the CSW bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:30]</td>
<td>-</td>
<td>Reserved. Read as 0b00.</td>
</tr>
<tr>
<td>[29]</td>
<td>MasterTypea</td>
<td>0 = core. 1 = debug. This bit must not be changed if a transaction is outstanding. A debugger must first check bit [7], TransInProg. Reset value = 0b1. An implementation can configure this bit to be read only with a value of 1. In that case, transactions are always indicated as debug.</td>
</tr>
<tr>
<td>[28:26]</td>
<td>-</td>
<td>Reserved, 0b00.</td>
</tr>
<tr>
<td>[23:12]</td>
<td>-</td>
<td>Reserved, 0x000.</td>
</tr>
<tr>
<td>[11:8]</td>
<td>Mode</td>
<td>Mode of operation bits: 0b0000 = normal download and upload mode 0b0001-0b1111 are reserved. Reset value = 0b0000.</td>
</tr>
<tr>
<td>[7]</td>
<td>TransInProg</td>
<td>Transfer in progress. This field indicates if a transfer is in progress on the APB master port.</td>
</tr>
<tr>
<td>[6]</td>
<td>DbgStatus</td>
<td>Indicates the status of the DAPEN port. 1 = AHB transfers permitted. 0 = AHB transfers not permitted.</td>
</tr>
</tbody>
</table>
Table 7-6 CSW bit assignments (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5:4]</td>
<td>AddrInc</td>
<td>Auto address increment and pack mode on Read or Write data access. Only increments if the current transaction completes with no error. Auto address incrementing and packed transfers are not performed on access to Banked Data registers 0x10 - 0x1C. The status of these bits is ignored in these cases. Increments and wraps within a 4-KB address boundary, for example from 0x1000 to 0x1FFC. If the start is at 0x14A0, then the counter increment to 0x1FFC, wraps to 0x1000, then continues incrementing to 0x149C. 0b00 = auto increment off. 0b01 = increment single. Single transfer from corresponding byte lane. 0b10 = increment packed.b 0b11 = reserved. No transfer. Size of address increment is defined by the Size field [2:0]. Reset value: 0b00.</td>
</tr>
<tr>
<td>[2:0]</td>
<td>Size</td>
<td>Size of access field: 0b000 = 8 bits 0b001 = 16 bits 0b010 = 32 bits 0b011-111 are reserved. Reset value: 0b000.</td>
</tr>
</tbody>
</table>

a. When clear, this bit prevents the debugger from setting the C_DEBUGEN bit in the Debug Halting Control and Status Register, and so prevents the debugger from being able to halt the processor.
b. See the definition of packed transfers in the *ARM Debug Interface v5 Architecture Specification*. 

7.3 About the Flash Patch and Breakpoint Unit (FPB)

The FPB:
• implements hardware breakpoints
• patches code and data from Code space to System space.

A full FPB unit contains:
• Two literal comparators for matching against literal loads from Code space, and
remapping to a corresponding area in System space.
• Six instruction comparators for matching against instruction fetches from Code space, and
remapping to a corresponding area in System space. Alternatively, you can configure the
comparators individually to return a Breakpoint Instruction (BKPT) to the processor core
on a match, to provide hardware breakpoint capability.

A reduced FPB unit contains:
• Two instruction comparators. You can configure each comparator individually to return a
Breakpoint Instruction to the processor on a match, to provide hardware breakpoint
capability.

7.3.1 FPB functional description

The FPB contains both a global enable and individual enables for the eight comparators. If the
comparison for an entry matches, the address is either:
• remapped to the address set in the remap register plus an offset corresponding to the
comparator that matched
• remapped to a BKPT instruction if that feature is enabled.

The comparison happens dynamically, but the result of the comparison occurs too late to stop
the original instruction fetch or literal load taking place from the Code space. The processor
ignores this transaction however, and only the remapped transaction is used.

If an MPU is present, the MPU lookups are performed for the original address, not the remapped
address.

You can remove the FPB if no debug is required, or you can reduce the number of breakpoints
it supports to two. If the FPB supports only two breakpoints then only comparators 0 and 1 are
used, and the FPB does not support flash patching.

__________ Note ___________
• Unaligned literal accesses are not remapped. The original access to the DCode bus takes
place in this case.
• Load exclusive accesses can be remapped. However, it is Unpredictable whether they are
performed as exclusive accesses or not.
• Setting the flash patch remap location to a bit-band alias is not supported and results in
Unpredictable behavior.
7.3.2 FPB programmers model

Table 7-7 shows the FPB registers. Depending on the implementation of your processor, some of these registers might not be present. Any register that is configured as not present reads as zero.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0002000</td>
<td>FP_CTRL</td>
<td>RW</td>
<td>0x260</td>
<td>FlashPatch Control Register</td>
</tr>
<tr>
<td>0xE0002004</td>
<td>FP_REMAP</td>
<td>RW</td>
<td></td>
<td>FlashPatch Remap Register</td>
</tr>
<tr>
<td>0xE0002008</td>
<td>FP_COMP0</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register0</td>
</tr>
<tr>
<td>0xE000200C</td>
<td>FP_COMP1</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register1</td>
</tr>
<tr>
<td>0xE0002010</td>
<td>FP_COMP2</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register2</td>
</tr>
<tr>
<td>0xE0002014</td>
<td>FP_COMP3</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register3</td>
</tr>
<tr>
<td>0xE0002018</td>
<td>FP_COMP4</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register4</td>
</tr>
<tr>
<td>0xE000201C</td>
<td>FP_COMP5</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register5</td>
</tr>
<tr>
<td>0xE0002020</td>
<td>FP_COMP6</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register6</td>
</tr>
<tr>
<td>0xE0002024</td>
<td>FP_COMP7</td>
<td>RW</td>
<td>0b0</td>
<td>FlashPatch Comparator Register7</td>
</tr>
<tr>
<td>0xE0002FD0</td>
<td>PID4</td>
<td>RO</td>
<td>0x04</td>
<td>Peripheral identification registers</td>
</tr>
<tr>
<td>0xE0002FD4</td>
<td>PID5</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0002FD8</td>
<td>PID6</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0002FDC</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0002FE0</td>
<td>PID0</td>
<td>RO</td>
<td>0x03</td>
<td></td>
</tr>
<tr>
<td>0xE0002FE4</td>
<td>PID1</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0002FE8</td>
<td>PID2</td>
<td>RO</td>
<td>0x2B</td>
<td></td>
</tr>
<tr>
<td>0xE0002FEC</td>
<td>PID3</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0002FF0</td>
<td>CID0</td>
<td>RO</td>
<td>0x00</td>
<td>Component identification registers</td>
</tr>
<tr>
<td>0xE0002FF4</td>
<td>CID1</td>
<td>RO</td>
<td>0xE0</td>
<td></td>
</tr>
<tr>
<td>0xE0002FF8</td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td></td>
</tr>
<tr>
<td>0xE0002FFC</td>
<td>CID3</td>
<td>RO</td>
<td>0xB1</td>
<td></td>
</tr>
</tbody>
</table>

Table 7-7 FPB register summary

a. For FP_COMP0 to FP_COMP7, bit 0 is reset to 0. Other bits in these registers are not reset.

All FPB registers are described in the *ARMv7-M Architecture Reference Manual*. 
Chapter 8
Data Watchpoint and Trace Unit

This chapter describes the Data Watchpoint and Trace (DWT) unit. It contains the following sections:

• About the DWT on page 8-2
• DWT functional description on page 8-3
• DWT Programmers Model on page 8-4.
8.1 About the DWT

The DWT is an optional debug unit that provides watchpoints, data tracing, and system profiling for the processor.
8.2 DWT functional description

A full DWT contains four comparators that you can configure as
• a hardware watchpoint
• an ETM trigger
• a PC sampler event trigger
• a data address sampler event trigger.

The first comparator, DWT_COMP0, can also compare against the clock cycle counter, CYCCNT. You can also use the second comparator, DWT_COMP1, as a data comparator.

A reduced DWT contains one comparator that you can use as a watchpoint or as a trigger. It does not support data matching.

The DWT if present contains counters for:
• clock cycles (CYCCNT)
• folded instructions
• Load Store Unit (LSU) operations
• sleep cycles
• CPI, that is all instruction cycles except for the first cycle
• interrupt overhead.

Note
An event is generated each time a counter overflows.

You can configure the DWT to generate PC samples at defined intervals, and to generate interrupt event information.

The DWT provides periodic requests for protocol synchronization to the ITM and the TPIU, if the your implementation includes the Cortex-M3 TPIU.
8.3 DWT Programmers Model

Table 8-1 lists the DWT registers. Depending on the implementation of your processor, some of these registers might not be present. Any register that is configured as not present reads as zero.

### Table 8-1 DWT register summary

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0001000</td>
<td>DWT_CTRL</td>
<td>RW</td>
<td>See a</td>
<td>Control Register</td>
</tr>
<tr>
<td>0xE0001004</td>
<td>DWT_CYCCNT</td>
<td>RW</td>
<td>0x00000000</td>
<td>Cycle Count Register</td>
</tr>
<tr>
<td>0xE0001008</td>
<td>DWT_CPICNT</td>
<td>RW</td>
<td>-</td>
<td>CPI Count Register</td>
</tr>
<tr>
<td>0xE000100C</td>
<td>DWT_EXCCNT</td>
<td>RW</td>
<td>-</td>
<td>Exception Overhead Count Register</td>
</tr>
<tr>
<td>0xE0001010</td>
<td>DWT_SLEEPCNT</td>
<td>RW</td>
<td>-</td>
<td>Sleep Count Register</td>
</tr>
<tr>
<td>0xE0001014</td>
<td>DWT_LSUCNT</td>
<td>RW</td>
<td>-</td>
<td>LSU Count Register</td>
</tr>
<tr>
<td>0xE0001018</td>
<td>DWT_FOLDCNT</td>
<td>RW</td>
<td>-</td>
<td>Folded-instruction Count Register</td>
</tr>
<tr>
<td>0xE000101C</td>
<td>DWT_PCSR</td>
<td>RO</td>
<td>-</td>
<td>Program Counter Sample Register</td>
</tr>
<tr>
<td>0xE0001020</td>
<td>DWT_COMP0</td>
<td>RW</td>
<td>-</td>
<td>Comparator Register0</td>
</tr>
<tr>
<td>0xE0001024</td>
<td>DWT_MASK0</td>
<td>RW</td>
<td>-</td>
<td>Mask Register0</td>
</tr>
<tr>
<td>0xE0001028</td>
<td>DWT_FUNCTION0</td>
<td>RW</td>
<td>0x00000000</td>
<td>Function Register0</td>
</tr>
<tr>
<td>0xE0001030</td>
<td>DWT_COMP1</td>
<td>RW</td>
<td>-</td>
<td>Comparator Register1</td>
</tr>
<tr>
<td>0xE0001034</td>
<td>DWT_MASK1</td>
<td>RW</td>
<td>-</td>
<td>Mask Register1</td>
</tr>
<tr>
<td>0xE0001038</td>
<td>DWT_FUNCTION1</td>
<td>RW</td>
<td>0x00000000</td>
<td>Function Register1</td>
</tr>
<tr>
<td>0xE0001040</td>
<td>DWT_COMP2</td>
<td>RW</td>
<td>-</td>
<td>Comparator Register2</td>
</tr>
<tr>
<td>0xE0001044</td>
<td>DWT_MASK2</td>
<td>RW</td>
<td>-</td>
<td>Mask Register2</td>
</tr>
<tr>
<td>0xE0001048</td>
<td>DWT_FUNCTION2</td>
<td>RW</td>
<td>0x00000000</td>
<td>Function Register2</td>
</tr>
<tr>
<td>0xE0001050</td>
<td>DWT_COMP3</td>
<td>RW</td>
<td>-</td>
<td>Comparator Register3</td>
</tr>
<tr>
<td>0xE0001054</td>
<td>DWT_MASK3</td>
<td>RW</td>
<td>-</td>
<td>Mask Register3</td>
</tr>
<tr>
<td>0xE0001058</td>
<td>DWT_FUNCTION3</td>
<td>RW</td>
<td>0x00000000</td>
<td>Function Register3</td>
</tr>
<tr>
<td>0xE0001FD0</td>
<td>PID4</td>
<td>RO</td>
<td>0x04</td>
<td>Peripheral identification registers</td>
</tr>
<tr>
<td>0xE001FD4</td>
<td>PID5</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE001FD8</td>
<td>PID6</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE001FDC</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE001FE0</td>
<td>PID0</td>
<td>RO</td>
<td>0x02</td>
<td></td>
</tr>
<tr>
<td>0xE001FE4</td>
<td>PID1</td>
<td>RO</td>
<td>0x80</td>
<td></td>
</tr>
<tr>
<td>0xE001FE8</td>
<td>PID2</td>
<td>RO</td>
<td>0x38</td>
<td></td>
</tr>
<tr>
<td>0xE001FEC</td>
<td>PID3</td>
<td>RO</td>
<td>0x80</td>
<td></td>
</tr>
</tbody>
</table>

**Note**
- Cycle matching functionality is only available in comparator 0.
- Data matching functionality is only available in comparator 1.
- Data value is only sampled for accesses that do not produce an MPU or bus fault. The PC is sampled irrespective of any faults. The PC is only sampled for the first address of a burst.
- The FUNCTION field in the DWT_FUNCTION1 register is overridden for comparators given by DATAVADDR0 and DATAVADDR1 if DATAVMATCH is also set in DWT_FUNCTION1. The comparators given by DATAVADDR0 and DATAVADDR1 can then only perform address comparator matches for comparator 1 data matches.
- If the data matching functionality is not included during implementation it is not possible to set DATAVADDR0, DATAVADDR1, or DATAVMATCH in DWT_FUNCTION1. This means that the data matching functionality is not available in the implementation. Test the availability of data matching by writing and reading the DATAVMATCH bit in DWT_FUNCTION1. If this bit cannot be set then data matching is unavailable.
- PC match is not recommended for watchpoints because it stops after the instruction. It mainly guards and triggers the ETM.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0001FF0</td>
<td>CID0</td>
<td>RO</td>
<td>0x00</td>
<td>Component identification registers</td>
</tr>
<tr>
<td>0xE0001FF4</td>
<td>CID1</td>
<td>RO</td>
<td>0xE0</td>
<td></td>
</tr>
<tr>
<td>0xE0001FF8</td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td></td>
</tr>
<tr>
<td>0xE0001FFC</td>
<td>CID3</td>
<td>RO</td>
<td>0x81</td>
<td></td>
</tr>
</tbody>
</table>

a. Possible reset values are:
- 0x40000000 if four comparators for watchpoints and triggers are present
- 0x4F000000 if four comparators for watchpoints only are present
- 0x10000000 if only one comparator is present
- 0x1F000000 if one comparator for watchpoints and not triggers is present
- 0x00000000 if DWT is not present.
Chapter 9
Instrumentation Trace Macrocell Unit

This chapter describes the Instrumentation Trace Macrocell (ITM) unit. It contains the following sections:

- About the ITM on page 9-2
- ITM functional description on page 9-3
- ITM programmers model on page 9-4.
9.1 About the ITM

The ITM is an optional application-driven trace source that supports printf() style debugging to trace operating system and application events, and generates diagnostic system information.
9.2 ITM functional description

The ITM generates trace information as packets. Multiple sources can generate packets. If multiple sources generate packets at the same time, the ITM arbitrates the order in which packets are output. These sources in decreasing order of priority are:

- Software trace. Software can write directly to ITM stimulus registers to generate packets.
- Hardware trace. The DWT generates these packets, and the ITM outputs them.
- Time stamping. Timestamps are generated relative to packets. The ITM contains a 21-bit counter to generate the timestamp. The Cortex-M3 clock or the bitclock rate of the Serial Wire Viewer (SWV) output clocks the counter.
9.3 ITM programmers model

Table 9-1 shows the ITM registers. Depending on the implementation of your processor, the ITM registers might not be present. Any register that is configured as not present reads as zero.

--- Note ---

- You must enable TRCENA of the Debug Exception and Monitor Control Register before you program or use the ITM.
- If the ITM stream requires synchronization packets, you must configure the synchronization packet rate in the DWT.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0000000-0xE000007C</td>
<td>ITM_STIM0-ITM_STIM31</td>
<td>RW</td>
<td>-</td>
<td>Stimulus Port Registers 0-31</td>
</tr>
<tr>
<td>0xE0000E00</td>
<td>ITM_TER</td>
<td>RW</td>
<td>0x00000000</td>
<td>Trace Enable Register</td>
</tr>
<tr>
<td>0xE0000E40</td>
<td>ITM_TPR</td>
<td>RW</td>
<td>0x00000000</td>
<td>ITM Trace Privilege Register. ITM_TPR on page 9-5</td>
</tr>
<tr>
<td>0xE0000E80</td>
<td>ITM_TCR</td>
<td>RW</td>
<td>0x00000000</td>
<td>Trace Control Register</td>
</tr>
<tr>
<td>0xE0000FD0</td>
<td>PID4</td>
<td>RO</td>
<td>0x00000004</td>
<td>Peripheral Identification registers</td>
</tr>
<tr>
<td>0xE0000FD4</td>
<td>PID5</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE0000FD8</td>
<td>PID6</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE0000FDC</td>
<td>PID7</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE0000FE0</td>
<td>PID0</td>
<td>RO</td>
<td>0x00000001</td>
<td></td>
</tr>
<tr>
<td>0xE0000FE4</td>
<td>PID1</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE0000FE8</td>
<td>PID2</td>
<td>RO</td>
<td>0x0000003B</td>
<td></td>
</tr>
<tr>
<td>0xE0000FEC</td>
<td>PID3</td>
<td>RO</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>0xE0000FF0</td>
<td>CID0</td>
<td>RO</td>
<td>0x0000000D</td>
<td>Component Identification registers</td>
</tr>
<tr>
<td>0xE0000FF4</td>
<td>CID1</td>
<td>RO</td>
<td>0x000000E0</td>
<td></td>
</tr>
<tr>
<td>0xE0000FF8</td>
<td>CID2</td>
<td>RO</td>
<td>0x00000005</td>
<td></td>
</tr>
<tr>
<td>0xE0000FFC</td>
<td>CID3</td>
<td>RO</td>
<td>0x000000B1</td>
<td></td>
</tr>
</tbody>
</table>

--- Note ---

ITM registers are fully accessible in privileged mode. In user mode, all registers can be read, but only the Stimulus Registers and Trace Enable Registers can be written, and only when the corresponding Trace Privilege Register bit is set. Invalid user mode writes to the ITM registers are discarded.

The following sections describes the ITM registers whose implementation is specific to this processor. Other registers are described in the ARMv7-M Architectural Reference Manual.
9.3.1 ITM Trace Privilege Register, ITM_TPR

The ITM_TPR characteristics are:

**Purpose**
Enables an operating system to control the stimulus ports that are accessible by user code.

**Usage constraints**
You can only write to this register in privileged mode.

**Configurations**
This register is available if the ITM is configured in your implementation.

**Attributes**
See Table 9-1 on page 9-4.

Figure 9-1 shows the ITM_TPR bit assignments.

![Figure 9-1 ITM_TPR bit assignments](image)

Table 9-2 shows the ITM_TPR bit assignments.

### Table 9-2 ITM_TPR bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
</table>
| [3:0] | PRIVMASK | Bit mask to enable tracing on ITM stimulus ports:  
|       |          | bit [0] = stimulus ports [7:0]  
Chapter 10
Embedded Trace Macrocell

This chapter describes the *Embedded Trace Macrocell* (ETM). It contains the following sections:

- *About the ETM* on page 10-2
- *ETM functional description* on page 10-3
- *ETM Programmers model* on page 10-9
10.1 About the ETM

The ETM is an optional debug component that enables reconstruction of program execution. The ETM is designed to be a high-speed, low-power debug tool that only supports instruction trace. This ensures that area is minimized, and that gate count is reduced.

The ETM implements ARM ETM architecture v3.5. See the *ARM Embedded Trace Macrocell Architecture Specification*.

The ETM traces all 32-bit Thumb instructions as a single instruction. The ETM traces instructions following an IT instruction as normal conditional instructions. The decompressor does not need to refer to the IT instruction.

You can use the CoreSight ETM-M3 either with the Cortex-M3 *Trace Port Interface Unit* (M3-TPIU), or as part of a CoreSight system.

10.1.1 Features

ETM-M3 provides:

- tracing of 16-bit and 32-bit Thumb instructions
- four EmbeddedICE watchpoint inputs
- a Trace Start/Stop block with EmbeddedICE inputs
- two external inputs
- a 24-byte FIFO queue
- global timestamping.

See the *Embedded Trace Macrocell Architecture Specification* for information about:

- the trace protocol
- controlling tracing using triggering and filtering resources.

See the *Cortex-M3 Integration and Implementation Manual* for information about the macrocell signals.

10.1.2 Configurable options

The ETM-M3 macrocell includes the following configuration inputs:

- the maximum number of external inputs, see *External inputs* on page 10-6
- whether the system supports the FIFOFULL mechanism for stalling the processor, see Table 10-1 on page 10-4.
10.2 ETM functional description

Figure 10-1 shows a block diagram of the ETM, and shows how the ETM interfaces to the Trace Port Interface Unit (TPIU).

The Cortex-M3 system can perform low-bandwidth data tracing using the Data Watchpoint and Trace (DWT) and Instruction Trace Macrocell (ITM) components.

The ETM trace output is compatible with the AMBA Trace Bus (ATB) protocol, irrespective of the configuration of the trace port size and trace port mode within the ETM programmers model. The TPIU exports trace information from the processor. An implementation can replace the TPIU with other CoreSight trace components.

For more information see:
- Chapter 8 Data Watchpoint and Trace Unit
- Chapter 9 Instrumentation Trace Macrocell Unit
- Chapter 11 Trace Port Interface Unit
- Embedded Trace Macrocell Architecture Specification.

The ETM provides a trace ID register for systems that use multiple trace sources. You must configure this register even if only a single trace source is in use.

The following sections provide information on features of the ETM:
- Resources
- Periodic synchronization on page 10-6
- Data and instruction address compare resources on page 10-6
- External inputs on page 10-6
- Start/stop block on page 10-6
- Triggering on page 10-7
- Interfaces on page 10-7
- Operation on page 10-8.

10.2.1 Resources

Because the ETM does not generate data trace information, the lower bandwidth reduces the requirement for complex triggering capabilities. This means that the ETM only includes a small sub-set of the possible resources allowed by the ETM architecture.
Table 10-1 lists the Cortex-M3 resources.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Present on ETM-M3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture version</td>
<td>ETMv3.5</td>
</tr>
<tr>
<td>Address comparator pairs</td>
<td>0</td>
</tr>
<tr>
<td>Data comparators</td>
<td>0</td>
</tr>
<tr>
<td>Context ID comparators</td>
<td>0</td>
</tr>
<tr>
<td>Memory Map Decoders (MMDs)</td>
<td>0</td>
</tr>
<tr>
<td>Counters</td>
<td>1, reduced function counter only</td>
</tr>
<tr>
<td>Sequencer</td>
<td>No</td>
</tr>
<tr>
<td>Start/stop block</td>
<td>Yes</td>
</tr>
<tr>
<td>Embedded ICE comparators</td>
<td>4</td>
</tr>
<tr>
<td>External inputs</td>
<td>2</td>
</tr>
<tr>
<td>External outputs</td>
<td>0</td>
</tr>
<tr>
<td>Extended external inputs</td>
<td>0</td>
</tr>
<tr>
<td>Extended external input selectors</td>
<td>0</td>
</tr>
<tr>
<td>FIFOFULL</td>
<td>Yes</td>
</tr>
<tr>
<td>FIFOFULL level setting</td>
<td>Yes</td>
</tr>
<tr>
<td>Branch broadcasting</td>
<td>Yes</td>
</tr>
<tr>
<td>ASIC Control Register</td>
<td>No</td>
</tr>
<tr>
<td>Data suppression</td>
<td>No</td>
</tr>
<tr>
<td>Software access to registers</td>
<td>Yes</td>
</tr>
<tr>
<td>Readable registers</td>
<td>Yes</td>
</tr>
<tr>
<td>FIFO size</td>
<td>24 bytes</td>
</tr>
<tr>
<td>Minimum port size</td>
<td>8 bits</td>
</tr>
<tr>
<td>Maximum port size</td>
<td>8 bits</td>
</tr>
<tr>
<td>Normal port mode</td>
<td>-</td>
</tr>
<tr>
<td>Normal half-rate clocking, 1:1</td>
<td>Yes - asynchronous</td>
</tr>
<tr>
<td>Demux port mode</td>
<td>-</td>
</tr>
<tr>
<td>Demux half-rate clocking, 1:2</td>
<td>No</td>
</tr>
<tr>
<td>Mux port mode, 2:1</td>
<td>No</td>
</tr>
<tr>
<td>1:4 port mode</td>
<td>No</td>
</tr>
<tr>
<td>Dynamic port mode, including stalling</td>
<td>No. Supported by asynchronous port mode.</td>
</tr>
<tr>
<td>Coprocessor Register Transfer (CPRT) data</td>
<td>No</td>
</tr>
</tbody>
</table>
Resource identification encoding

You configure the trace enable event and trigger event using the same mechanism. For each event, a 17-bit register is used to define the event. This register provides:
- Resource A, bits [6:0]
- a Boolean function, bits [16:14].

Table 10-2 shows the encodings used for the Boolean function.

Table 10-2 Boolean function encoding for events

<table>
<thead>
<tr>
<th>Encoding</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>A</td>
</tr>
<tr>
<td>0b001</td>
<td>NOT(A)</td>
</tr>
<tr>
<td>0b010</td>
<td>A AND B</td>
</tr>
<tr>
<td>0b011</td>
<td>NOT(A) AND B</td>
</tr>
<tr>
<td>0b100</td>
<td>NOT(A) AND NOT (B)</td>
</tr>
<tr>
<td>0b101</td>
<td>A OR B</td>
</tr>
<tr>
<td>0b110</td>
<td>NOT (A) OR B</td>
</tr>
<tr>
<td>0b111</td>
<td>NOT (A) OR NOT (B)</td>
</tr>
</tbody>
</table>

Table 10-3 shows the encodings used for Resource identification.

Table 10-3 Resource identification encoding

<table>
<thead>
<tr>
<th>Resource type</th>
<th>Index range</th>
<th>Description of resource type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b010</td>
<td>0-3</td>
<td>DWT Comparator inputs (0-3)</td>
</tr>
<tr>
<td>0b100</td>
<td>0</td>
<td>Counter 1 at zero</td>
</tr>
<tr>
<td>0b101</td>
<td>15</td>
<td>Trace Start/Stop resource</td>
</tr>
<tr>
<td>0b110</td>
<td>0-1</td>
<td>ExtIn (0-1)</td>
</tr>
<tr>
<td>0b111</td>
<td>15</td>
<td>HardWired (always True)</td>
</tr>
</tbody>
</table>

10.2.2 Timestamp format

Timestamps are encoded as 48-bit natural binary numbers. A system implementation may provide a timestamp count which can be used by several trace sources as an aid to correlating the trace streams.

10.2.3 Periodic synchronization

The ETM uses a fixed synchronization packet generation frequency of every 1024 bytes of trace.

10.2.4 Data and instruction address compare resources

The DWT provides four address comparators on the data bus that provide debug functionality. Within the DWT unit, you can specify the functions triggered by a match, and one of these functions is to generate an ETM match input. These inputs are presented to the ETM as Embedded In Circuit Emulator (ICE) comparator inputs.

A single DWT resource can trigger an ETM event and also generate instrumentation trace directly from the same event.

You can configure the four DWT comparators individually to compare with the address of the current executing instruction to permit the ETM access to an instruction address compare resource. These inputs are presented to the ETM as Embedded ICE comparator inputs. The DWT provides either one or four comparators, depending on the implementation of the processor.

______ Note ______

Using a DWT comparator as an instruction address comparator reduces the number of available data address comparisons.

See Chapter 8 Data Watchpoint and Trace Unit for more information about the DWT unit.

10.2.5 External inputs

Two external inputs, ETMEXTIN[1:0], enable additional components to generate trigger and enable signals for the ETM.

10.2.6 Start/stop block

The start/stop block provides a single-bit resource that can be used as an input to other parts of the resource logic, including the trace enable logic. The start/stop block can only be controlled by using the EmbeddedICE inputs to the ETM. The DWT controls these inputs.

The start/stop block is set to the start state if any of the EmbeddedICE watchpoint inputs selected as start resources in ETMTESSEICR go HIGH. The start/stop block is set to the stop state if any of the EmbeddedICE watchpoint inputs selected as stop resources in ETMTESSEICR go LOW.

If bit [25] of ETMTECR1 is 1, tracing will only be enabled when the start/stop block is in the start state.

Tracing is also only enabled when the result of evaluating the Trace Enable Event is TRUE. This event can be set to always be TRUE by programming a value of 0x6F to ETMTEEVR. For more information see the Embedded Trace Macrocell Architecture Specification.
10.2.7 Triggering

The ETM provides a trigger resource that can be used to identify a point within a trace run. The generation of a trigger does not affect the tracing in any way, but the trigger will be output in the trace stream, and can also be passed to other trace components or used to halt the processor. An external trace port analyzer can use the trigger to determine when to start and stop capture of trace.

10.2.8 Interfaces

The ETM-M3 has the following external interfaces:

- **ATB**
  - A 32-bit Advanced Trace Bus provides trace output from the macrocell. See the AMBA 3 ATB Protocol Specification for more information about this interface.

- **APB**
  - An Advanced Peripheral Bus provides the control interface for the macrocell. See the AMBA 3 APB Protocol Specification for more information about this interface.

- **CTI**
  - Your implementation can provide a Cross Trigger Interface to manage the interconnection of trigger and control signals between the processor core, ETM, and TPIU. The implementation of your Cortex-M3 processor determines which ETM functions are visible to the CTI.

**Recommended CTI connections**

Table 10-4 and Table 10-5 on page 10-8 show the recommended CTI connections for Cortex-M3 systems.

--- Note ---

These tables show the ARM standard connections, but the actual connections are implementation-defined. Check the documentation from the supplier of your device for any changes to these connections.

<table>
<thead>
<tr>
<th>Trigger bit</th>
<th>Source signal</th>
<th>Source device</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>ETMTRIGOUT</td>
<td>ETM</td>
<td>Recommended if ETM is present.</td>
</tr>
<tr>
<td>[3]</td>
<td>ACQCOMP</td>
<td>ETB</td>
<td>Recommended if an Embedded Trace Buffer (ETB) is present. If multiple cores share a single ETB, you must only connect to the CTI of one of the cores.</td>
</tr>
<tr>
<td>[2]</td>
<td>FULL</td>
<td>ETB</td>
<td></td>
</tr>
<tr>
<td>[1]</td>
<td>User Defined</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>[0]</td>
<td>HALTED</td>
<td>Core</td>
<td>Compulsory.</td>
</tr>
</tbody>
</table>
### Table 10-5 Trigger output connections

<table>
<thead>
<tr>
<th>Trigger bit</th>
<th>Destination signal</th>
<th>Destination device</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>User defined</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[6]</td>
<td>User defined</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[4]</td>
<td>ETMEXTIN[0]</td>
<td>ETM</td>
<td>Compulsory if ETM is present.</td>
</tr>
<tr>
<td>[3]</td>
<td>INTISR[y]</td>
<td>NVIC</td>
<td>Recommended if an ETB is present. If multiple cores share a single ETB, you must only connect to the CTI of one of the cores.</td>
</tr>
<tr>
<td>[2]</td>
<td>INTISR[x]</td>
<td>NVIC</td>
<td>Compulsory. Any interrupt can be used.</td>
</tr>
<tr>
<td>[1]</td>
<td>User defined</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[0]</td>
<td>EDBGREQ</td>
<td>Core</td>
<td>Compulsory.</td>
</tr>
</tbody>
</table>

### 10.2.9 Operation

ETM-M3 implements version 3.5 of the ARM Embedded Trace Macrocell protocol.
10.3 ETM Programmers model

This section describes the mechanisms for programming the registers used to set up the trace and triggering facilities of the macrocell. The programmers model enables you to use the ETM registers to control the macrocell.

10.3.1 Modes of operation and execution

ETM-M3 implements ETMv3.5 for tracing 16-bit and 32-bit Thumb instructions. The Embedded Trace Macrocell Architecture Specification describes the features of ETMv3.5.

See Features on page 10-2 for information on the trace features of the ETM-M3.

When the ETM is powered up or reset, you must program all of the registers that do not have an architected reset state before you enable tracing. If you do not do so, the trace results are Unpredictable.

When programming the ETM registers you must enable all the changes at the same time. To achieve this, the Programming bit in ETMCR should be used. See Main Control Register, ETMCR on page 10-11.

When the Programming bit is set to 0 you must not write to registers other than ETMCR, because this can lead to Unpredictable behavior.

When setting the Programming bit, you must not change any other bits of ETMCR. You must only change the value of bits other than the Programming bit of ETMCR when bit [1] of ETMSR is set to 1. ARM recommends that you use a read-modify-write procedure when changing ETMCR.

10.3.2 Register summary

Table 10-6 shows the ETM registers.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Reset</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0041000</td>
<td>ETMCR</td>
<td>0x00000411</td>
<td>RW</td>
<td>Main Control Register, ETMCR on page 10-11</td>
</tr>
<tr>
<td>0xE0041004</td>
<td>ETMCCR</td>
<td>0x8C802000</td>
<td>RO</td>
<td>Configuration Code Register, ETMCCR on page 10-14</td>
</tr>
<tr>
<td>0xE0041008</td>
<td>EMTTRIGGER</td>
<td></td>
<td>RW</td>
<td>Trigger Event Register. See ARM Embedded Trace Macrocell Architecture Specification</td>
</tr>
<tr>
<td>0xE0041010</td>
<td>ETMSR</td>
<td></td>
<td>RW</td>
<td>ERM Status Register. See ARM Embedded Trace Macrocell Architecture Specification</td>
</tr>
<tr>
<td>0xE0041014</td>
<td>ETMSCR</td>
<td>0x00020009</td>
<td>RO</td>
<td>System Configuration Register, ETMSCR on page 10-15</td>
</tr>
<tr>
<td>0xE0041020</td>
<td>EMTTEEVPR</td>
<td></td>
<td>RW</td>
<td>TraceEnable Event Register. See ARM Embedded Trace Macrocell Architecture Specification</td>
</tr>
<tr>
<td>0xE0041024</td>
<td>EMTTECRI</td>
<td></td>
<td>RW</td>
<td>TraceEnable Control 1 Register, ETMTECRI on page 10-16</td>
</tr>
<tr>
<td>0xE0041028</td>
<td>ETMFFLR</td>
<td></td>
<td>RW</td>
<td>FIFOFULL Level Register. See ARM Embedded Trace Macrocell Architecture Specification</td>
</tr>
<tr>
<td>0xE0041140</td>
<td>ETMCNTRLDVR1</td>
<td></td>
<td>RW</td>
<td>Free-running counter reload value</td>
</tr>
<tr>
<td>0xE00411E0</td>
<td>ETMSYNCFR</td>
<td>0x00000400</td>
<td>RO</td>
<td>Synchronisation Frequency Register. See ARM Embedded Trace Macrocell Architecture Specification</td>
</tr>
<tr>
<td>Address</td>
<td>Name</td>
<td>Reset</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------</td>
<td>-----------</td>
<td>-------</td>
<td>------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0xE00411E4</td>
<td>ETMIDR</td>
<td>0x4114F253</td>
<td>RO</td>
<td>ID Register, ETMIDR on page 10-17</td>
</tr>
<tr>
<td>0xE00411E8</td>
<td>ETMCCER</td>
<td>0x18541800</td>
<td>RO</td>
<td>Configuration Code Extension Register, ETMCCER on page 10-18</td>
</tr>
<tr>
<td>0xE0041F0</td>
<td>ETMTESSEICR</td>
<td>-</td>
<td>RW</td>
<td>TraceEnable Start/Stop EmbeddedICE Control Register, ETMTESSEICR on page 10-19</td>
</tr>
<tr>
<td>0xE0041F8</td>
<td>ETMTSEVR</td>
<td>-</td>
<td>RW</td>
<td>Timestamp Event Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE004200</td>
<td>ETMTRACEIDR</td>
<td>0x00000000</td>
<td>RW</td>
<td>CoreSight Trace ID Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE004208</td>
<td>ETMIDR2</td>
<td>0x00000000</td>
<td>RO</td>
<td>ETM ID Register 2. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041314</td>
<td>ETMPDSR</td>
<td>0x00000001</td>
<td>RO</td>
<td>Device Power-Down Status Register, ETMPDSR on page 10-19</td>
</tr>
<tr>
<td>0xE0041EE0</td>
<td>ITMISCIN</td>
<td>-</td>
<td>RO</td>
<td>Integration Test Miscellaneous Inputs, ITMISCIN on page 10-20</td>
</tr>
<tr>
<td>0xE0041EE8</td>
<td>ITTRIGOUT</td>
<td>-</td>
<td>WO</td>
<td>Integration Test Trigger Out, ITTRIGOUT on page 10-21</td>
</tr>
<tr>
<td>0xE0041F0</td>
<td>ETM_ITATBCTR2</td>
<td>-</td>
<td>RO</td>
<td>ETM Integration Test ATB Control 2, ETM_ITATBCTR2 on page 10-21</td>
</tr>
<tr>
<td>0xE0041F8</td>
<td>ETM_ITATBCTR0</td>
<td>-</td>
<td>WO</td>
<td>ETM Integration Test ATB Control 0, ETM_ITATBCTR0 on page 10-22</td>
</tr>
<tr>
<td>0xE0041F00</td>
<td>ETMITCTRL</td>
<td>0x00000000</td>
<td>RW</td>
<td>Integration Mode Control Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041FA0</td>
<td>ETMCLAIMSET</td>
<td>-</td>
<td>RW</td>
<td>Claim Tag Set Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041FA4</td>
<td>ETMCLAIMCLR</td>
<td>-</td>
<td>RW</td>
<td>Claim Tag Clear Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041FB0</td>
<td>ETMLAR</td>
<td>-</td>
<td>RW</td>
<td>Lock Access Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041FB4</td>
<td>ETMLSR</td>
<td>-</td>
<td>RO</td>
<td>Lock Status Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041FB8</td>
<td>ETMAUTHSTATUS</td>
<td>-</td>
<td>RO</td>
<td>Authentication Status Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
<tr>
<td>0xE0041FC0</td>
<td>ETMDEVTYPE</td>
<td>0x00000013</td>
<td>RO</td>
<td>CoreSight Device Type Register. See ARM Embedded Trace Macrocell Architecture Specfication</td>
</tr>
</tbody>
</table>
10.3.3 Main Control Register, ETMCR

The ETMCR characteristics are:

**Purpose**
Controls general operation of the ETM, such as whether tracing is enabled.

**Usage constraints**
There are no usage constraints.

**Configurations**
This register is only available if the processor is configured to use the ETM.

**Attributes**
See the ETM register summary in Table 10-6 on page 10-9.

Figure 10-2 shows the ETMCR bit assignments.

Table 10-7 on page 10-12 shows the ETMCR bit assignments.
Table 10-7 ETMCR bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:22]</td>
<td>RAZ</td>
<td></td>
</tr>
<tr>
<td>[28]</td>
<td>Timestamp enable</td>
<td>When set, this bit enables timestamping. An ETM reset sets this bit to 0.</td>
</tr>
<tr>
<td>[21]</td>
<td>Port size[3]</td>
<td>This bit is implemented but has no function. An ETM reset sets this bit to 0.</td>
</tr>
<tr>
<td>[20:18]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>[17:16]</td>
<td>Port mode [1:0]</td>
<td>These bits are implemented but have no function. An ETM reset sets these bits to 0.</td>
</tr>
<tr>
<td>[15:14]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>[13]</td>
<td>Port mode[2]</td>
<td>This bit is implemented but has no function. An ETM reset sets this bit to 0.</td>
</tr>
<tr>
<td>[12]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>[11]</td>
<td>ETM port selection</td>
<td>This bit can be used to control other trace components in an implementation. The possible values are: 0 ETMEN is LOW. 1 ETMEN is HIGH. This bit must be set by the trace software tools to ensure that trace output is enabled from this ETM. An ETM reset sets this bit to 0.</td>
</tr>
<tr>
<td>[10]</td>
<td>ETM programming</td>
<td>This bit must be set to 1 at the start of the ETM programming sequence. Tracing is prevented while this bit is set to 1. On an ETM reset this bit is set to 0b1.</td>
</tr>
<tr>
<td>[9]</td>
<td>Debug request control</td>
<td>When set to 1 and the trigger event occurs, the DBGRQ output is asserted until DBGACK is observed. This enables the ARM processor to be forced into Debug state. An ETM reset sets this bit to 0.</td>
</tr>
<tr>
<td>[8]</td>
<td>Branch output</td>
<td>When set to 1 all branch addresses are output, even if the branch was because of a direct branch instruction. Setting this bit enables reconstruction of the program flow without having access to the memory image of the code being executed. When this bit is set to 1, more trace data is generated, and this may affect the performance of the trace system. Information about the execution of a branch is traced regardless of the state of this bit. An ETM reset sets this bit to 0.</td>
</tr>
<tr>
<td>[7]</td>
<td>Stall processor</td>
<td>The FIFOFULL output can be used to stall the processor to prevent overflow. The FIFOFULL output is only enabled when the stall processor bit is set to 1. When the bit is 0 the FIFOFULL output remains LOW at all times and the FIFO overflows if there are too many trace packets. Trace resumes without corruption once the FIFO has drained, if overflow does occur. An ETM reset sets this bit to 0. For information about the interaction of this bit with the ETMFFLR register see the Embedded Trace Macrocell Architecture Specification.</td>
</tr>
</tbody>
</table>
Port size [2:0] The ETM-M3 has no influence over the external pins used for trace. These bits are implemented but not used.
On an ETM reset these bits reset to 0b001.

[3:1] - Reserved

[0] ETM power down
This bit can be used by an implementation to control if the ETM is in a low power state. This bit must be cleared by the trace software tools at the beginning of a debug session.
When this bit is set to 1, writes to some registers and fields might be ignored. You can always write to the following registers and fields:
• ETMCR bit [0]
• ETMLAR
• ETMCLAIMSET register
• ETMCLAIMCLR register.
When the ETMCR is written with this bit set to 1, bits other than bit [0] might be ignored.
On an ETM reset this bit is set to 1.
10.3.4 Configuration Code Register, ETMCCR

The ETM Configuration Code Register characteristics are:

**Purpose**
Enables software to read the implementation-specific configuration of the ETM.

**Usage constraints**
There are no usage constraints.

**Configurations**
This register is only available if the processor is configured to use the ETM.

**Attributes**
See the ETM register summary in Table 10-6 on page 10-9.

Figure 10-3 shows the ETMCCR bit assignments.

![Figure 10-3 ETMCCR bit assignments](image)

Table 10-8 shows the ETMCCR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>ETM ID register present</td>
<td>The value of this bit is 1, indicating that the ETMIDR, register 0x79, is present and defines the ETM architecture version in use.</td>
</tr>
<tr>
<td>[27]</td>
<td>Coprocessor and memory access</td>
<td>The value of this bit is 1, indicating that memory-mapped access to registers is supported.</td>
</tr>
<tr>
<td>[26]</td>
<td>Trace start/stop block present</td>
<td>The value of this bit is 1, indicating that the Trace start/stop block is present.</td>
</tr>
<tr>
<td>[25:24]</td>
<td>Number of Context ID comparators</td>
<td>The value of these bits is 0b00, indicating that Context ID comparators are not implemented.</td>
</tr>
<tr>
<td>[23]</td>
<td><strong>FIFOFULL</strong> logic present</td>
<td>The value of this bit is 1, indicating that <strong>FIFOFULL</strong> logic is present in the ETM. To use FIFOFULL the system must also support the function, as indicated by bit [8] of ETMSCR, see <strong>System Configuration Register, ETMSCR</strong> on page 10-15.</td>
</tr>
<tr>
<td>[22:20]</td>
<td>Number of external outputs</td>
<td>The value of these bits is 0b00, indicating that no external outputs are supported.</td>
</tr>
<tr>
<td>[19:17]</td>
<td>Number of external inputs</td>
<td>The value of these bits is between 0b00 and 0b10, indicating the number of external inputs, from 0 to 2, implemented in the system.</td>
</tr>
<tr>
<td>[16]</td>
<td>Sequencer present</td>
<td>The value of this bit is 0, indicating that the sequencer is not implemented.</td>
</tr>
</tbody>
</table>
10.3.5 System Configuration Register, ETMSCR

The ETMSCR characteristics are:

**Purpose**
Shows the ETM features supported by the implementation of the ETM macrocell.

**Usage constraints**
There are no usage constraints.

**Configurations**
This register is only available if the processor is configured to use the ETM.

**Attributes**
See the register summary in Table 10-6 on page 10-9.

Figure 10-4 shows the ETMSCR bit assignments.

![Figure 10-4 ETMSCR bit assignments](image)

Table 10-9 shows the ETMSCR bit assignments.

---

### Table 10-8 ETMCCR bit assignments (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:13]</td>
<td>Number of counters</td>
<td>The value of these bits is 0b001, indicating that one counter is implemented.</td>
</tr>
<tr>
<td>[12:8]</td>
<td>Number of memory map decoders</td>
<td>The value of these bits is 0b00000, indicating that memory map decoder inputs are not implemented.</td>
</tr>
<tr>
<td>[7:4]</td>
<td>Number of data value comparators</td>
<td>The value of these bits is 0b0000, indicating that data value comparators are not implemented.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>Number of address comparator pairs</td>
<td>The value of these bits is 0b0000, indicating that address comparator pairs are not implemented.</td>
</tr>
</tbody>
</table>

---

### Table 10-9 ETMSCR bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:18]</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>[17]</td>
<td>No Fetch comparisons</td>
<td>The value of this bit is 1, indicating that fetch comparisons are not implemented.</td>
</tr>
<tr>
<td>[14:12]</td>
<td>(N-1)</td>
<td>These bits give the number of supported processors minus 1. The value of these bits is 0b000, indicating that there is only one processor connected.</td>
</tr>
<tr>
<td>[11]</td>
<td>Port mode supported</td>
<td>This bit reads as 1 if the currently selected port mode is supported. This has no effect on the TPIU trace port.</td>
</tr>
</tbody>
</table>
10.3.6 TraceEnable Control 1 Register, ETMTECR1

The ETMTECR1 characteristics are:

- **Purpose**: Enables the start/stop logic used for trace enable.
- **Usage constraints**: There are no usage constraints.
- **Configurations**: This register is only available if the processor is configured to use the ETM.
- **Attributes**: See the register summary in Table 10-6 on page 10-9.

Figure 10-5 shows the ETMTECR1 bit assignments.

![Figure 10-5 ETMTECR1 bit assignments](image)

Table 10-10 shows the ETMTECR1 bit assignments.
10.3.7 ID Register, ETMIDR

The ETMIDR characteristics are:

**Purpose**

Holds the ETM architecture variant, and defines the programmers model for the ETM.

**Usage constraints**

There are no usage constraints.

**Configurations**

This register is only available if the processor is configured to use the ETM.

**Attributes**

See the register summary in Table 10-6 on page 10-9.

Figure 10-6 shows the ETMIDR bit assignments.

![Figure 10-6 ETMIDR bit assignments](image)

Table 10-11 shows the ETMIDR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:24]</td>
<td>Implementer code</td>
<td>These bits identify ARM as the implementer of the processor. The value of these bits is 0b01000001.</td>
</tr>
<tr>
<td>[20]</td>
<td>Branch packet encoding</td>
<td>The value of this bit is 1, indicating that alternative branch packet encoding is implemented.</td>
</tr>
<tr>
<td>[19]</td>
<td>Security Extensions support</td>
<td>The value of this bit is 0, indicating that the ETM behaves as if the processor is in Secure state at all times.</td>
</tr>
<tr>
<td>[18]</td>
<td>32-bit Thumb instruction tracing</td>
<td>The value of this bit is 1, indicating that a 32-bit Thumb instruction is traced as a single instruction.</td>
</tr>
<tr>
<td>[17]</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[16]</td>
<td>Load PC first</td>
<td>The value of this bit is 0, indicating that data tracing is not supported.</td>
</tr>
<tr>
<td>[15:12]</td>
<td>Processor family</td>
<td>The value of these bits is 0b1111, indicating that the processor family is not identified in this register.</td>
</tr>
<tr>
<td>[11:8]</td>
<td>Major ETM architecture version</td>
<td>The value of these bits is 0b0010, indicating major architecture version number 3, ETMv3.</td>
</tr>
<tr>
<td>[7:4]</td>
<td>Minor ETM architecture version</td>
<td>The value of these bits is 0b0101, indicating minor architecture version number 5.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>Implementation revision</td>
<td>The value of these bits is 0b0011, indicating implementation revision, 3.</td>
</tr>
</tbody>
</table>
10.3.8 Configuration Code Extension Register, ETMCCER

The ETMCCER characteristics are:

**Purpose**
Holds ETM configuration information additional to that in the ETMCCR. See *Configuration Code Register, ETMCCR* on page 10-14.

**Usage constraints**
There are no usage constraints.

**Configurations**
This register is only available if the processor is configured to use the ETM.

**Attributes**
See the register summary in Table 10-6 on page 10-9.

Figure 10-7 shows the ETMCCER bit assignments.

![Figure 10-7 ETMCCER bit assignments](image)

Table 10-12 shows the ETMCCER bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[29]</td>
<td>Timestamp size</td>
<td>Set to 0 to indicate a size of 48 bits.</td>
</tr>
<tr>
<td>[28]</td>
<td>Timestamp encoding</td>
<td>Set to 1 to indicate that the timestamp is encoded as a natural binary number.</td>
</tr>
<tr>
<td>[27]</td>
<td>Reduced function counter</td>
<td>Set to 1 to indicate that Counter 1 is a reduced function counter.</td>
</tr>
<tr>
<td>[22]</td>
<td>Timestamping implemented</td>
<td>This bit is set to 1, indicating that timestamping is implemented.</td>
</tr>
<tr>
<td>[21]</td>
<td>EmbeddedICE behavior control implemented</td>
<td>The value of this bit is 0, indicating that the ETMEIBCR is not implemented. For more information on EmbeddedICE behavior see the <em>Embedded Trace Macrocell Architecture Specification</em>.</td>
</tr>
<tr>
<td>[20]</td>
<td>Trace Start/Stop block uses EmbeddedICE watchpoint inputs</td>
<td>The value of this bit is 1, indicating that the Trace Start/Stop block uses the EmbeddedICE watchpoint inputs.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>EmbeddedICE watchpoint inputs</td>
<td>The value of these bits is 0b0100, indicating that the number of EmbeddedICE watchpoint inputs implemented is four. These inputs come from the DWT.</td>
</tr>
<tr>
<td>[15:13]</td>
<td>Instrumentation resources</td>
<td>The value of these bits is 0b0000, indicating that no Instrumentation resources are supported.</td>
</tr>
</tbody>
</table>
10.3.9 TraceEnable Start/Stop EmbeddedICE Control Register, ETMTESSEICR

The ETMTESSEICR characteristics are:

**Purpose**
Specifies the EmbeddedICE watchpoint comparator inputs that are used to control the start/stop resource.

**Usage constraints**
There are no usage constraints.

**Configurations**
This register is only available if the processor is configured to use the ETM.

**Attributes**
See the register summary in Table 10-6 on page 10-9.

Figure 10-8 shows the ETMTESSEICR bit assignments.

Table 10-12 ETMCCER bit assignments (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>Data address comparisons</td>
<td>The value of this bit is 1, indicating that data address comparisons are not supported.</td>
</tr>
<tr>
<td>[11]</td>
<td>Readable registers</td>
<td>The value of this bit is 1, indicating that all registers are readable.</td>
</tr>
<tr>
<td>[10:3]</td>
<td>Extended external input bus</td>
<td>The value of these bits is 0, indicating that the extended external input bus is not implemented.</td>
</tr>
<tr>
<td>[2:0]</td>
<td>Extended external input selectors</td>
<td>The value of these bits is 0, indicating that extended external input selectors are not implemented.</td>
</tr>
</tbody>
</table>

![Figure 10-8 ETMTESSEICR bit assignments](image)

Table 10-13 shows the ETMTESSEICR bit assignments.

Table 10-13 ETMTESSEICR bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
</table>

10.3.10 Device Power-Down Status Register, ETMPDSR

The ETMPDSR characteristics are:

**Purpose**
Indicates the power-down status of the ETM.
Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use an ETM.

Attributes See the register summary in Table 10-6 on page 10-9.

Figure 10-9 shows the ETMPDSR bit assignments.

![Figure 10-9 ETMPDSR bit assignments](image)

Table 10-14 shows the ETMPDSR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[0]</td>
<td>ETM powered up</td>
<td>The value of this bit indicates whether you can access the ETM Trace Registers. The value of this bit is always 1, indicating that the ETM Trace Registers can be accessed.</td>
</tr>
</tbody>
</table>

10.3.11 Integration Test Miscellaneous Inputs, ITMISCIN

The ITMISCIN characteristics are:

Purpose Integration test.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 10-6 on page 10-9.

Figure 10-10 shows the ITMISCIN bit assignments.

![Figure 10-10 ITMISCIN bit assignments](image)
Table 10-15 shows the ITMISCIN bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:5]</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[4]</td>
<td>COREHALT</td>
<td>A read of this bit returns the value of the COREHALT input pin.</td>
</tr>
<tr>
<td>[1:0]</td>
<td>EXTIN[1:0]</td>
<td>A read of these bits returns the value of the EXTIN[1:0] input pins.</td>
</tr>
</tbody>
</table>

10.3.12 Integration Test Trigger Out, ITTRIGOUT

The ITMISCIN characteristics are:

**Purpose**  Integration test.

**Usage constraints**  You must set bit [0] of ETMITCTRL to use this register.

**Configurations**  This register is only available if the processor is configured to use the ETM.

**Attributes**  See the register summary in Table 10-6 on page 10-9.

Figure 10-11 shows the ITTRIGOUT bit assignments.

![Figure 10-11 ITTRIGOUT bit assignments](image)

Table 10-16 shows the ITTRIGOUT bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:1]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[0]</td>
<td>TRIGGER output value</td>
<td>A write to this bit sets the TRIGGER output.</td>
</tr>
</tbody>
</table>

10.3.13 ETM Integration Test ATB Control 2, ETM_ITATBCTR2

The ETM_ITATBCTR2 characteristics are:

**Purpose**  Integration test.

**Usage constraints**  You must set bit [0] of ETMITCTRL to use this register.

**Configurations**  This register is only available if the processor is configured to use the ETM.

**Attributes**  See the register summary in Table 10-6 on page 10-9.

Figure 10-12 on page 10-22 shows the ETM_ITATBCTR2 bit assignments.
10.3.14 ETM Integration Test ATB Control 0, ETM_ITATBCTR0

The Integration Test ATB Control (ETM_ITATBCTR0) characteristics are:

**Purpose** Integration test.

**Usage constraints** You must set bit [0] of ETMITCTRL to use this register.

**Configurations** This register is only available if the processor is configured to use the ETM.

**Attributes** See the register summary in Table 10-6 on page 10-9.

Figure 10-13 shows the ETM_ITATBCTR0 bit assignments.

### Table 10-17 ETM_ITATBCTR2 bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:1]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[0]</td>
<td>ATREADY input value</td>
<td>A read of this bit returns the value of the ETM ATREADY input.</td>
</tr>
</tbody>
</table>

### Table 10-18 ETM_ITATBCTR0 bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:1]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[0]</td>
<td>ATVALID output value</td>
<td>A write to this bit sets the value of the ETM ATVALID output.</td>
</tr>
</tbody>
</table>
Chapter 11
Trace Port Interface Unit

This chapter describes the Cortex-M3 TPIU, the Trace Port Interface Unit specific to the Cortex-M3 processor. It contains the following sections:

- About the Cortex-M3 TPIU on page 11-2
- TPIU functional description on page 11-3
- TPIU programmers model on page 11-5.
11.1 About the Cortex-M3 TPIU

The Cortex-M3 TPIU is an optional component that acts as a bridge between the on-chip trace data from the Embedded Trace Macrocell (ETM) and the Instrumentation Trace Macrocell (ITM), with separate IDs, to a data stream. The TPIU encapsulates IDs where required, and the data stream is then captured by a Trace Port Analyzer (TPA).

The Cortex-M3 TPIU is specially designed for low-cost debug. It is a special version of the CoreSight TPIU. Your implementation can replace the Cortex-M3 TPIU with other CoreSight components if your implementation requires the additional features of the CoreSight TPIU.

In this chapter, the term TPIU refers to the Cortex-M3 TPIU. For information about the CoreSight TPIU, see the ARM CoreSight Components Technical Reference Manual.
11.2 TPIU functional description

There are two configurations of the TPIU:
• A configuration that supports ITM debug trace.
• A configuration that supports both ITM and ETM debug trace.

If your implementation requires no trace support then the TPIU might not be present.

Note
If your Cortex-M3 system uses the optional ETM component, the TPIU configuration supports both ITM and ETM debug trace. See Chapter 10 Embedded Trace Macrocell.

11.2.1 TPIU block diagrams

Figure 11-1 shows the component layout of the TPIU for both configurations.

![TPIU block diagram](image_url)

**Figure 11-1 TPIU block diagram**

11.2.2 TPIU Formatter

The formatter inserts source ID signals into the data packet stream so that trace data can be re-associated with its trace source. The formatter is always active when the Trace Port Mode is active.

The formatting protocol is described in the CoreSight Architecture Specification. You must enable synchronization packets in the DWT to provide synchronization for the formatter.

When the formatter is enabled, half-sync packets may be inserted if there is no data to output after a frame has been started. Synchronization, caused by the distributed synchronization from the DWT, will ensure that any partial frame is completed, and at least one full synchronization packet will be generated.
11.2.3 Serial Wire Output format

The TPIU can output trace data in a *Serial Wire Output* (SWO) format:

- TPIU_DEVID specifies the formats that are supported. See TPIU_DEVID on page 11-12.
- TPIU_SPPR specifies the SWO format in use. See the *ARMv7-M Architecture Reference Manual*.

When one of the two SWO modes is selected, you can enable the TPIU to bypass the formatter for trace output. If the formatter is bypassed, only the ITM and DWT trace source passes through. The TPIU accepts and discards data from the ETM. This function can be used to connect a device containing an ETM to a trace capture device that is only able to capture SWO data.
11.3 TPIU programmers model

Table 11-1 provides a summary of the TPIU registers. Depending on the implementation of your processor, the TPIU registers might not be present, or the CoreSight TPIU might be present instead. Any register that is configured as not present reads as zero.

Table 11-1 TPIU registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0040000</td>
<td>TPIU_SSPSR</td>
<td>RO</td>
<td>0x0xx</td>
<td>Supported Parallel Port Size Register</td>
</tr>
<tr>
<td>0xE0040004</td>
<td>TPIU_CPSR</td>
<td>RW</td>
<td>0x01</td>
<td>Current Parallel Port Size Register</td>
</tr>
<tr>
<td>0xE0040010</td>
<td>TPIU_ACPR</td>
<td>RW</td>
<td>0x0000</td>
<td>Asynchronous Clock Prescaler Register, TPIU_ACPR on page 11-6</td>
</tr>
<tr>
<td>0xE00400F0</td>
<td>TPIU_SPPR</td>
<td>RW</td>
<td>0x01</td>
<td>Selected Pin Protocol Register</td>
</tr>
<tr>
<td>0xE0040300</td>
<td>TPIU_FFSR</td>
<td>RO</td>
<td>0x08</td>
<td>Formatter and Flush Status Register, TPIU_FFSR on page 11-6</td>
</tr>
<tr>
<td>0xE0040304</td>
<td>TPIU_FFCR</td>
<td>RW</td>
<td>0x102</td>
<td>Formatter and Flush Control Register, TPIU_FFCR on page 11-7</td>
</tr>
<tr>
<td>0xE0040308</td>
<td>TPIU_FSCR</td>
<td>RO</td>
<td>0x00</td>
<td>Formatter Synchronization Counter Register</td>
</tr>
<tr>
<td>0xE0040EE8</td>
<td>TRIGGER</td>
<td>RO</td>
<td>0x0</td>
<td>TRIGGER on page 11-8</td>
</tr>
<tr>
<td>0xE0040EEC</td>
<td>FIFO data 0</td>
<td>RO</td>
<td>0x---000000</td>
<td>Integration ETM Data on page 11-8</td>
</tr>
<tr>
<td>0xE0040EF0</td>
<td>ITATBCTR2</td>
<td>RO</td>
<td>0x0</td>
<td>ITATBCTR2 on page 11-9</td>
</tr>
<tr>
<td>0xE0040EFC</td>
<td>FIFO data 1</td>
<td>RO</td>
<td>0x---000000</td>
<td>Integration ITM Data on page 11-10</td>
</tr>
<tr>
<td>0xE0040F08</td>
<td>ITATBCTR0</td>
<td>RO</td>
<td>0x0</td>
<td>ITATBCTR0 on page 11-11</td>
</tr>
<tr>
<td>0xE0040F00</td>
<td>ITCTRL</td>
<td>RW</td>
<td>0x0</td>
<td>Integration Mode Control, TPIU_ITCTRL on page 11-11</td>
</tr>
<tr>
<td>0xE0040FA0</td>
<td>CLAIMSET</td>
<td>RW</td>
<td>0xF</td>
<td>Claim tag set</td>
</tr>
<tr>
<td>0xE0040FA4</td>
<td>CLAIMCLR</td>
<td>RW</td>
<td>0x0</td>
<td>Claim tag clear</td>
</tr>
<tr>
<td>0xE0040F08</td>
<td>DEVID</td>
<td>RO</td>
<td>0xCA0/0xCA1</td>
<td>TPIU_DEVID on page 11-12</td>
</tr>
<tr>
<td>0xE0040FE0</td>
<td>DEVTYPE</td>
<td>RO</td>
<td>0x11</td>
<td>TPIU_DEVTYPE on page 11-13</td>
</tr>
<tr>
<td>0xE0040FD0</td>
<td>PID4</td>
<td>RO</td>
<td>0x04</td>
<td>Peripheral identification registers</td>
</tr>
<tr>
<td>0xE0040FD4</td>
<td>PID5</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0040FD8</td>
<td>PID6</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0040FDC</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0040FE0</td>
<td>PID0</td>
<td>RO</td>
<td>0x23</td>
<td></td>
</tr>
<tr>
<td>0xE0040FE4</td>
<td>PID1</td>
<td>RO</td>
<td>0x09</td>
<td></td>
</tr>
<tr>
<td>0xE0040FE8</td>
<td>PID2</td>
<td>RO</td>
<td>0x38</td>
<td></td>
</tr>
<tr>
<td>0xE0040FEC</td>
<td>PID3</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0040FF0</td>
<td>CID0</td>
<td>RO</td>
<td>0x0D</td>
<td>Component identification registers</td>
</tr>
<tr>
<td>0xE0040FF4</td>
<td>CID1</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0xE0040FF8</td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td></td>
</tr>
<tr>
<td>0xE0040FFC</td>
<td>CID3</td>
<td>RO</td>
<td>0x81</td>
<td></td>
</tr>
</tbody>
</table>
The following sections describe the TPIU registers whose implementation is specific to this processor. The Formatter, Integration Mode Control, and Claim Tag registers are described in the CoreSight Components Technical Reference Manual. Other registers are described in the ARMv7-M Architecture Reference Manual.

11.3.1 Asynchronous Clock Prescaler Register, TPIU_ACPR

The TPIU_ACPR characteristics are:

- **Purpose**: Scales the baud rate of the asynchronous output.
- **Usage constraints**: There are no usage constraints.
- **Configurations**: This register is available in all processor configurations.
- **Attributes**: See Table 11-1 on page 11-5.

Figure 11-2 shows the TPIU_ACPR bit assignments.

![Figure 11-2 TPIU_ACPR bit assignments](image)

Table 11-2 shows the TPIU_ACPR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:13]</td>
<td>-</td>
<td>Reserved. RAZ/SBZP.</td>
</tr>
<tr>
<td>[12:0]</td>
<td>PRESCALER</td>
<td>Divisor for TRACECLKIN is Prescaler + 1.</td>
</tr>
</tbody>
</table>

11.3.2 Formatter and Flush Status Register, TPIU_FFSR

The TPIU_FFSR characteristics are:

- **Purpose**: Indicates the status of the TPIU formatter.
- **Usage constraints**: There are no usage constraints.
- **Configurations**: This register is available in all processor configurations.
- **Attributes**: See Table 11-1 on page 11-5.

Figure 11-3 shows the TPIU_FFSR bit assignments.

![Figure 11-3 TPIU_FFSR bit assignments](image)
Table 11-3 shows the TPIU_FFSR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:4]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[3]</td>
<td>FtNonStop</td>
<td>Formatter cannot be stopped</td>
</tr>
<tr>
<td>[2]</td>
<td>TCPresent</td>
<td>This bit always reads zero</td>
</tr>
<tr>
<td>[1]</td>
<td>FtStopped</td>
<td>This bit always reads zero</td>
</tr>
<tr>
<td>[0]</td>
<td>FlInProg</td>
<td>This bit always reads zero</td>
</tr>
</tbody>
</table>

11.3.3 Formatter and Flush Control Register, TPIU_FFCR

The TPIU_FFCR characteristics are:

**Purpose**

Controls the TPIU formatter.

**Usage constraints**

There are no usage constraints.

**Configurations**

This register is available in all processor configurations.

**Attributes**

See Table 11-1 on page 11-5.

Figure 11-4 shows the TPIU_FFCR bit assignments.

<p>| | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 11-4 TPIU_FFCR bit assignments**

Table 11-4 shows the TPIU_FFCR bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:9]</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[8]</td>
<td>TrigIn</td>
<td>This bit Reads-As-One (RAO), specifying that triggers are inserted when a trigger pin is asserted.</td>
</tr>
<tr>
<td>[7:2]</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[1]</td>
<td>EnFCont</td>
<td>Enable continuous formatting. Value can be:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Continuous formatting disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Continuous formatting enabled.</td>
</tr>
<tr>
<td>[0]</td>
<td>-</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

The TPIU can output trace data in a Serial Wire Output (SWO) format. See Serial Wire Output format on page 11-4.
When one of the two SWO modes is selected, bit [1] of TPIU_FFCR enables the formatter to be bypassed. If the formatter is bypassed, only the ITM and DWT trace source passes through. The TPIU accepts and discards data from the ETM. This function is can be used to connect a device containing an ETM to a trace capture device that is only able to capture SWO data. Enabling or disabling the formatter causes momentary data corruption.

Note

If TPIU_SPPR is set to select Parallel Port Mode, the formatter is automatically enabled. If you then select one of the SWO modes, TPIU_FFCR reverts to its previously programmed value.

11.3.4 TRIGGER

The TRIGGER characteristics are:

Purpose
Integration test of the TRIGGER input.

Usage constraints
There are no usage constraints.

Configurations
This register is available in all processor configurations.

Attributes
See Table 11-1 on page 11-5.

Figure 11-5 shows the TRIGGER bit assignments.

Table 11-5 shows the TRIGGER bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:1]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[0]</td>
<td>TRIGGER input value</td>
<td>When read, this bit returns the TRIGGER input.</td>
</tr>
</tbody>
</table>

11.3.5 Integration ETM Data

The Integration ETM Data characteristics are:

Purpose
Trace data integration testing.

Usage constraints
You must set bit [1] of TPIU_ITCTRL to use this register. See Integration Mode Control, TPIU_ITCTRL on page 11-11.

Configurations
This register is available in all processor configurations.

Attributes
See Table 11-1 on page 11-5.

Figure 11-6 on page 11-9 shows the Integration ETM Data bit assignments.
Table 11-6 shows the Integration ETM Data bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:30]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[29]</td>
<td>ITM ATVALID input</td>
<td>Returns the value of the ITM ATVALID signal.</td>
</tr>
<tr>
<td>[28:27]</td>
<td>ITM byte count</td>
<td>Number of bytes of ITM trace data since last read of Integration ITM Data Register.</td>
</tr>
<tr>
<td>[26]</td>
<td>ETM ATVALID input</td>
<td>Returns the value of the ETM ATVALID signal.</td>
</tr>
<tr>
<td>[25:24]</td>
<td>ETM byte count</td>
<td>Number of bytes of ETM trace data since last read of Integration ETM Data Register.</td>
</tr>
<tr>
<td>[23:16]</td>
<td>ETM data 2</td>
<td>ETM trace data. The TPIU discards this data when the register is read.</td>
</tr>
<tr>
<td>[15:8]</td>
<td>ETM data 1</td>
<td></td>
</tr>
<tr>
<td>[7:0]</td>
<td>ETM data 0</td>
<td></td>
</tr>
</tbody>
</table>

### 11.3.6 ITATBCTR2

The ITATBCTR2 characteristics are:

**Purpose** Integration test.

**Usage constraints** You must set bit [0] of TPIU_ITCTRL to use this register. See Integration Mode Control, TPIU_ITCTRL on page 11-11.

**Configurations** This register is available in all processor configurations.

**Attributes** See Table 11-1 on page 11-5.

Figure 11-7 shows the ITATBCTR2 bit assignments.
11.3.7 Integration ITM Data

The Integration ITM Data characteristics are:

**Purpose**
Trace data integration testing.

**Usage constraints**
You must set bit [1] of TPIU_ITCTRL to use this register. See *Integration Mode Control, TPIU_ITCTRL* on page 11-11.

**Configurations**
This register is available in all processor configurations.

**Attributes**
See Table 11-1 on page 11-5.

Figure 11-8 shows the Integration ITM Data bit assignments.

Table 11-7 shows the ITATBCTR2 bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:1]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[0]</td>
<td>ATREADY1, ATREADY2</td>
<td>This bit sets the value of both the ETM and ITM ATREADY outputs, if the TPIU is in integration test mode.</td>
</tr>
</tbody>
</table>

### Table 11-7 ITATBCTR2 bit assignments

![Figure 11-8 Integration ITM Data bit assignments](image)

Table 11-8 shows the Integration ITM Data bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:30]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[29]</td>
<td>ITM ATVALID input</td>
<td>Returns the value of the ITM ATVALID signal.</td>
</tr>
<tr>
<td>[28:27]</td>
<td>ITM byte count</td>
<td>Number of bytes of ITM trace data since last read of Integration ITM Data Register.</td>
</tr>
<tr>
<td>[26]</td>
<td>ETM ATVALID input</td>
<td>Returns the value of the ETM ATVALID signal.</td>
</tr>
<tr>
<td>[25:24]</td>
<td>ETM byte count</td>
<td>Number of bytes of ETM trace data since last read of Integration ETM Data Register.</td>
</tr>
<tr>
<td>[23:16]</td>
<td>ITM data 2</td>
<td>ITM trace data. The TPIU discards this data when the register is read.</td>
</tr>
<tr>
<td>[15:8]</td>
<td>ITM data 1</td>
<td></td>
</tr>
<tr>
<td>[7:0]</td>
<td>ITM data 0</td>
<td></td>
</tr>
</tbody>
</table>
11.3.8 ITATBTCR0

The ITATBTCR0 characteristics are:

**Purpose** Integration test.

**Usage constraints** There are no usage constraints.

**Configurations** This register is available in all processor configurations.

**Attributes** See Table 11-1 on page 11-5.

Figure 11-9 shows the ITATBTCR0 bit assignments.

Table 11-9 shows the ITATBTCR0 bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:1]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[0]</td>
<td>ATVALID1, ATVALID2</td>
<td>A read of this bit returns the value of ATVALIDS1 OR-ed with ATVALIDS2.</td>
</tr>
</tbody>
</table>

Figure 11-9 ITATBTCR0 bit assignments

11.3.9 Integration Mode Control, TPIU_ITCTRL

The TPIU_ITCTRL characteristics are:

**Purpose** Specifies normal or integration mode for the TPIU.

**Usage constraints** There are no usage constraints.

**Configurations** This register is available in all processor configurations.

**Attributes** See Table 11-1 on page 11-5.

Figure 11-10 shows the TPIU_ITCTRL bit assignments.

Figure 11-10 TPIU_ITCTRL bit assignments
Table 11-10 shows the TPIU_ITCTRL bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:2]</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[1:0]</td>
<td>Mode</td>
<td>Specifies the current mode for the TPIU:</td>
</tr>
<tr>
<td></td>
<td>0b00</td>
<td>normal mode</td>
</tr>
<tr>
<td></td>
<td>0b01</td>
<td>integration test mode</td>
</tr>
<tr>
<td></td>
<td>0b10</td>
<td>integration data test mode</td>
</tr>
<tr>
<td></td>
<td>0b11</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In integration data test mode, the trace output is disabled, and data can be read directly from each input port using the integration data registers.</td>
</tr>
</tbody>
</table>

### 11.3.10 TPIU_DEVID

The TPIU_DEVID characteristics are:

**Purpose**
Indicates the functions provided by the TPIU for use in topology detection.

**Usage constraints**
There are no usage constraints.

**Configurations**
This register is available in all processor configurations.

**Attributes**
See Table 11-1 on page 11-5.

Figure 11-11 shows the TPIU_DEVID bit assignments.

![Figure 11-11 TPIU_DEVID bit assignments](image)

Table 11-11 shows the TPIU_DEVID bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:12]</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>[11]</td>
<td>Asynchronous Serial Wire Output (NRZ)</td>
<td>This bit Reads-As-One (RAO), indicating that the output is supported.</td>
</tr>
<tr>
<td>[10]</td>
<td>Asynchronous Serial Wire Output (Manchester)</td>
<td>This bit Reads-As-One (RAO), indicating that the output is supported.</td>
</tr>
<tr>
<td>[9]</td>
<td>Parallel trace port mode</td>
<td>This bit Reads-As-Zero (RAZ), indicating that parallel trace port mode is supported.</td>
</tr>
</tbody>
</table>
11.3.11 TPIU_DEVTYPE

The Device Type Identifier Register is read-only. It provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

The TPIU_DEVTYPE characteristics are:

**Purpose**
Indicates the type of functionality the component supports.

**Usage Constraints**
There are no usage constraints.

**Configurations**
This register is available in all processor configurations.

**Attributes**
The Device Type reads as 0x11 and indicates this device is a trace sink and specifically a TPIU.

If your implementation includes an ETM, the value of this field is 0b00001.

Figure 11-12 shows the TPIU_DEVTYPE bit assignments.

---

**Table 11-11 TPIU_DEVID bit assignments (continued)**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8:6]</td>
<td>Minimum buffer size</td>
<td>Specifies the minimum TPIU buffer size:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b010 = 4 bytes.</td>
</tr>
<tr>
<td>[5]</td>
<td>Asynchronous TRACECLKIN</td>
<td>Specifies whether TRACECLKIN can be asynchronous to CLK:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b1 = TRACECLKIN can be asynchronous to CLK.</td>
</tr>
<tr>
<td>[4:0]</td>
<td>Number of trace inputs</td>
<td>Specifies the number of trace inputs:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b000000 = 1 input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b000001 = 2 inputs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If your implementation includes an ETM, the value of this field is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b00001.</td>
</tr>
</tbody>
</table>

---

**Figure 11-12 TPIU_DEVTYPE bit assignments**
## Appendix A
### Revisions

This appendix describes the technical changes between released issues of this book.

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introductory processor information updated</td>
<td>Issue H distributes this information between <em>About the processor</em> on page 1-2 and <em>Features</em> on page 1-3 and removes duplicate information from these sections.</td>
</tr>
<tr>
<td>Processor block diagram updated</td>
<td>Figure 2-1 on page 2-2</td>
</tr>
<tr>
<td>Introductory information added, including:</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>• TPIU subsection</td>
<td></td>
</tr>
<tr>
<td>• Addition of note to SW/SWJ-DP subsection</td>
<td></td>
</tr>
<tr>
<td>• ROM table subsection</td>
<td></td>
</tr>
<tr>
<td>Introductory processor core information updated</td>
<td></td>
</tr>
<tr>
<td>APB bus now version 3.0</td>
<td><em>Architecture and protocol information</em> on page 1-7</td>
</tr>
<tr>
<td>Configurable options information expanded to include:</td>
<td><em>Configurable options</em> on page 1-5</td>
</tr>
<tr>
<td>• Added DWT configurability information</td>
<td></td>
</tr>
<tr>
<td>• New subsections for ITM, AHB-AP, FPB and Observation</td>
<td></td>
</tr>
<tr>
<td>New subsection added to list changes in functionality between r1p1 and r2p0</td>
<td><em>Differences in functionality between r1p1 and r2p0</em> on page 1-10</td>
</tr>
<tr>
<td>Information about the programmers model updated</td>
<td>Issue H distributes this information between <em>Operating modes</em> on page 3-3 and <em>Operating states</em> on page 3-3.</td>
</tr>
</tbody>
</table>
### Table A-1 Differences between issue E and issue F (continued)

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Definition of ICI field of Execution Program Status Register updated</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Table of nonsupported Thumb instructions removed.</td>
<td></td>
</tr>
<tr>
<td>Second footnote on Table 5-1 removed.</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Addition of note to vector table and reset description</td>
<td></td>
</tr>
<tr>
<td>Description of SLEEPING and SLEEPDEEP signals updated.</td>
<td></td>
</tr>
<tr>
<td>Description of extending sleep functionality added</td>
<td></td>
</tr>
<tr>
<td>Addition of Auxiliary Control Register</td>
<td>Auxiliary Control Register, ACTLR on page 4-5</td>
</tr>
<tr>
<td>Irq 0 to 31 Priority Register amended to Irq 0 to 3 Priority Register</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Irq 236 to 239 Priority Register amended to Irq 224 to 239 Priority Register</td>
<td></td>
</tr>
<tr>
<td><strong>HCLK</strong> changed to <strong>FCLK</strong></td>
<td></td>
</tr>
<tr>
<td>Addition of ascending MPU region priority information</td>
<td>About the MPU on page 5-2</td>
</tr>
<tr>
<td>Extra paragraph added.</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Debug Core Register Selector Register REGSEL bit field function updated</td>
<td></td>
</tr>
<tr>
<td>Paragraph added about removing FPB</td>
<td></td>
</tr>
<tr>
<td>Addition of note about configuring flash patch registers to be present or not</td>
<td>FPB programmers model on page 7-10</td>
</tr>
<tr>
<td>First bullet point updated</td>
<td>About the DWT on page 8-2</td>
</tr>
<tr>
<td>Addition of note about configuring DWT registers to be present or not</td>
<td>DWT Programmers Model on page 8-4</td>
</tr>
<tr>
<td>DWT Control Register reset state updated</td>
<td>Table 8-1 on page 8-4</td>
</tr>
<tr>
<td>DWT Control Register bit assignments updated</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Addition of note about configuring ITM registers to be present or not</td>
<td>ITM programmers model on page 9-4</td>
</tr>
<tr>
<td>ITM Trace Control Register TSENA field bit function updated</td>
<td></td>
</tr>
<tr>
<td>Addition of note about configuring AHB-AP registers to be present or not</td>
<td>AHB-AP programmers model on page 7-6</td>
</tr>
<tr>
<td>AHB-AP Banked Data Register DATA field reset value removed</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Addition of information about absence of debug functionality</td>
<td>About debug on page 7-2</td>
</tr>
<tr>
<td>Information about exclusive memory accesses updated</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Note about bit-band accesses updated</td>
<td>Bit-banding on page 3-16</td>
</tr>
<tr>
<td>ETM block diagram updated</td>
<td>Figure 10-1 on page 10-3</td>
</tr>
</tbody>
</table>
### Table A-1 Differences between issue E and issue F (continued)

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCLK and CLK replaced by FCLK</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>ETM Trigger Even Register description upgraded</td>
<td></td>
</tr>
<tr>
<td>ETM Status Register description updated</td>
<td></td>
</tr>
<tr>
<td>TraceEnable register replaced by Trace Start/Stop Resource Control</td>
<td></td>
</tr>
<tr>
<td>TraceEnable Control 2 register added</td>
<td></td>
</tr>
<tr>
<td>Lock Status Register added</td>
<td></td>
</tr>
<tr>
<td>Description of FIFOFULL Region Register added</td>
<td></td>
</tr>
<tr>
<td>Description of FIFOFULL Level Register updated</td>
<td></td>
</tr>
<tr>
<td>Description of CoreSight Trace ID Register updated</td>
<td></td>
</tr>
<tr>
<td>Description ETM Control Register implementation bits expanded</td>
<td>Main Control Register, ETMCR on page 10-11</td>
</tr>
<tr>
<td>Description of TraceEnable Control 1 Register updated</td>
<td>TraceEnable Control 1 Register, ETMTECR1 on page 10-16</td>
</tr>
<tr>
<td>Description ETM ID Register updated to reflect revision 2</td>
<td>ID Register, ETMIDR on page 10-17</td>
</tr>
<tr>
<td>Subsection describing ETM Event Resources added</td>
<td>Resources on page 10-3</td>
</tr>
<tr>
<td>Subsection describing Cross Trigger Interface added</td>
<td>Recommended CTI connections on page 10-7</td>
</tr>
<tr>
<td>Branch status interface section updated</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Note about HADDRICore and HTRANSICore removed</td>
<td></td>
</tr>
<tr>
<td>Example of an opcode sequence timing diagram updated</td>
<td></td>
</tr>
<tr>
<td>Description of APB interface inputs added</td>
<td></td>
</tr>
<tr>
<td>Addition of note about configuring TPIU registers to be present or not</td>
<td>TPIU programmers model on page 11-5</td>
</tr>
<tr>
<td>The following TPIU registers removed from summary table and descriptions:</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>• Trigger control registers</td>
<td></td>
</tr>
<tr>
<td>• EXTCTL port registers</td>
<td></td>
</tr>
<tr>
<td>• Test pattern registers</td>
<td></td>
</tr>
<tr>
<td>The following TPIU registers added to the summary table and descriptions:</td>
<td></td>
</tr>
<tr>
<td>• Integration Register: TRIGGER</td>
<td></td>
</tr>
<tr>
<td>• Integration Mode Control Register</td>
<td></td>
</tr>
<tr>
<td>• Integration Register: FIFO data 0</td>
<td></td>
</tr>
<tr>
<td>• Integration Register: FIFO data 1</td>
<td></td>
</tr>
<tr>
<td>• Claim tag set register</td>
<td></td>
</tr>
<tr>
<td>• Claim tag clear register</td>
<td></td>
</tr>
<tr>
<td>• Device ID register</td>
<td></td>
</tr>
<tr>
<td>• PID registers</td>
<td></td>
</tr>
<tr>
<td>• CID registers</td>
<td></td>
</tr>
<tr>
<td>Change</td>
<td>Location</td>
</tr>
<tr>
<td>-----------------------------------------------------------------------</td>
<td>----------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Wake-up Interrupt Controller (WIC) added to Cortex-M3 block diagram</td>
<td>Figure 2-1 on page 2-2</td>
</tr>
<tr>
<td>Section 1-2 and section 1-3 combined</td>
<td>Issue H distributes this information between Features on page 1-3, Interfaces on page 1-4, and Configurable options on page 1-5.</td>
</tr>
<tr>
<td>New subsection added to list changes in functionality between r1p1 and r2p0</td>
<td>Differences in functionality between r1p1 and r2p0 on page 1-10</td>
</tr>
<tr>
<td>New subsection added to describe the WIC</td>
<td>Low power modes on page 6-3</td>
</tr>
<tr>
<td>New bullet point to describe FIXHASTERTYPE pin</td>
<td>Differences in functionality between r1p1 and r2p0 on page 1-10</td>
</tr>
<tr>
<td>Table of supported instruction removed</td>
<td>Issue H reinstates this information in Table 3-1 on page 3-4.</td>
</tr>
<tr>
<td>More information added about the stacked xPSR</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>Reset value of Configuration Control Register changed to 0x00000200</td>
<td></td>
</tr>
<tr>
<td>System and Vendor_SYS memory regions added to table of memory region permissions</td>
<td></td>
</tr>
<tr>
<td>Memory region for Private Peripheral Bus changed to +00000000</td>
<td></td>
</tr>
<tr>
<td>SLEEPHOLDREQ changed to SLEEPHOLDREQn</td>
<td></td>
</tr>
<tr>
<td>SLEEPHOLDACK changed to SLEEPHOLDACKn</td>
<td></td>
</tr>
<tr>
<td>DEEPSLEEP signal changed to SLEEPDEEP</td>
<td></td>
</tr>
<tr>
<td>DBGRESTARTACK changed to DBGRESTARTED</td>
<td></td>
</tr>
<tr>
<td>DBGRESTARTREQ changed to DBGRESTART</td>
<td></td>
</tr>
<tr>
<td>New subsection added to describe the WIC</td>
<td></td>
</tr>
<tr>
<td>Address of Irq 224 to 239 Priority Register changed to 0xE000E4EC</td>
<td></td>
</tr>
<tr>
<td>Enhanced description of function of C_MASKINTS field</td>
<td></td>
</tr>
<tr>
<td>Settings for DWT Function Registers updated</td>
<td></td>
</tr>
<tr>
<td>Minor change to timing information of ETMIA</td>
<td></td>
</tr>
</tbody>
</table>
Table A-2 Differences between issue F and issue G (continued)

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change to timing information for ETMIVVALID</td>
<td>Issue H removes this information.</td>
</tr>
<tr>
<td>SLEEPHOLDREQn removed from table of miscellaneous input</td>
<td></td>
</tr>
<tr>
<td>ports timing parameters</td>
<td></td>
</tr>
<tr>
<td>Table of low power input ports timing parameters</td>
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<tr>
<td>FIXHMASTERTYPE added to table of debug input ports timing</td>
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<td>Input changed to Output in table header</td>
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<tr>
<td>SLEEPING, SLEEPDEEP, and SLEEPHOLDACKn removed from</td>
<td></td>
</tr>
<tr>
<td>table of miscellaneous output ports timing parameters</td>
<td></td>
</tr>
<tr>
<td>SLEEPDEEP, SLEEPING, SLEEPHOLDREQ, and SLEEPHOLDACK removed</td>
<td></td>
</tr>
<tr>
<td>New section added to describe the low power interface signals</td>
<td></td>
</tr>
<tr>
<td>New section added to describe the WIC interface signals</td>
<td></td>
</tr>
<tr>
<td>SLEEPHOLDACKn removed from table of miscellaneous signals</td>
<td></td>
</tr>
<tr>
<td>Asserted changed to de-asserted in the description of</td>
<td></td>
</tr>
<tr>
<td>SLEEPHOLDREQn in table of low power interface signals</td>
<td></td>
</tr>
<tr>
<td>FIXMASTERTYPE added to list of AHB-AP interface signals</td>
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</tr>
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</table>

**Note**

Issue H of this book is significantly reorganized and simplified to eliminate duplication of information contained in the ARM Architecture Reference Manual and other ARM documentation.

Table A-3 Differences between issue G and issue H

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
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</thead>
<tbody>
<tr>
<td>Chapter 1 simplified to provide only a high-level description of the</td>
<td>Chapter 1 Introduction</td>
</tr>
<tr>
<td>processor. Some information to Chapter 2.</td>
<td>Chapter 2 Functional Description</td>
</tr>
<tr>
<td>Removed the following sections from Chapter 1:</td>
<td>See the <em>ARMv7-M Architecture Reference Manual</em> and the implementation documentation for the processor.</td>
</tr>
<tr>
<td>• Execution pipeline stages</td>
<td></td>
</tr>
<tr>
<td>• Prefetch unit</td>
<td></td>
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<tr>
<td>• Branch target forwarding</td>
<td></td>
</tr>
<tr>
<td>• Store buffers.</td>
<td></td>
</tr>
<tr>
<td>Added functional description chapter</td>
<td>Chapter 2 Functional Description</td>
</tr>
<tr>
<td>Simplified description of the programmers model and modes of operation</td>
<td>About the programmers model on page 3-2</td>
</tr>
<tr>
<td>and execution</td>
<td>Modes of operation and execution on page 3-3</td>
</tr>
<tr>
<td>Added cycle counts to instruction set summary</td>
<td>Instruction set summary on page 3-4</td>
</tr>
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</table>
### Table A-3 Differences between issue G and issue H (continued)

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Descriptions of the memory system and of exceptions moved to Chapter 3</td>
<td>Chapter 3 <em>Programmers Model</em></td>
</tr>
<tr>
<td>Component-specific registers moved from System Control chapter to appropriate chapters within the manual.</td>
<td>Chapter 4 <em>System Control</em></td>
</tr>
<tr>
<td>Deleted Clocking and Resets chapter.</td>
<td>See the implementation documentation for the processor.</td>
</tr>
<tr>
<td>Deleted Power Management chapter.</td>
<td></td>
</tr>
<tr>
<td>In the Memory Protection Unit and Nested Vector Interrupt Controller chapters, removed description of architecturally-defined registers.</td>
<td></td>
</tr>
<tr>
<td>Reorganized debug description into a single chapter.</td>
<td>Chapter 7 <em>Debug</em></td>
</tr>
<tr>
<td>Deleted Bus Interface chapter and moved high-level information to appropriate chapters.</td>
<td>Chapter 1 <em>Introduction</em> Chapter 2 <em>Functional Description</em> Chapter 3 <em>Programmers Model</em></td>
</tr>
<tr>
<td>Deleted Debug Port chapter and incorporated general information from this chapter into chapters 2 and 7.</td>
<td>Chapter 2 <em>Functional Description</em> Chapter 7 <em>Debug</em></td>
</tr>
<tr>
<td>Moved information from the System Debug chapter to create new chapters for the Data Watchpoint and Trace Unit and the Instrumentation Trace Macrocell Unit.</td>
<td>Chapter 8 <em>Data Watchpoint and Trace Unit</em> Chapter 9 <em>Instrumentation Trace Macrocell Unit</em></td>
</tr>
<tr>
<td>Reorganized Embedded Trace Macrocell description into a single chapter.</td>
<td>Chapter 10 <em>Embedded Trace Macrocell</em></td>
</tr>
<tr>
<td>Removed signal information and architecturally-defined register descriptions from the Trace Port Interface Unit chapter.</td>
<td>Removed duplicate information. See the <em>ARMv7-M Architecture Reference Manual</em> and the implementation documentation for the processor.</td>
</tr>
<tr>
<td>Moved instruction timing information to chapter 3.</td>
<td><em>Instruction set summary</em> on page 3-4</td>
</tr>
<tr>
<td>Removed AC Characteristics and Signal Descriptions chapters.</td>
<td>See the implementation documentation for the processor.</td>
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### Table A-4 Differences between issue H and issue I

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated Bus interfaces information.</td>
<td><em>Bus interfaces</em> on page 2-4</td>
</tr>
<tr>
<td>Added information on Private Peripheral Bus</td>
<td><em>Private Peripheral Bus (PPB)</em> on page 2-5</td>
</tr>
<tr>
<td>Updated Load/store timings information.</td>
<td><em>Load/store timings</em> on page 3-8</td>
</tr>
<tr>
<td>Updated Exclusive monitor information.</td>
<td><em>Exclusive monitor</em> on page 3-15</td>
</tr>
<tr>
<td>Updated Reset values for Register summary information.</td>
<td>Table 4-1 on page 4-3</td>
</tr>
<tr>
<td>Reset values updated.</td>
<td>Table 4-1 on page 4-3</td>
</tr>
<tr>
<td>Updated Reset values for MPU register information.</td>
<td>Table 5-1 on page 5-4</td>
</tr>
<tr>
<td>Changed address range of NVIC_IPR registers.</td>
<td>Table 6-1 on page 6-4</td>
</tr>
<tr>
<td>Updated values for the Cortex-M3 ROM table information and added Peripheral IDs 5-7.</td>
<td>Table 7-1 on page 7-3</td>
</tr>
</tbody>
</table>
Table A-4 Differences between issue H and issue I (continued)

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
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</thead>
<tbody>
<tr>
<td>Added Timestamp format information.</td>
<td>Timestamp format on page 10-6</td>
</tr>
<tr>
<td>Added ETM register descriptions.</td>
<td>Table 10-6 on page 10-9</td>
</tr>
<tr>
<td>Added ETMCNTRLDVR1 ETM register.</td>
<td>Table 10-6 on page 10-9</td>
</tr>
<tr>
<td>Changed reset values for ETMVCCR and ETMCCER.</td>
<td>Table 10-6 on page 10-9</td>
</tr>
<tr>
<td>Updated ETMCR register bit assignments.</td>
<td>Table 10-7 on page 10-12</td>
</tr>
<tr>
<td>Updated ETMCCR bit assignments.</td>
<td>Table 10-8 on page 10-14</td>
</tr>
<tr>
<td>Updated ETMCCER bit assignments.</td>
<td>Table 10-12 on page 10-18</td>
</tr>
<tr>
<td>Added TPIU_DEVTYPE TPIU Register. Changed reset values.</td>
<td>Table 11-1 on page 11-5</td>
</tr>
<tr>
<td>Updated TPIU Formatter information</td>
<td>TPIU Formatter on page 11-3</td>
</tr>
<tr>
<td>Replaced FIFO 0 with ETM.</td>
<td>Integration ETM Data on page 11-8</td>
</tr>
<tr>
<td></td>
<td>Integration ITM Data on page 11-10</td>
</tr>
<tr>
<td>Replaced FIFO 1 with ITM</td>
<td>Integration ETM Data on page 11-8</td>
</tr>
<tr>
<td></td>
<td>Integration ITM Data on page 11-10</td>
</tr>
<tr>
<td>Added TPIU_DEVTYPE Register description.</td>
<td>TPIU_DEVTYPE on page 11-13</td>
</tr>
</tbody>
</table>
This glossary describes some of the terms used in technical documents from ARM.

**Abort**

A mechanism that indicates to a core that the attempted memory access is invalid or not allowed or that the data returned by the memory access is invalid. An abort can be caused by the external or internal memory system as a result of attempting to access invalid or protected instruction or data memory.

*See also* Data Abort, External Abort and Prefetch Abort.

**Addressing modes**

Various mechanisms, shared by many different instructions, for generating values used by the instructions.

**Advanced High-performance Bus (AHB)**

A bus protocol with a fixed pipeline between address/control and data phases. It only supports a subset of the functionality provided by the AMBA AXI protocol. The full AMBA AHB protocol specification includes a number of features that are not commonly required for master and slave IP developments and ARM recommends only a subset of the protocol is usually used. This subset is defined as the AMBA AHB-Lite protocol.

*See also* Advanced Microcontroller Bus Architecture and AHB-Lite.

**Advanced Microcontroller Bus Architecture (AMBA)**

A family of protocol specifications that describe a strategy for the interconnect. AMBA is the ARM open standard for on-chip buses. It is an on-chip bus specification that details a strategy for the interconnection and management of functional blocks that make up a *System-on-Chip* (SoC). It aids in the development of embedded processors with one or more CPUs or signal processors and multiple peripherals. AMBA complements a reusable design methodology by defining a common backbone for SoC modules.
**Advanced Peripheral Bus (APB)**
A simpler bus protocol than AXI and AHB. It is designed for use with ancillary or general-purpose peripherals such as timers, interrupt controllers, UARTs, and I/O ports. Connection to the main system bus is through a system-to-peripheral bus bridge that helps to reduce system power consumption.

**AHB**
*See Advanced High-performance Bus.*

**AHB Access Port (AHB-AP)**
An optional component of the DAP that provides an AHB interface to a SoC.

**AHB-AP**
*See AHB Access Port.*

**AHB-Lite**
A subset of the full AMBA AHB protocol specification. It provides all of the basic functions required by the majority of AMBA AHB slave and master designs, particularly when used with a multi-layer AMBA interconnect. In most cases, the extra facilities provided by a full AMBA AHB interface are implemented more efficiently by using an AMBA AXI protocol interface.

**AHB Trace Macrocell**
A hardware macrocell that, when connected to a processor core, outputs data trace information on a trace port.

**Aligned**
A data item stored at an address that is divisible by the number of bytes that defines the data size is said to be aligned. Aligned words and halfwords have addresses that are divisible by four and two respectively. The terms word-aligned and halfword-aligned therefore stipulate addresses that are divisible by four and two respectively.

**AMBA**
*See Advanced Microcontroller Bus Architecture.*

**Advanced Trace Bus (ATB)**
A bus used by trace devices to share CoreSight capture resources.

**APB**
*See Advanced Peripheral Bus.*

**Application Specific Integrated Circuit (ASIC)**
An integrated circuit that has been designed to perform a specific application function. It can be custom-built or mass-produced.

**Architecture**
The organization of hardware and/or software that characterizes a processor and its attached components, and enables devices with similar characteristics to be grouped together when describing their behavior, for example, Harvard architecture, instruction set architecture, ARMv7-M architecture.

**ARM instruction**
An instruction of the ARM Instruction Set Architecture (ISA). These cannot be executed by the Cortex-M3 processor.

**ARM state**
The processor state in which the processor executes the instructions of the ARM ISA. The processor only operates in Thumb state, never in ARM state.

**ASIC**
*See Application Specific Integrated Circuit.*

**ATB**
*See Advanced Trace Bus.*

**ATB bridge**
A synchronous ATB bridge provides a register slice to facilitate timing closure through the addition of a pipeline stage. It also provides a unidirectional link between two synchronous ATB domains.

An asynchronous ATB bridge provides a unidirectional link between two ATB domains with asynchronous clocks. It is intended to support connection of components with ATB ports residing in different clock domains.
**Base register**
A register specified by a load or store instruction that is used to hold the base value for the address calculation for the instruction. Depending on the instruction and its addressing mode, an offset can be added to or subtracted from the base register value to form the address that is sent to memory.

**Base register write-back**
Updating the contents of the base register used in an instruction target address calculation so that the modified address is changed to the next higher or lower sequential address in memory. This means that it is not necessary to fetch the target address for successive instruction transfers and enables faster burst accesses to sequential memory.

**Beat**
Alternative word for an individual data transfer within a burst. For example, an INCR4 burst comprises four beats.

**BE-8**
Big-endian view of memory in a byte-invariant system.

*See also* BE-32, LE, Byte-invariant and Word-invariant.

**BE-32**
Big-endian view of memory in a word-invariant system.

*See also* BE-8, LE, Byte-invariant and Word-invariant.

**Big-endian**
Byte ordering scheme in which bytes of decreasing significance in a data word are stored at increasing addresses in memory.

*See also* Little-endian and Endianness.

**Big-endian memory**
Memory in which:

- a byte or halfword at a word-aligned address is the most significant byte or halfword within the word at that address
- a byte at a halfword-aligned address is the most significant byte within the halfword at that address.

*See also* Little-endian memory.

**Boundary scan chain**
A boundary scan chain is made up of serially-connected devices that implement boundary scan technology using a standard JTAG TAP interface. Each device contains at least one TAP controller containing shift registers that form the chain connected between TDI and TDO, through which test data is shifted. Processors can contain several shift registers to enable you to access selected parts of the device.

**Branch folding**
Branch folding is a technique where the branch instruction is completely removed from the instruction stream presented to the execution pipeline.

**Breakpoint**
A breakpoint is a mechanism provided by debuggers to identify an instruction at which program execution is to be halted. Breakpoints are inserted by the programmer to enable inspection of register contents, memory locations, variable values at fixed points in the program execution to test that the program is operating correctly. Breakpoints are removed after the program is successfully tested.

*See also* Watchpoint.

**Burst**
A group of transfers to consecutive addresses. Because the addresses are consecutive, there is no requirement to supply an address for any of the transfers after the first one. This increases the speed at which the group of transfers can occur. Bursts over AMBA are controlled using signals to indicate the length of the burst and how the addresses are incremented.

*See also* Beat.
**Glossary**

**Byte**  
An 8-bit data item.

**Byte-invariant**  
In a byte-invariant system, the address of each byte of memory remains unchanged when switching between little-endian and big-endian operation. When a data item larger than a byte is loaded from or stored to memory, the bytes making up that data item are arranged into the correct order depending on the endianness of the memory access. The ARM architecture supports byte-invariant systems in ARMv6 and later versions. When byte-invariant support is selected, unaligned halfword and word memory accesses are also supported. Multi-word accesses are expected to be word-aligned.

*See also* Word-invariant.

**Clock gating**  
Gating a clock signal for a macrocell with a control signal and using the modified clock that results to control the operating state of the macrocell.

**Clocks Per Instruction (CPI)**  
*See* Cycles Per Instruction (CPI).

**Cold reset**  
Also known as power-on reset.

*See also* Warm reset.

**Context**  
The environment that each process operates in for a multitasking operating system.

*See also* Fast context switch.

**Core**  
A core is that part of a processor that contains the ALU, the datapath, the general-purpose registers, the Program Counter, and the instruction decode and control circuitry.

**Core reset**  
*See* Warm reset.

**CoreSight**  
The infrastructure for monitoring, tracing, and debugging a complete system on chip.

**CPI**  
*See* Cycles per instruction.

**Cycles Per Instruction (CPI)**  
Cycles per instruction (or clocks per instruction) is a measure of the number of computer instructions that can be performed in one clock cycle. This figure of merit can be used to compare the performance of different CPUs that implement the same instruction set against each other. The lower the value, the better the performance.

**Data Abort**  
An indication from a memory system to the core of an attempt to access an illegal data memory location. An exception must be taken if the processor attempts to use the data that caused the abort.

*See also* Abort.

**DCode Memory**  
Memory space at 0x00000000 to 0xFFFFFFFF.

**Debug Access Port (DAP)**  
A TAP block that acts as an AMBA, AHB or AHB-Lite, master for access to a system bus. The DAP is the term used to encompass a set of modular blocks that support system wide debug. The DAP is a modular component, intended to be extendable to support optional access to multiple systems such as memory mapped AHB and CoreSight APB through a single debug interface.

**Debugger**  
A debugging system that includes a program, used to detect, locate, and correct software faults, together with custom hardware that supports software debugging.

**Embedded Trace Buffer**  
The ETB provides on-chip storage of trace data using a configurable sized RAM.
Embedded Trace Macrocell (ETM)
A hardware macrocell that, when connected to a processor core, outputs instruction trace information on a trace port.

Endianness
The scheme that determines the order of successive bytes of a data word when it is stored in memory.

See also Little-endian and Big-endian

ETB
See Embedded Trace Buffer.

ETM
See Embedded Trace Macrocell.

Exception
An error or event which can cause the processor to suspend the currently executing instruction stream and execute a specific exception handler or interrupt service routine. The exception could be an external interrupt or NMI, or it could be a fault or error event that is considered serious enough to require that program execution is interrupted. Examples include attempting to perform an invalid memory access, external interrupts, and undefined instructions. When an exception occurs, normal program flow is interrupted and execution is resumed at the corresponding exception vector. This contains the first instruction of the interrupt service routine to deal with the exception.

Exception handler
See Interrupt service routine.

Exception vector
See Interrupt vector.

External PPB
PPB memory space at 0xE0040000 to 0xE00FFFFF.

Flash Patch and Breakpoint unit (FPB)
A set of address matching tags, that reroute accesses into flash to a special part of SRAM. This permits patching flash locations for breakpointing and quick fixes or changes.

Formatter
The formatter is an internal input block in the ETB and TPIU that embeds the trace source ID within the data to create a single trace stream.

Halfword
A 16-bit data item.

Halt mode
One of two mutually exclusive debug modes. In halt mode all processor execution halts when a breakpoint or watchpoint is encountered. All processor state, coprocessor state, memory and input/output locations can be examined and altered by the JTAG interface.

See also Monitor debug-mode.

Host
A computer that provides data and other services to another computer. Especially, a computer providing debugging services to a target being debugged.

HTM
See AHB Trace Macrocell.

ICode Memory
Memory space at 0x00000000 to 0x3FFFFFFF.

Illegal instruction
An instruction that is architecturally Undefined.

Implementation-defined
The behavior is not architecturally defined, but is defined and documented by individual implementations.

Implementation-specific
The behavior is not architecturally defined, and does not have to be documented by individual implementations. Used when there are a number of implementation options available and the option chosen does not affect software compatibility.
Instruction cycle count
The number of cycles for which an instruction occupies the Execute stage of the pipeline.

Instrumentation trace
A component for debugging real-time systems through a simple memory-mapped trace interface, providing printf() style debugging.

Intelligent Energy Management (IEM)
A technology that enables dynamic voltage scaling and clock frequency variation to be used to reduce power consumption in a device.

Internal PPB
PPB memory space at 0xE0000000 to 0xE003FFFF.

Interrupt service routine
A program that control of the processor is passed to when an interrupt occurs.

Interrupt vector
One of a number of fixed addresses in low memory that contains the first instruction of the corresponding interrupt service routine.

Joint Test Action Group (JTAG)
The name of the organization that developed standard IEEE 1149.1. This standard defines a boundary-scan architecture used for in-circuit testing of integrated circuit devices. It is commonly known by the initials JTAG.

JTAG
See Joint Test Action Group.

JTAG Debug Port (JTAG-DP)
An optional external interface for the DAP that provides a standard JTAG interface for debug access.

JTAG-DP
See JTAG Debug Port.

LE
Little-endian view of memory in both byte-invariant and word-invariant systems. See also Byte-invariant, Word-invariant.

Little-endian
Byte ordering scheme in which bytes of increasing significance in a data word are stored at increasing addresses in memory.

See also Big-endian and Endianness.

Little-endian memory
Memory in which:
- a byte or halfword at a word-aligned address is the least significant byte or halfword within the word at that address
- a byte at a halfword-aligned address is the least significant byte within the halfword at that address.

See also Big-endian memory.

Load/store architecture
A processor architecture where data-processing operations only operate on register contents, not directly on memory contents.

Load Store Unit (LSU)
The part of a processor that handles load and store transfers.

LSU
See Load Store Unit.

Macrocell
A complex logic block with a defined interface and behavior. A typical VLSI system comprises several macrocells (such as a processor, an ETM, and a memory block) plus application-specific logic.
Memory coherency  A memory is coherent if the value read by a data read or instruction fetch is the value that was most recently written to that location. Memory coherency is made difficult when there are multiple possible physical locations that are involved, such as a system that has main memory, a write buffer and a cache.

Memory Protection Unit (MPU)  Hardware that controls access permissions to blocks of memory. Unlike an MMU, an MPU does not modify addresses.

Microprocessor  See Processor.

Monitor debug-mode  One of two mutually exclusive debug modes. In Monitor debug-mode the processor enables a software abort handler provided by the debug monitor or operating system debug task. When a breakpoint or watchpoint is encountered, this enables vital system interrupts to continue to be serviced while normal program execution is suspended.

See also Halt mode.

MPU  See Memory Protection Unit.

Multi-layer  An interconnect scheme similar to a cross-bar switch. Each master on the interconnect has a direct link to each slave, the link is not shared with other masters. This enables each master to process transfers in parallel with other masters. Contention only occurs in a multi-layer interconnect at a payload destination, typically the slave.

Nested Vectored Interrupt Controller (NVIC)  Provides the processor with configurable interrupt handling abilities.

NMI  See Non-maskable interrupt

Non-maskable interrupt  A NonMaskable Interrupt (NMI) can be signalled by a peripheral or triggered by software. This is the highest priority exception other than reset. It is permanently enabled and has a fixed priority of -2. NMIs cannot be:

• masked or prevented from activation by any other exception
• preempted by any exception other than Reset.

NVIC  See Nested Vectored Interrupt Controller.

Penalty  The number of cycles in which no useful Execute stage pipeline activity can occur because an instruction flow is different from that assumed or predicted.

PFU  See Prefetch Unit.

PMU  See Power Management Unit.

Power Management Unit (PMU)  Provides the processor with power management capability.

Power-on reset  See Cold reset.

PPB  See Private Peripheral Bus.

Prefetching  In pipelined processors, the process of fetching instructions from memory to fill up the pipeline before the preceding instructions have finished executing. Prefetching an instruction does not mean that the instruction has to be executed.
Prefetch Abort

An indication from a memory system to the core that an instruction has been fetched from an illegal memory location. An exception must be taken if the processor attempts to execute the instruction. A Prefetch Abort can be caused by the external or internal memory system as a result of attempting to access invalid instruction memory.

See also Data Abort, Abort.

Prefetch Unit (PFU)

The PFU fetches instructions from the memory system that can supply one word each cycle. The PFU buffers up to three word fetches in its FIFO, which means that it can buffer up to three 32-bit Thumb instructions or six 16-bit Thumb instructions.

Private Peripheral Bus

Memory space at 0xE0000000 to 0xE00FFFFF.

Processor

A processor is the circuitry in a computer system required to process data using the computer instructions. It is an abbreviation of microprocessor. A clock source, power supplies, and main memory are also required to create a minimum complete working computer system.

RW1C

Register bits marked RW1C can be read normally and support write-one-to-clear. A read then write of the result back to the register will clear all bits set. RW1C protects against read-modify-write errors occurring on bits set between reading the register and writing the value back (since they are written as zero, they will not be cleared).

RealView ICE

A system for debugging embedded processor cores using a JTAG interface.

Reserved

A field in a control register or instruction format is reserved if the field is to be defined by the implementation, or produces Unpredictable results if the contents of the field are not zero. These fields are reserved for use in future extensions of the architecture or are implementation-specific. All reserved bits not used by the implementation must be written as 0 and read as 0.

Scan chain

A scan chain is made up of serially-connected devices that implement boundary scan technology using a standard JTAG TAP interface. Each device contains at least one TAP controller containing shift registers that form the chain connected between TDI and TDO, through which test data is shifted. Processors can contain several shift registers to enable you to access selected parts of the device.

Serial-Wire Debug Port

An optional external interface for the DAP that provides a serial-wire bidirectional debug interface.

Serial-Wire JTAG Debug Port

A standard debug port that combines JTAG-DP and SW-DP.

SW-DP

See Serial-Wire Debug Port.

SWJ-DP

See Serial-Wire JTAG Debug Port.

Synchronization primitive

The memory synchronization primitive instructions are those instructions that are used to ensure memory synchronization. That is, the LDREX and STREX instructions.

System memory

Memory space at 0x20000000 to 0xFFFFFFFF, excluding PPB space at 0xE0000000 to 0xE00FFFFF.

TAP

See Test access port.

Test Access Port (TAP)

The collection of four mandatory and one optional terminals that form the input/output and control interface to a JTAG boundary-scan architecture. The mandatory terminals are TDI, TDO, TMS, and TCK. The optional terminal is TRST. This signal is mandatory in ARM cores because it is used to reset the debug logic.
<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thread Control Block</td>
<td>A data structure used by an operating system kernel to maintain information specific to a single thread of execution.</td>
</tr>
<tr>
<td>Thumb instruction</td>
<td>A halfword that specifies an operation for an ARM processor in Thumb state to perform. Thumb instructions must be halfword-aligned.</td>
</tr>
<tr>
<td>Thumb state</td>
<td>A processor that is executing Thumb (16-bit) halfword aligned instructions is operating in Thumb state.</td>
</tr>
<tr>
<td>TPA</td>
<td>See Trace Port Analyzer.</td>
</tr>
<tr>
<td>TPIU</td>
<td>See Trace Port Interface Unit.</td>
</tr>
<tr>
<td>Trace Port Analyzer (TPA)</td>
<td>A hardware device that captures trace information output on a trace port. This can be a low-cost product designed specifically for trace acquisition, or a logic analyzer.</td>
</tr>
<tr>
<td>Trace Port Interface Unit (TPIU)</td>
<td>Drains trace data and acts as a bridge between the on-chip trace data and the data stream captured by a TPA.</td>
</tr>
<tr>
<td>Unaligned</td>
<td>A data item stored at an address that is not divisible by the number of bytes that defines the data size is said to be unaligned. For example, a word stored at an address that is not divisible by four.</td>
</tr>
<tr>
<td>Wake-up Interrupt Controller (WIC)</td>
<td>The Wake-up Interrupt Controller provides significantly reduced gate count interrupt detection and prioritization logic.</td>
</tr>
<tr>
<td>Warm reset</td>
<td>Also known as a core reset. initializes the majority of the processor excluding the debug controller and debug logic. This type of reset is useful if you are using the debugging features of a processor.</td>
</tr>
<tr>
<td>Watchpoint</td>
<td>A watchpoint is a mechanism provided by debuggers to halt program execution when the data contained by a particular memory address is changed. Watchpoints are inserted by the programmer to enable inspection of register contents, memory locations, and variable values when memory is written to test that the program is operating correctly. Watchpoints are removed after the program is successfully tested. See also Breakpoint.</td>
</tr>
<tr>
<td>WIC</td>
<td>See Wake-up Interrupt Controller.</td>
</tr>
<tr>
<td>Word</td>
<td>A 32-bit data item.</td>
</tr>
<tr>
<td>Word-invariant</td>
<td>In a word-invariant system, the address of each byte of memory changes when switching between little-endian and big-endian operation, in such a way that the byte with address A in one endianness has address A EOR 3 in the other endianness. As a result, each aligned word of memory always consists of the same four bytes of memory in the same order, regardless of endianness. The change of endianness occurs because of the change to the byte addresses, not because the bytes are rearranged. The ARM architecture supports word-invariant systems in ARMv3 and later versions. When word-invariant support is selected, the behavior of load or store instructions that are given unaligned addresses is instruction-specific, and is in general not the expected behavior for an unaligned access. It is recommended that word-invariant systems use the endianness that produces the required byte addresses at all times, apart possibly from very early in their reset handlers before they have set up the endianness, and that this early part of the reset handler must use only aligned word memory accesses. See also Byte-invariant.</td>
</tr>
<tr>
<td>Write buffer</td>
<td>A pipeline stage for buffering write data to prevent bus stalls from stalling the processor.</td>
</tr>
</tbody>
</table>