Novel Epitaxial Nanostructures for the Improvement of InGaN LEDs Efficiency

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Abstract—We demonstrated that the efficiency of an InGaN LED can be improved by using a novel epitaxial nanostructure, namely, the nanostructured semipolar (N SSP) gallium nitride (GaN). The NSSP GaN template was fabricated on a c-plane GaN surface using a standard GaN metal-organic chemical vapor deposition tool on c-plane sapphire substrates. We showed that the surface of NSSP GaN consisted of two semipolar orientations: (10–11) and (11–22). InGaN/GaN multiple quantum wells (MQWs) fabricated on NSSP GaN exhibited negligible quantum-confined Stark effect (QCSE) and a 30% improvement in internal quantum efficiency as compared to planar c-plane InGaN/GaN MQWs. Using time-resolved photoluminescence (PL), a considerable improvement in radiative recombination lifetime was also observed. We fabricated and characterized semipolar InGaN LEDs on NSSP GaN that emitted at 543 nm and showed negligible QCSE. The NSSP GaN structure can also be applied to improve the photon extraction efficiency of InGaN-based LEDs. The surface texturing was performed in situ together with the LED epitaxy without additional ex situ etching processes. The in situ surface texturing improved the PL intensity by a factor of two. An electrical injection LED structure employing in situ surface texturing was also demonstrated.

Index Terms—Light-emitting diodes, nanotechnology, quantum-confined Stark effect, semiconductor epitaxial layers.

I. INTRODUCTION

C OST-EFFECTIVE solid-state lighting (SSL) requires high efficiency visible (white) light emitters operating at high injection current over a wide temperature range. Among the highest efficiency solid-state light emitters achieved to date, InGaN-based light-emitting diodes (LEDs) emitting in the blue/green/yellow wavelength range and AlGaN-based LEDs emitting in the orange/red wavelength range are promising candidates in realizing the next-generation SSL technology. Despite recent advances in blue InGaN LEDs, efficiency droop at high operating current and low internal quantum efficiency (IQE) in the green/yellow (G/Y) wavelength range still prevent the SSL technology from becoming truly cost-competitive to state-of-the-art fluorescence lamps [1]. It has been found that a strong internal electric field (IEF) that exists in InGaN LEDs grown on polar (c-plane) GaN surfaces can directly or indirectly lead to the lowering of IQE [2]–[4] and induce efficiency droop at high operating current [4]–[6]. The IEF originates from spontaneous and strain-induced piezoelectric polarization charges that are strongly dependent on the crystal orientation of epitaxial heterostructures in InGaN LEDs [2]. The IEF can separate the electrons from holes and increase electron leakage, which results in low IQE and efficiency droop, respectively. The suppression of the IEF, which is expected to increase the IQE and the current density at which efficiency droop occurs, can be achieved by reducing the lattice mismatch in heterostructures or growing them on semipolar (e.g., (10–11) and (11–22)) and nonpolar (e.g., a-plane and m-plane) surfaces. In this paper, we will investigate novel epitaxial nanostructures on c-plane GaN for the reduction of IEF, and hence the improvement of efficiency in InGaN LEDs.

At least three approaches to fabricating semipolar InGaN LEDs have been reported to date. These include the growth of GaN on spinel substrates [7], on bulk GaN substrates [8]–[10], and on the sidewalls of pyramidal or ridge GaN structures created on planar polar GaN surfaces using selective area epitaxy (SAE) [11]–[14]. GaN grown on spinel substrates has so far exhibited a high density of threading dislocations and stacking faults, thereby compromising the potential improvement of efficiency from the lowering of the IEF. The use of bulk semipolar GaN substrates has demonstrated the advantage of a lower IEF on the enhanced efficiency of green and yellow LEDs [8], [9]. However, issues such as high wafer cost and small substrate size need to be resolved before this approach can become more practical. On the other hand, the SAE technique can create semipolar planes on polar GaN surfaces. High-quality polar GaN films have been fabricated from a variety of substrates including sapphire, 6H-SiC, and bulk GaN by metal-organic chemical vapor deposition (MOCVD). Using growth rate anisotropy and 3-D growth, different semipolar and nonpolar GaN planes can be generated on c-plane GaN [15]. It has been shown that high-quality InGaN multiple quantum wells (MQWs) that exhibit IQE as large as a factor of three compared to polar MQWs can be grown on pyramidal GaN microstructures [11]. This approach, however, requires ex situ patterning and can not easily produce a planar structure for electrical contacts. In this paper, a new semipolar LED structure is investigated, which is enabled by a novel epitaxial nanostructure, namely the nanostructured semipolar (N SSP) GaN, which can be fabricated directly on c-plane GaN but without the issues of the SAE technique mentioned above [16]. NSSP GaN also eliminates the issues of excessive defects on spinel substrates and lowers the cost of using bulk semipolar GaN substrates. The surface of NSSP GaN consists of two different semipolar planes: (10–11) and (11–22). Previously, we have shown that blue-emitting InGaN MQWs
grown on NSSP GaN exhibited negligible quantum-confined Stark effect (QCSE), which was attributed to the suppression of the IEF [16]. In this paper, we will demonstrate that a G/Y semipolar InGaN LED with negligible QCSE can be achieved on NSSP GaN. In addition, we will show that these nanostructures can provide a cost-effective approach to improving the extraction efficiency of InGaN LEDs.

The organization of this paper is as follows. In Section II, we will describe the experimental procedure to create NSSP GaN and its characterizations. In Section III, we will describe the fabrication and characterization of semipolar InGaN LEDs emitting at 543 nm on NSSP GaN. In Section IV, we will investigate how NSSP GaN structures can be applied to improve the extraction efficiency of InGaN LEDs. In Section V, we will conclude and discuss ongoing challenges in the application of NSSP InGaN LEDs in solid-state lighting.

II. NSSP GaN Using In Situ Processing

The detailed experimental procedure and conditions to fabricate an NSSP GaN template have been reported previously in Ref. [16]. Fig. 1 illustrates this procedure that consists of two separate steps, both of which were performed in situ in MOCVD (Thomas-Swan CCS 3 × 2) on c-plane sapphire substrates: 1) the creation of nanoscale truncated cone structures on c-plane GaN surface using in situ silane treatment (ISST) as shown in Fig. 1(b) and 2) the reshaping of truncated cone structures into NSSP surfaces using high-temperature treatment (HTT) as shown in Fig. 1(c). Also shown in Fig. 1 are the deposition of InGaN/GaN MQWs [Fig. 1(d)] and the planarization of the device surface [Fig. 1(e)]. The duration of the combined ISST and HTT processes is typically 15–25 min and use only standard gas sources found in GaN MOCVD tools. No ex situ patterning is required that greatly reduces the complexity and cost of the process. In addition, the NSSP GaN surface is continuous that makes the subsequent LED growth and processing compatible with the state-of-the-art technology.

A. In Situ Silane Treatment Process

The ISST process transforms a planar c-plane GaN surface into a nanoscale-textured surface. The surface morphology evolved with the duration of ISST as shown by a series of scanning electron micrographs (FEI Nova Nanolab) in Fig. 2(a)–(e). To quantify the morphological evolution, we also plot the root mean square (rms) roughness of the as-treated sample versus the ISST time measured by atomic force microscopy (AFM; Digital Instruments Nanoscope) in Fig. 2(f). The rms roughness increased initially with the ISST time and peaked at around 5 min before decreasing after that. This trend was attributed to the coalescence of adjacent islands after 5 min of ISST as shown in Fig. 2(d)–(e).

The mechanism underlying the ISST process is not yet clear. Two different models have been proposed for a short ISST process, typically less than 1 min. In [17]–[19], it was suggested that during the ISST process, a porous monolayer of SiN was deposited on the GaN surface. In [20], it was suggested that the surface of the GaN was etched by silane under an ammonia environment. In both models, the reduction of the threading dislocation (TD) density was observed in a GaN overlayer grown after the ISST process. To confirm whether a long ISST process (e.g., 5-min ISST treatment) could also result in a reduction of the TD density, a thick GaN layer was overgrown on an ISST-treated GaN surface. The TD density was measured by cross-sectional transmission electron microscopy (TEM; JEOL 2010F) and nearly an order of magnitude TD density reduction was observed as shown in Fig. 3.

Our characterizations so far have suggested that the ISST process was the result of the interaction between the silane gas and the TDs under an ammonia environment. In our experiment,
Fig. 2. SEM images showing the surface morphology of ISST-treated samples with ISST treatment times varying from (a) 0 sec, (b) 60 sec, (c) 150 sec, (d) 300 sec, to (e) 600 sec. The RMS surface roughness measured by AFM is shown in (f) versus the ISST time.

we observed the formation of nanoscale pits on the surfaces of samples undergone 1 min of ISST as shown in Fig. 2(b). The density of the pits was measured to be $8 \times 10^{8} \text{cm}^{-2}$, which corresponded to the intersection of TDs with the GaN surface. These pits evolved into nanoscale structures with an increasing ISST time. If the SiN$_x$ model were correct, the level of surface roughness we observed in Fig. 2(f) could only be attributed to thermal etching of the uncovered GaN surface [21]. However, in a control experiment in which the same ISST process was performed for 5 min except with the silane gas turned off, we observed, using AFM, a smooth sample surface with rms roughness comparable to an untreated GaN template. On the other hand, an ISST-treated sample measured by X-ray photoelectron spectroscopy (Kratos Axis Ultra) showed no SiN$_x$ trace. To further characterize the ISST mechanism, we are currently conducting cross-sectional scanning TEM measurement with electron energy loss spectroscopy. The details of these studies will be reported elsewhere.

B. High-Temperature Treatment Process

The HTT process reshapes the truncated cone structures into nanoscale pyramidal-like structures bounded by semipolar facets. The HTT process was performed at a temperature $\sim 70 ^\circ C$ higher than the typical GaN growth temperature for around 10 min. At a higher growth temperature, slowest growing planes emerge after the HTT process as shown in Fig. 1(c). We have measured the crystal orientation of the sample surface after the combined ISST and HTT processes using TEM and found two different semipolar planes including (10–11) and (11–22) planes. According to [2], typical blue and G/Y InGaN MQWs grown on these planes can exhibit more than 85% suppression of the IEF compared to MQWs grown on polar GaN.

C. Epitaxial Growth on NSSP GaN Templates

After the formation of an NSSP GaN template, InGaN MQWs can be deposited using similar growth conditions as on the planar polar GaN template. Although the MQWs growth was performed on a nonplanar surface, both InGaN quantum wells (QW) as indicated by the white arrows in Fig. 1(d) and GaN barriers are quite uniform in thickness.

We have also demonstrated that it was possible to planarize the surface of NSSP GaN devices. This makes the fabrication of InGaN LEDs grown on NSSP GaN, as will be discussed in Section III, directly compatible with the existing processing technology. The planarization mechanism is similar to the epitaxial lateral overgrowth in III-nitride materials [15]. As shown in Fig. 1(e), a 200 nm of p-type GaN layer was overgrown on the nanostructured InGaN MQWs at 1000$^\circ C$. The surface morphology measured by SEM was similar to the planar starting surface as shown in Fig. 1(a).

III. GREEN InGaN LEDs Fabricated on NSSP GaN

In this Section, we investigate the electrical injection InGaN LED structure based on an NSSP GaN template. The procedure of the epitaxial growth of the NSSP LED is shown in Fig. 1. To demonstrate the principle, we grew three pairs of InGaN/GaN MQWs on the NSSP surface followed by 230 nm of Mg-doped p-type GaN. After the formation of the NSSP surface, the substrate temperature was lowered to 760$^\circ C$ for the growth of MQWs, using a nitrogen carrier gas at a 400 mTorr reactor pressure. Subsequently, the growth temperature was raised again to 1000$^\circ C$ for the p-GaN growth. The growth conditions used for all layers were very similar to those used in a planar LED device except for the addition of ISST and HTT processes. The entire epitaxial sequence was performed in one shot starting from a c-plane sapphire substrate. No electron blocking layer was included to allow us to focus on the optical and electrical properties of the nanostructured active region.

We fabricated the NSSP LED using a simple top-emitting mesa structure. The mesa area was 350 by 350 $\mu$m and was defined by a conventional photolithography and reactive ion
etching (RIE; Lam 9400). A thin metal film consisting of 5 nm of Ni and 5 nm of Au was deposited across the entire mesa as the transparent electrode. Three hundred seventy nanometer of Au and 380 nm of Ti/Au were deposited by the e-beam evaporator as the p-type and n-type Ohmic contacts, respectively. The LEDs were characterized by standard electroluminescence (EL) measurements at room temperature with no intentional cooling applied.

The EL spectra under a range of continuous-wave (CW) current injection are shown in Fig. 4(a). The peak wavelength was around 543 nm and did not show any blueshift with increasing current. Instead, the peak wavelength showed a slight redshift (<2 nm across the measurement range) possibly due to joule heating as shown in Fig. 4(b). The absence of QCSE in the measurement range was attributed to the suppression of IEF in semipolar MQWs and agreed well with our previous results on the photoluminescence (PL) characterization of blue-emitting NSSP MQWs [16], [22]. The full-width-half-maximum (FWHM) EL linewidth increased slightly with increasing injection and was comparable to semipolar G/Y LEDs grown on semipolar bulk GaN substrates [8], [9].

The $I-V$ and $L-I$ characteristics of the NSSP LED are shown in Fig. 4(c). The turn-on voltage was 4.2 V at 20 mA. We attributed the high operating voltage to the unoptimized growth conditions of the NSSP template and the p-GaN current spreading layer. In addition, we observed roughly 300 microscale pits on the surface of each LED device. These microscale pits could be resulted from the interplay between TDs and the ISST process and could degrade the electrical properties. We expect to reduce the impact of these pits by optimizing the p-GaN layer thickness and planarization conditions.

To further characterize the optical properties of the NSSP active region, we have performed temperature-dependent PL [22] and time-resolved PL (TRPL), using the triple-frequency output of a mode-locked titanium-sapphire laser (Spectra-Physics Tsunami). We compared the results from the NSSP MQWs sample with those from a polar MQWs sample grown under the same conditions. In contrast to the electrical injection NSSP LED sample mentioned above, the sample used in the TRPL investigation had no p-type GaN layer. The excitation wavelength was centered at 260 nm with a 130 fs pulse width and a repetition rate of 80 MHz. The average laser intensity at the sample surface was estimated to be 1 kW/cm². The room-temperature TRPL signal as shown in Fig. 5 was dispersed through a 0.5 m monochromater and was recorded by a silicon-based single photon detector (id Quantique id-100) with a timing resolution of 50 ps. The monochrometer grating was tuned to the peak wavelength of the MQWs. To extract the radiative and nonradiative lifetimes, we use the following relationships: $1/\tau_{PL} = 1/\tau_r + 1/\tau_{nr}$ and

$$\eta_{int} = 1/(1 + \tau_e/\tau_{nr})$$

where $\tau_{PL}$, $\tau_r$, and $\tau_{nr}$ are the TRPL, radiative, and nonradiative lifetimes, respectively; $\eta_{int}$ is the internal quantum efficiency (IQE), which was obtained from the
temperature-dependent PL measurement by assuming that $\eta_{\text{int}}$ was 100% at low temperature (10 K) [22]. The results are summarized in Table I. It can be seen that although the radiative lifetime was reduced considerably in the NSSP sample due to the absence of QCSE, the nonradiative lifetime was also reduced. This explains why only a 30% improvement in IQE was observed in the NSSP sample while a factor of three improvement in IQE was previously measured in semipolar InGaN/GaN MQWs grown on pyramidal GaN surfaces using SAE [11]. The physical mechanism of the decreased nonradiative lifetime is still under investigation. However, preliminary low-temperature PL results suggested that it was related to the generation of gallium vacancies during the ISST process. Because gallium vacancies (point defects) were not present in the InGaN MQWs, we believe by optimizing the HTT conditions after the ISST process and therefore annealing the defects, the nonradiative recombination could be minimized.

IV. IMPROVEMENT OF PHOTON EXTRACTION

In this Section, we will show that the NSSP GaN structures can also be applied to the surface of an InGaN LED to improve photon extraction from the active region. It is known that the total internal reflection (TIR) at the smooth LED surface is the major limiting factor to LED extraction efficiency [23]. Surface texturing of LEDs has proven to be effective in improving the extraction efficiency. Approaches to texturing the surface include the introduction of photonic crystal structures [24], [25] and random nanostructures on nitrogen-polar GaN surfaces using photoelectrochemical (PEC) etching [26]. Both approaches require ex situ processes that add costs and additional demands on resources. On the other hand, the NSSP GaN structures discussed in this paper can be formed in situ in standard GaN MOCVD tools. As shown in Fig. 1, the formation consists of the ISST and HTT processes. In the following, we will show that the ISST process alone is sufficient to generate suitable surface texturing for the improvement of InGaN LED extraction efficiency.

To characterize the extraction efficiency, we compared two samples with complete LED structures grown back-to-back on c-plane sapphire substrates under the same conditions. A 5-min ISST process was added at the end of the epitaxial process for one sample while the other sample was left untreated. The active regions for both samples consisted of three pairs of InGaN/GaN MQWs. In both samples, there were 150 nm of GaN overlayers on top of the active regions. We performed room-temperature PL measurements on both samples under the same excitation conditions. The excitation was generated from a CW He-Cd laser at 325 nm wavelength. The excitation intensity was estimated to be 300 W/cm$^2$ at the sample surfaces.

The comparison of the PL results for both ISST-treated and untreated samples is shown in Fig. 6(a). The peak wavelengths for both samples were around 458 nm. The PL intensity of the ISST-treated sample was measured to be a factor of two compared to that of the untreated sample. This enhancement was attributed to the reduction of TIR at the sample surface due to surface texturing. It was further confirmed by the disappearance

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<th>TABLE I</th>
<th>SUMMARY OF TIME-RESOLVED PHOTOLUMINESCENCE RESULTS</th>
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<td>NSSP MQWs</td>
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<tr>
<td>$\eta_{\text{int}}$</td>
<td>21 %</td>
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<tr>
<td>$\tau_{\text{PL}}$</td>
<td>0.16 ns</td>
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<tr>
<td>$\tau_{r}$</td>
<td>0.76 ns</td>
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<td>$\tau_{nr}$</td>
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Fig. 6. Characterization results of an InGaN LED with its surface treated by the ISST process for 5 min: (a) PL spectrum compared to that of an untreated sample is shown. Both GaN and InGaN (∼458 nm) peaks are shown; (b) Electroluminescence spectra; (c) $L$-I and $I$-$V$ curves.
of interference fringes that were observed in the untreated sample. The fringes originated from multiple reflections between sapphire/GaN and GaN/air interfaces [26]. Surface texturing considerably reduced the reflection at the GaN/air interface and suppressed the interference fringes. Our results agreed with previous results obtained on roughened nitrogen-polar GaN surfaces using PEC etching [26].

One might think improving the extraction efficiency using the ISST process is not feasible in making electrical injection LEDs due to the unpatterned roughened surface. To this end, we fabricated current injection LED devices incorporating the ISST process as described above. The LED structure had a 180 nm of p-GaN grown at 1000 °C. We performed the ISST process immediately after the p-GaN growth for 5 min at 1000 °C. The as-grown sample was observed under SEM and similar surface morphology as in Fig. 1 was found despite a 30 °C lower ISST temperature. We used the same top-emitting LED structure as described in the previous section.

The measured EL spectra are shown in Fig. 6(b) under CW current injection. In contrast to the PL results, we noticed the existence of fringes in the EL spectra. We attributed these fringes to the reflection from the interface between the p-GaN and the n-type transparent electrode. Both the J-V and L-f characteristics are shown in Fig. 6(c). The turn-on voltage was measured to be 3.9 V at 20 mA. This was attributed partially to the high contact resistance at the textured surface. Further optimization of device structures and metal interface is still required. Due to the unoptimized electrical properties, we were not able to directly compare the external quantum efficiency of the ISST-treated LED and the planar LED so far.

V. CONCLUSION

In summary, we have experimentally demonstrated a novel cost-effective epitaxial nanostructure, namely the NSSP GaN, which can be inserted into conventional InGaN-based LEDs to improve both the internal quantum efficiency and the extraction efficiency. The NSSP GaN can be formed in situ in standard GaN MOCVD tools on c-plane GaN templates that can be fabricated on a variety of substrates including low-cost sapphire and large-area silicon substrates. The formation of NSSP GaN consists of two steps, the ISST and HTT processes. No ex situ patterning is required. The resulting NSSP GaN surface consists of two semipolar planes: (10–11) and (11–22). InGaN/GaN MQWs have been deposited directly on the NSSP GaN surface and shown to exhibit negligible QCSE.

Using NSSP GaN templates, we fabricated and characterized semipolar InGaN LEDs. Both photoluminescence and electroluminescence measurements were performed. Even without intentional cooling, the NSSP LED showed negligible QCSE and comparable FWHM linewidths as compared to those fabricated on bulk semipolar GaN substrates. Time-resolved photoluminescence confirmed a considerable reduction of the radiative recombination lifetime in the NSSP LED. A 30% improvement in internal quantum efficiency was also measured in the NSSP MQWs as compared to the polished MQWs.

In addition, the ISST process was shown to be able to improve the extraction efficiency of InGaN LEDs by creating surface texturing to suppress the total internal reflection. A factor of two improvement in photoluminescence intensity was observed from the ISST-treated LED structure as compared to an untreated one. Electroluminescence was also demonstrated by directly depositing p-type electrode on the roughened surface.

The electrical characteristics of InGaN LEDs fabricated so far, which incorporate NSSP GaN structures, still exhibited high turn-on voltages as compared to typical planar LEDs. This was attributed to the unoptimized formation process of the NSSP GaN. For NSSP InGaN LEDs to be successfully applied to the next-generation solid-state lighting, we must further optimize the growth conditions for ISST, HTT, and the subsequent p-GaN planarization processes.

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