Study and Simulation of CMOS *LC* Oscillator Phase Noise and Jitter

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ABSTRACT

In this work we review the processes of phase noise and jitter in electronic oscillators and the relationship between the two. Frequency and time domain simulation techniques and results are presented through the study of performance enhancement for a CMOS LC oscillator. The studied enhancements significantly reduce flicker noise upconversion, while the results demonstrate good agreement between time and frequency domain design approaches.

1. Introduction

Periodic oscillators perform a vital function in integrated circuits ranging from RF systems to microprocessors. In RF systems, these signals provide functionality for frequency translation and filtering, while in synchronous digital systems, clock signals pace all functions including capturing data, reading memory, and synchronizing communications. The relative stability of these signals is of particular interest when designing such systems. Frequency instability can lead to serious performance degradation such as intermodulation distortion and logic timing errors in RF and digital systems respectively. The metrics commonly employed to describe this instability are phase noise and jitter.

Much RF work to date has focused on frequency domain simulation of phase noise, while in most digital systems jitter is the metric employed. As integrated circuits migrate toward mixed-signal operation, time and frequency domain metrics overlap. Thus, it is important to be able to design and simulate systems with the noise mechanisms that contribute to instability in both domains. Moreover, a fundamental understanding of the relationship between the two domains is mandatory in order to specify and develop subsystems that are mixed-signal in nature. Here we present a review of these concepts while demonstrating techniques for frequency stability enhancement in a CMOS *LC* oscillator.

2. Phase Noise and Jitter in Oscillators

Phase noise and jitter are metrics that quantify the frequency stability of a periodic signal. Phase noise defines the noise power spectrum, *P*, around the fundamental frequency as shown in Fig. 1. In the ideal case, the spectrum is a Dirac-delta function at the fundamental output frequency f_o. Practically, due to device noise, the oscillator output spectrum exhibits noise power around the fundamental frequency.

Jitter metrics quantify the time domain uncertainty in the oscillator period. Ideally, edges of the oscillator signal occur at identical intervals in time as shown by the voltage waveform in Fig. 2. In practical circuits, the edges of the signal deviate from this ideal position in time by some amount each cycle.

2.1 Phase Noise

Consider the ideal voltage output, $v_o(t)$, of an autonomous oscillator as a function of time, *t*. This signal can be expressed as,

$$v_o(t) = V_o \cos(\omega_o t) \tag{1}$$

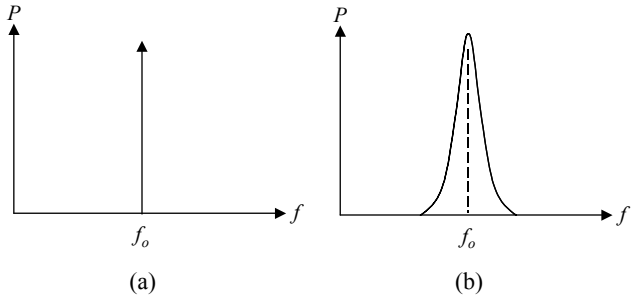

Figure 1. Output spectrum (a) ideal (b) with phase noise

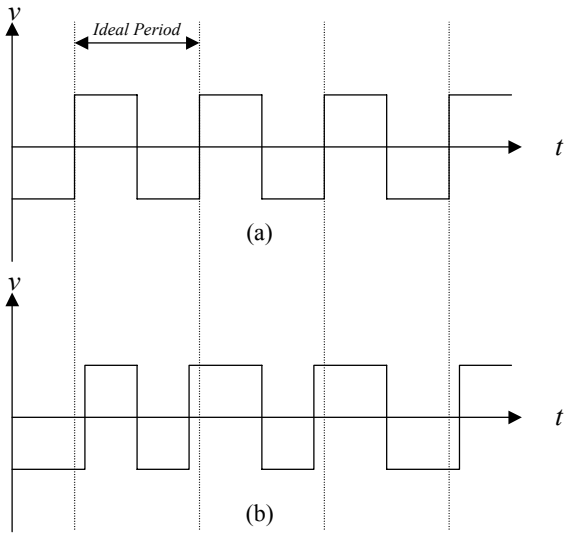

Figure 2. Time domain output (a) ideal (b) with jitter

where ω_o is the fundamental radian frequency, and V_o is the nominal voltage amplitude. The output of the same oscillator, under the influence of noise processes, can then be described by,

$$v_n(t) = (V_o + \varepsilon(t))\cos(\omega_o t + \phi(t)) \tag{2}$$

where $\varepsilon(t)$ and $\phi(t)$ are, in general, zero-mean stochastic processes. Typically, fluctuations in the amplitude of the oscillator signal are ignored as they can be eliminated with the introduction of a limiter. Therefore, $\phi(t)$ is the only process of concern when considering phase noise and jitter. The power spectral density of $\phi(t)$, $S_\phi(f)$, describes the frequency domain noise power of this process. However, in practice the voltage power spectral density, $S_v(f)$, is typically measured with a spectrum analyzer. Then the single sideband phase noise spectral density, $(N_o/P_o)_{fm}$, is described as the noise power relative to the fundamental power, P_o, at frequency, f_o, for

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some offset, f_m.

$$\left(\frac{N_o}{P_o}\right)_{fm} = \frac{S_v(f_c + f_m)}{P_o} \quad (3)$$

In [1] it has been shown that the phase noise spectral density for an autonomous oscillator with white noise sources can be described by the Lorentzian function as follows,

$$\left(\frac{N_o}{P_o}\right)_{fm} = \frac{1}{2}\frac{f_o^2 a}{\pi^2 f_o^4 a^2 + f_m^2} \quad (4)$$

where a is a constant. The corner frequency of this function is given by:

$$f_{corner} = \pi a f_o^2 \quad (5)$$

Using (4), in [2] it has been shown that $S_\phi(f)$ can be related to the phase noise density at frequencies above f_{corner} by,

$$\left(\frac{N_o}{P_o}\right)_{fm} = \frac{a f_o^2}{2 f_m^2} = \frac{1}{2} S_\phi(f_m) \quad (6)$$

It is imperative to note that throughout the derivation of this expression in [2], the noise process, $\phi(t)$, is assumed to be a white, zero-mean, Gaussian process. Thus, device flicker noise is not considered. Although this function describes the behavior of phase noise well for offset frequencies where white of frequency phase noise is observed, it does not describe phase noise that arises from flicker noise sources.

In [3], an analytical model including flicker noise has been developed. Specifically, this model utilizes the Lorentzian function for the device white noise sources and the Gaussian function for the device flicker noise sources. The final spectral representation is found from the convolution of the two functions. The result is the Voight line profile for which there is no analytical expression and results must be obtained numerically.

2.2 Jitter

The three most commonly employed timing jitter metrics for autonomous oscillators include long-term, period, and cycle-to-cycle jitter. All three metrics quantify the uncertainty in the oscillator period. Consider $v_o(t)$ again and define the fundamental oscillation period as $T = 2\pi/\omega_o$. Next, consider the noisy signal, $v_n(t)$. Define the absolute instant in time of the k-th positive voltage transition of $v_n(t)$ as t_k and the period of the k-th cycle as T_k. The expected value of the discrete random sequence T_k is $E[T_k] = T$ and $T_k = t_{k+1} - t_k$.

The long-term, or n-cycle, jitter is defined as,

$$J_n(k) = \sqrt{var(t_{k+n} - t_k)} \quad (7)$$

This metric measures the variation of the signal edges across n-cycles. The period jitter, J, is simply a specialized case of the long-term jitter, where $n = 1$ as given by,

$$J_1(k) = \sqrt{var(t_{k+1} - t_k)} = \sqrt{var(T_k)} = J \quad (8)$$

and clearly J is simply the standard deviation of a single period.

Lastly, cycle-to-cycle jitter measures the variation between adjacent periods as given by,

$$J_{cc}(k) = \sqrt{var(T_{k+1} - T_k)} \quad (9)$$

It has been shown in [2] that if the oscillator exhibits simple accumulating jitter, then these metrics can be related by,

$$J_n = \sqrt{n} J \quad (10)$$

and,

$$J_{cc} = \sqrt{2} J \quad (11)$$

The period jitter is of most interest in the design of oscillators as it characterizes the short-term variation in each period from the mean. This metric is utilized in a variety of time domain specifications, including timing budgets for microprocessors. Moreover, the period jitter can be determined from the phase noise spectral density as will be shown next.

2.3 Relationship Between Phase Noise and Jitter

In [2] it has been shown that the period jitter, J, can be expressed as,

$$J = \sqrt{aT} \quad (12)$$

where a is the constant associated with the Lorentzian function given in (4). Using (6), it is trivial to show that,

$$a = 2\frac{f_m^2}{f_o^2}\left(\frac{N_o}{P_o}\right)_{fm} \quad (13)$$

and thus the single sideband phase noise spectral density can be related to the period jitter by the following expression:

$$J = \sqrt{2\frac{f_m^2}{f_o^3}\left(\frac{N_o}{P_o}\right)_{fm}} \quad (14)$$

However, this relationship has been derived in the absence of device flicker noise and thus all noise sources in the circuit are assumed to be white. Nevertheless, this expression is reasonably accurate for period jitter calculations as will be shown. The expression is employed by selecting a frequency at which the phase noise density is measured that is well above the corner frequency of the Lorentzian function (5) and well below f_o.

Expressions have been presented in previous work [4] to calculate long-term jitter in the presence of flicker noise. These expressions will not be addressed here as period jitter is of primary interest in this work.

3. Oscillator Topology and Design

In this work we have designed and enhanced the differential cross-coupled CMOS *LC* oscillator, shown in Fig. 3 with f_o = 1.865GHz, in order to study the phase noise and jitter performance. The tank is modeled with parasitic components that were extracted from simulation of the inductor and capacitor structures. Specifically, the *LC*-tank performance includes an inductor with a device Q of 17 and a capacitor with a device Q of 50. The unloaded tank Q is approximately 13. The configuration is a negative resistance cross-coupled differential pair. The design has been completed to realize a loop gain of at least 5 and a quiescent current that will allow the tank to maintain voltages on the edge of the current limited regime, as explained in [5]. The doubly balanced configuration was selected to promote waveform symmetry in the output signal, thus reducing the likelihood of the rising and falling edges being dissimilar. In [6], it

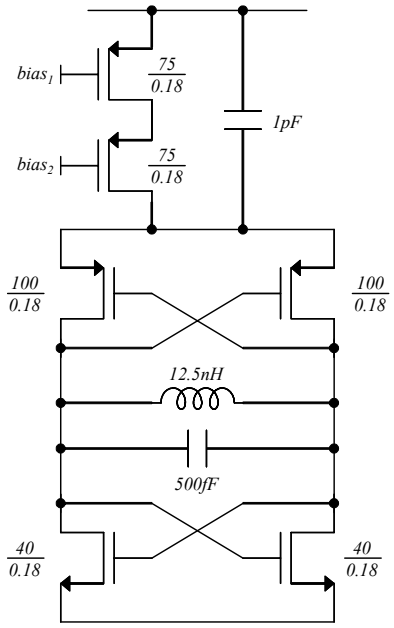

Figure 3. CMOS *LC* oscillator with noise reduction enhancements

has been shown that waveform symmetry can attenuate flicker noise upconversion from the tail current source. The circuit of Fig. 3 was designed using the *BSIM*3v3.2 RF noise parameters for the 0.18µm mixed-mode process available from *Taiwan Semiconductor Manufacturing Company.* Both flicker and thermal noise were modeled using the *BSIM* and *SPICE* noise models respectively.

4. Performance Enhancement Techniques

The phase noise density expression for a generic *LC* oscillator is described by the classic Leeson model,

$$L(f_m) = \frac{1}{8Q^2}\frac{FkT}{C}\left(\frac{f_o}{f_m}\right)^2 \qquad (15)$$

where F is the circuit noise factor, k is Boltzman's constant, T is temperature, C is the oscillator output power, Q is the tank quality factor, f_o is the oscillator fundamental frequency, and f_m is the frequency offset from the fundamental.

The most obvious performance enhancements for frequency stability include increasing the quality factor of the tank, increasing the output power, and reducing the noise factor. Much literature has been published on high Q-factor tanks, and optimization of this parameter is well worth the effort given the quadratic improvement in performance. Increasing the power is typically not desirable, so power is often a key constraint.

Improving the noise factor is another endeavor. The most significant contribution to phase noise and jitter in CMOS electronics is device flicker noise. Specifically, low frequency device flicker noise from the tail current source is modulated and upconverted around the oscillator fundamental frequency. In [7], the details of this process are described. Here we show improvement techniques that reduce the flicker noise upconversion from this source and improve the oscillator phase noise performance by elaborating on the techniques presented previously in [8].

4.1 PMOS vs. NMOS Tail Current Source

PMOS devices exhibit a flicker noise power spectral density that is as much as 10 times less than comparable NMOS devices [8]. Choosing the tail current source to be PMOS as opposed to NMOS will realize gains of approximately 10dB in terms of phase noise performance. In addition to the device polarity change, the tail current transistor can be sized longer and wider in order to reduce flicker noise.

4.2 Stabilizing the Common Mode Point

By stabilizing the common mode point around the tail current source, less flicker noise upconversion is introduced. We demonstrate this fact with two techniques. First, the common mode point can be stabilized by placing a capacitor across the tail current source. Second, using a cascode tail current source increases the output resistance of the bias network and stabilizes the common mode point.

4.3 Weak Inversion Tail Current Source

By placing the tail current source device on the edge of weak inversion, as opposed to strong inversion, flicker noise is reduced. Previous work has shown flicker noise power to be a function of gate voltage, where the input referred noise power decreases with decreasing gate voltage [9]. This is likely related to an increase in gate oxide trap density with increased gate voltage. However, the *BSIM* noise model supports only flicker noise dependence on gate voltage and not oxide trap density dependence. This should be considered when examining results.

5. Simulation Environments and Results

We have employed two CAD environments to perform phase noise and jitter simulations. In this work, we demonstrate these environments for each proposed enhancement incrementally and a comparison between the results from the two simulation domains is made.

We have utilized the *Cadence SpectreRF* environment to perform phase noise simulations. *SpectreRF* makes use of a periodic steady-state (PSS) analysis to determine the steady-state response of autonomous circuits. Once the PSS solution has been determined, the phase noise is computed through linearization of every time step in the period. Noise is accumulated from all sources, and over every time point as described in [10]. This environment supports nonlinear modeling of the noise processes, including flicker noise upconversion.

Results from the phase noise simulations are found in Fig. 4. Here we observe upconverted flicker noise close to the fundamental. The corner frequency is near 1MHz for the PMOS configurations. The NMOS configuration exhibits substantially more flicker noise upconversion and it is observed over a much wider bandwidth. A gain of over 10dB is achieved in the device polarity change from NMOS to PMOS. The other enhancements show gains from 1.7dB to 3.4dB each. The proposed enhancements show an overall improvement of almost 20dB as compared to the baseline configuration.

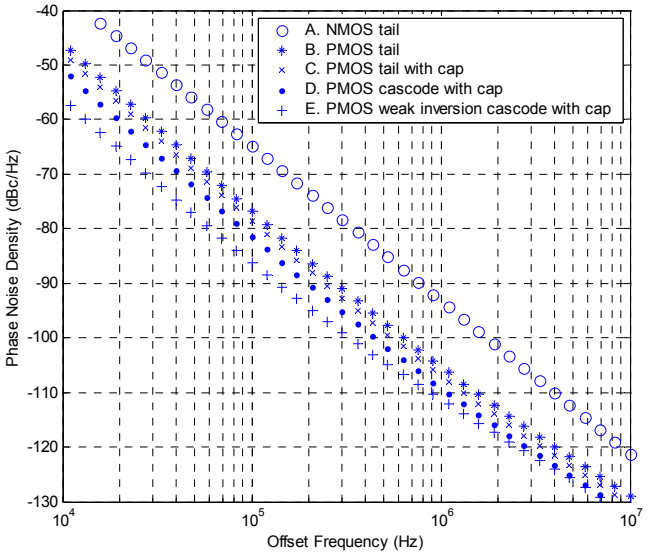

Figure 4. Phase noise spectral density results for each topology

The *Agilent ADS* environment supports time-domain noise simulations that include device flicker noise. We have employed this environment to perform long time domain transient simulations and calculate the period jitter through statistical analysis. First each cycle period, T_k, was determined and the period jitter was calculated from (8). It was expected that the jitter process would exhibit a zero mean Gaussian distribution. In Fig. 5, the period offset distribution is illustrated and this expectation is confirmed.

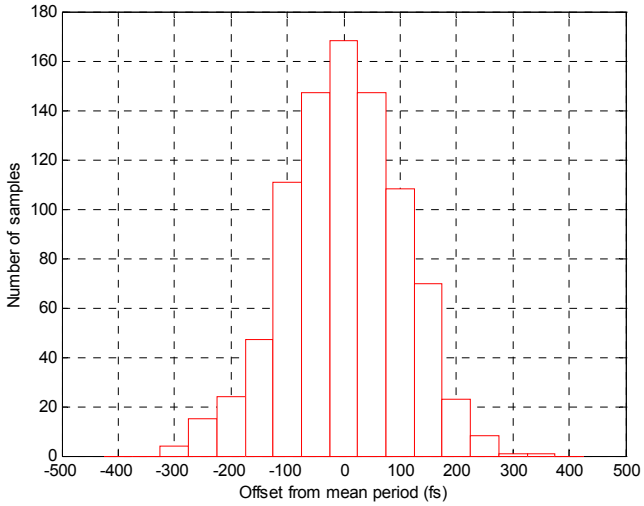

Figure 5. Calculated deviation from mean period for topology C

Time domain simulations required significant time as well as data capacity. A maximum transient step size of 1/10th of the expected jitter was used to accurately determine the period jitter. In the simulation described previously, approximately 1,000 cycle periods were calculated after initial start-up. Over 10 hours were required to complete the simulation and over 250MB of data were recorded. In some design applications, such intensive simulations may not be practical, but in many circumstances, time domain analysis is the only option, particularly when periodic steady-state convergence cannot be achieved.

Using (14) the results of the phase noise simulations were converted to period jitter. The time domain simulations were compared to calculations and good agreement was found, as illustrated in Table I. Variations were expected as the simulated jitter is only one realization of the sample function for the stochastic process, $\phi(t)$, and the acquired data have a finite sample size.

6. Conclusion

A review of phase noise, jitter, and the relationship between the two has been presented. Minimization of these processes was illustrated in the design and study of a CMOS *LC* oscillator where several performance enhancements were presented for the chosen topology. Two distinct simulation environments were employed to determine the phase noise and jitter performance. Phase noise results were utilized to calculate expected jitter and results were compared to statistics acquired from time domain noise simulations. Good agreement was shown between the two. Moreover, the proposed enhancements showed significant frequency stability improvement.

7. References

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Oscillator Topology	Phase Noise at 600kHz Offset (dBc/Hz)	Calculated Period Jitter from Phase Noise (fs)	Simulated Period Jitter (fs)
A. NMOS tail current	-86.9	481	515
B. PMOS tail current	-99.3	114	118
C. PMOS tail with capacitor	-101.0	94	93
D. PMOS cascode tail with capacitor	-102.8	76	83
E. PMOS weak inversion cascode tail with capacitor	-106.2	51	79

Table I: Summary of simulated and calculated phase noise and jitter for each oscillator configuration, f_o = 1.865GHz