TOP-DOWN AND BOTTOM-UP APPROACHES TO STABLE CLOCK SYNTHESIS

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ABSTRACT

In this work we present and study bottom-up, or multiplicative, clock synthesis and compare it to a proposed and alternative top-down, or divisive, methodology. The focus of the work is on the short-term stability for each approach and the implications associated with frequency multiplication and division. The analysis and simulation demonstrate that for a common application, a top-down clock synthesis approach achieves similar stability performance when compared to bottom-up synthesis, while also being substantially simpler to implement.

1. INTRODUCTION

Clock synthesis is typically achieved with a low-frequency off-chip quartz crystal reference oscillator along with an on-chip phase locked loop (PLL) or delay locked loop (DLL). The PLL or DLL generates the signals needed for the application through frequency multiplication. Often the multiplicative factor in systems such as these can be on the order of 50 or higher. Though this approach is ubiquitous in electronic systems today, a significant systemic drawback resides in the fact that the short-term frequency stability of the clock signal is degraded by frequency multiplication. Here an alternative approach to clock synthesis is proposed in which a stable high-frequency clock is generated, and the signal is then divided to lower frequencies for the application. With this approach, the short-term stability is actually enhanced by the same factor it is degraded in the previous traditional approach.

2. EFFECTS OF FREQUENCY DIVISION AND MULTIPLICATION ON FREQUENCY STABILITY

2.1. Short-Term Stability Metrics

The two most commonly employed metrics that describe the short-term frequency stability of periodic signals are phase noise and period jitter. Consider the ideal periodic voltage signal, $v_o(t)$, as a function of time, t. This signal can be expressed mathematically as follows,

$$v_o(t) = V_o \cos(\omega_o t) \tag{1}$$

where ω_o is the fundamental radian frequency and V_o is the nominal voltage amplitude. The same signal under the influence of phase noise can then be described by,

$$v_n(t) = V_o \cos(\omega_o t + \phi(t)) \tag{2}$$

where $\phi(t)$ represents the phase noise of the oscillator and is, in general, a zero-mean stochastic process.

Phase noise is a frequency domain metric that quantifies the noise power around the fundamental frequency. Ideally there is no noise power around the fundamental and the spectrum is a Dirac-delta function at ω_o. Practical periodic signals exhibit finite noise power around the fundamental which is quantified by the power spectral density of $\phi(t)$, $S_\phi(f)$. In practice the voltage power spectral density, $S_v(f)$, is typically measured with a spectrum analyzer. Then the single sideband (SSB) phase noise spectral density, $(N_o/P_o)_{fm}$, is described as the noise power relative to the fundamental power P_o, at frequency f_o, for some offset f_m as shown in (3).

$$\left(\frac{N_o}{P_o}\right)_{fm} = \frac{S_v(f_o + f_m)}{P_o} \tag{3}$$

Period jitter quantifies the time domain uncertainty in the period of an autonomous oscillator. Ideally, the edges of a periodic signal occur at identical intervals in time. In practical circuits, the edges of the signal are shifted from this ideal position by some amount each cycle. This type of jitter is referred to as accumulating jitter and is exhibited by autonomous, as opposed to driven, systems [1]. Consider $v_n(t)$ again and define the k-th positive voltage transition of $v_n(t)$ as t_k and the period of the k-th cycle as T_k. The period jitter, J, is given by,

$$J = \sqrt{var(t_{k+1} - t_k)} = \sqrt{var(T_k)} \tag{4}$$

and clearly J is simply the standard deviation of the period. As shown in [1] and [2], the phase noise induced period jitter can be related to the phase noise density by the following expression, using an appropriate offset frequency, f_m.

$$J = \sqrt{2\frac{f_m^2}{f_o^3}\left(\frac{N_o}{P_o}\right)_{fm}} \tag{5}$$

Equation (5) holds for periodic signals that exhibit simple accumulating jitter, which does not include flicker noise. Nevertheless, this conversion is reasonably accurate for CMOS electronics as shown in [2].

2.2. Frequency Multiplication and Division

Recall that phase and frequency are related by a linear operator and specifically frequency is the time differential of phase.

$$\omega = \frac{d\phi}{dt} \tag{6}$$

Therefore frequency multiplication will also result in phase multiplication. Consider the noisy periodic signal $v_n(t)$ again. If this signal is frequency multiplied by an integer N, the output signal is then described by,

$$v_{n,\,mult}(t) = V_o \cos(N\omega_o t + N\phi_n(t)) \tag{7}$$

where phase noise contributed by the multiplication circuitry has been ignored. Clearly the phase noise component of the signal has been increased by N. More

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importantly, though, by using the narrowband small angle modulation approximation, it can be shown that the phase noise power has increased by N^2 [3].

If the periodic signal, $v_n(t)$, is divided in frequency by an integer, N, then the signal becomes,

$$v_{n,\,div}(t) = V_o \cos\left(\frac{\omega_o t}{N} + \frac{\phi_n(t)}{N}\right) \tag{8}$$

where the phase noise contribution from the divider circuitry has been ignored. Also by the narrowband small angle modulation approximation, the phase noise is reduced by N and the noise power is reduced by N^2.

Interestingly, frequency division of a periodic signal causes the period jitter to increase. A divider circuit will output only one pulse for N input pulses and thus the variance of the output period is the sum of the variances of the N input periods. Since the period jitter is simply the standard deviation of the period, the jitter of a signal divided in frequency by N is given by,

$$J_{div} = \sqrt{N} J \tag{9}$$

where J is the period jitter before division. One can show the same result by using (5). A periodic signal divided in frequency by N will have a phase noise density that is reduced by N^2. Substituting yields,

$$J_{div} = \sqrt{2\,\frac{f_m^2}{(f_o/N)^3}\frac{1}{N^2}\left(\frac{N_o}{P_o}\right)_{fm}} = \sqrt{N} J \tag{10}$$

In contrast, multiplication reduces the period jitter by the same factor. This may seem, at first, counter intuitive since the phase noise spectral density is reduced substantially by division and increased substantially by multiplication. To clarify this relationship, consider the case of frequency division and the fact that although the period jitter has increased by $\sqrt{N}$, the period has also increased by N. Also, the relative period jitter, J_{ppm}, in parts per million (ppm) can be given by,

$$J_{ppm} = \frac{J}{T/10^6} \tag{11}$$

where T is the period. Thus the relative period jitter for a signal divided in frequency by N is given by,

$$J_{ppm,\,div} = \frac{\sqrt{N} J}{NT/10^6} = \frac{J_{ppm}}{\sqrt{N}} \tag{12}$$

and clearly the relative, or fractional, period jitter is reduced by frequency division. The relative period jitter is increased by the same factor in the case of frequency multiplication. Table 1 summarizes these relationships.

2.3. The Relationship with Quality Factor

The expression for the phase noise spectral density of a generalized resonant oscillator is described by the classic Leeson model,

$$\left(\frac{N_o}{P_o}\right)_{fm} = \frac{1}{8Q^2}\frac{FkT}{C}\left(\frac{f_o}{f_m}\right)^2 \tag{13}$$

where F is the circuit noise factor, k is Boltzmann's constant, T is temperature, C is the oscillator output power, Q is the resonant device quality factor, f_o is the oscillator fundamental frequency, and f_m is the frequency offset from the fundamental. Note that Q is also quadratically related to the phase noise power spectral density.

One could consider that frequency multiplication and division effectively degrade and enhance the quality factor of the reference oscillator respectively. Therefore it is possible that a very high-Q (Q_{mult}) reference oscillator that is multiplied in frequency by the factor N_{mult} and a very low-Q (Q_{div}) reference oscillator that is divided in frequency by the factor N_{div} may have the same short-term stability performance at the application frequency. Given that the phase noise spectral density is quadratic in both Q and frequency translation (N), one can determine the rough estimate that if $N_{div}N_{mult} > Q_{mult}/Q_{div}$, then the short-term stability of the divided signal will be comparable to that of the multiplied signal. Of course, this relationship ignores the noise contribution of additional circuit components and assumes that the noise factor and oscillator power are the same for both references, which may not be the case.

3. TOP-DOWN AND BOTTOM-UP SYNTHESIS

3.1. Bottom-Up

Bottom-up, or multiplicative, frequency synthesis is certainly the most common technique utilized for clock generation in electronic systems. Typically bottom-up synthesis is achieved with the use of a PLL or DLL. Fig. 1 illustrates the components of a simple PLL. The reference oscillator is compared against a frequency-divided image of the VCO output. The phase-frequency detector (PFD) drives a charge pump (CP) and a low pass filter (LPF) that sets the control voltage, v_{ctrl}, for the VCO. The PLL effec-

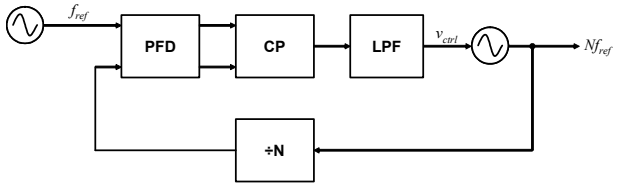

Figure 1. PLL-based bottom-up clock synthesis architecture.

Table 1. Summary of short-term frequency stability relationships for bottom-up and top-down frequency synthesis.

Variable/Metric	Reference Oscillator	Bottom-Up Synthesis	Top-Down Synthesis
Output Frequency (Hz)	f_{ref}	Nf_{ref}	f_{ref}/N
SSB Phase Noise Spectral Density (dBc/Hz)	$\left(\frac{N_o}{P_o}\right)_{fm}$	$\left(\frac{N_o}{P_o}\right)_{fm} + 20\log N$	$\left(\frac{N_o}{P_o}\right)_{fm} - 20\log N$
Period Jitter (s)	J	$J/\sqrt{N}$	$\sqrt{N}J$
Relative Period Jitter (ppm)	J_{ppm}	$J_{ppm}\sqrt{N}$	$J_{ppm}/\sqrt{N}$

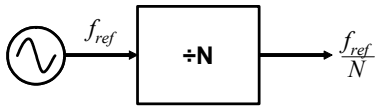

Figure 2. Simple top-down clock synthesis architecture.

tively multiplies the reference oscillator frequency, f_{ref}, to Nf_{ref}. Often f_{ref} is very low since low-frequency crystals are inexpensive and the reference oscillator can be realized with very low power dissipation.

Systems such as these are relatively straight-forward to develop and are capable of synthesizing a wide variety of frequencies. Fractional frequency multiplication can be achieved with the addition of some digital circuitry.

The drawbacks associated with PLL and DLL systems include the accumulated frequency instability and the number of components required for system implementation, which ultimately translates into power dissipation and silicon area.

3.2. Top-Down

An alternative approach to clock generation is to directly synthesize the desired frequencies by division of a stable high-frequency reference. This architecture, shown in Fig. 2, is significantly simpler than the traditional architecture shown in Fig. 1. Additional electronics would be required for fractional-*N* synthesis.

The most formidable challenge associated with a top-down approach is that the reference oscillator must be both highly stable and accurate. If such a reference could be realized, the system could be developed in monolithic form requiring no external components.

4. APPLICATION, DESIGN, AND SIMULATION

As a benchmark for analysis we have selected a common application for clock synthesis–*Intel*'s SA-1110 microprocessor. The processor runs up to 200MHz from a 3.6864MHz crystal reference oscillator. An on-chip PLL is utilized to frequency multiply the reference signal [4].

For this application we developed a simulation bench for each clock synthesis approach and designed the system components using the RF noise models, including device thermal and flicker noise, for the 0.18µm mixed-mode process available from *Taiwan Semiconductor Manufacturing Company*. We have employed the *Cadence SpectreRF* environment for phase noise simulations.

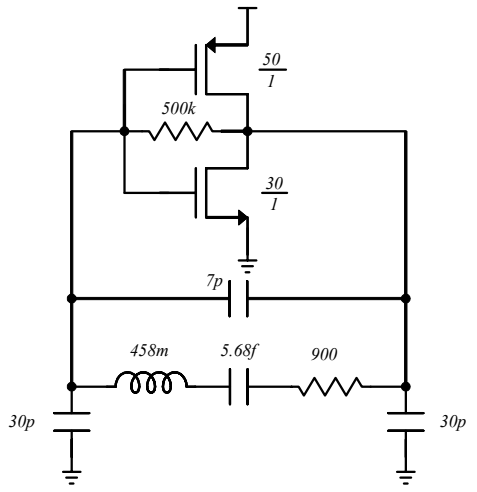

Figure 3. 3.125MHz bottom-up Pierce reference oscillator with equivalent electrical model for quartz crystal device.

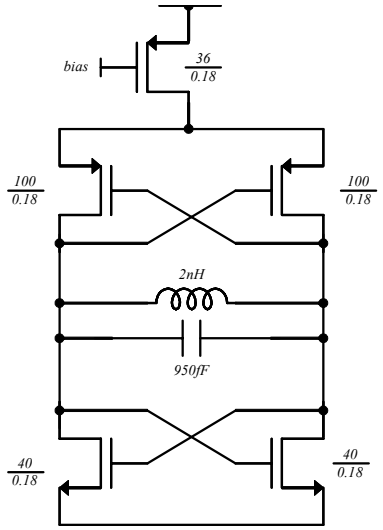

Figure 4. 3.2GHz CMOS-*LC* top-down reference oscillator.

In the bottom-up approach, the clock signal is generated from the Pierce reference oscillator shown in Fig. 3. The Pierce configuration, selected because it is a low phase noise topology [5], is commonly employed for clock generation. The quartz crystal has been modeled as a lumped series *RLC* circuit with parasitics, per a common manufacturer's specification. The quality factor of the device is 10,000 and the series resonant frequency is 3.125MHz. This particular resonant frequency deviates slightly from the *Intel* specification, but does not create a loss of generality in the analysis. It simply allows for integer frequency relationships. A ring VCO was also developed for the bottom-up system. Although an *LC* VCO is substantially more stable, for a 200MHz application frequency the required *L* and *C* component values are impractical to integrate on-chip.

The phase noise for both of the oscillators was simulated with *SpectreRF* and the results were modeled using *Verilog-A* and the phase-domain techniques described in [1]. Noise was modeled only for the Pierce reference oscillator and the VCO. Noiseless models for the PFD, CP, LPF, and divider were developed in *Verilog-A*. Noise was not included for these components since they introduce synchronous jitter and thus complicate this analysis. The designed PLL loop bandwidth was 600kHz. The phase-domain approach described in [1] was employed to simulate the noise performance of the entire system using these *Verilog-A* models.

The top-down design included a highly-stable 3.2GHz CMOS-*LC* oscillator, shown in Fig. 4, and a series of 4 D-flip-flops for frequency division. The loaded quality factor of the *LC* tank was estimated to be approximately 10. The complete top-down system was simulated at the device level in *SpectreRF*.

5. RESULTS

Table 2, on the following page, summarizes the results from the design, simulation, and analysis. The frequency division factor in the top-down approach is 16 and thus the theoretical phase noise improvement is 24.1dB. The achieved improvement was 23.8dB.

In contrast, the frequency multiplication factor in the bottom-up approach was 64, which corresponds to a theoretical phase noise degradation factor of 36.1dB. The simulated degradation was 36.2dB. Phase noise density plots for each approach are shown in Fig. 5 and Fig. 6. Note that the phase noise of the PLL output tracks the reference

Table 2. Performance metric comparison between bottom-up and top-down frequency synthesis approaches.

Performance Metric	Bottom-Up Synthesis	Top-Down Synthesis
Application Frequency, f_o (MHz)	200	200
Reference Oscillator Frequency, f_{ref} (MHz)	3.125	3,200
Multiplication/Division Factor, N	×64	÷16
Reference Oscillator Quality Factor, Q	10,000	10
Reference Oscillator Phase Noise Density, $(N_o/P_o)_{fm}$ (dBc/Hz)	-140.8 @ 10kHz offset	-83.0 @ 10kHz offset
Calculated Period Jitter at Reference from $(N_o/P_o)_{fm}$ @ 10kHz offset, J (fs)	233	5.5
Calculated Relative Period Jitter at Reference, J_{ppm} (ppm)	0.73	18
Synthesizer Output Phase Noise Density, $(N_o/P_o)_{fm}$ (dBc/Hz)	**-104.6 @ 10kHz offset**	**-106.8 @ 10kHz offset**
Calculated Period Jitter at Output from $(N_o/P_o)_{fm}$ @ 10kHz offset, J (fs)	**29**	**23**
Calculated Relative Period Jitter at Output J_{ppm} (ppm)	**5.9**	**4.6**
Phase Noise Density Accumulation/Reduction Factor, (dB)	+36.2	-23.8
Period Jitter Accumulation/Reduction Factor	0.12	4.2
Relative Period Jitter Accumulation/Reduction Factor	8.0	0.23

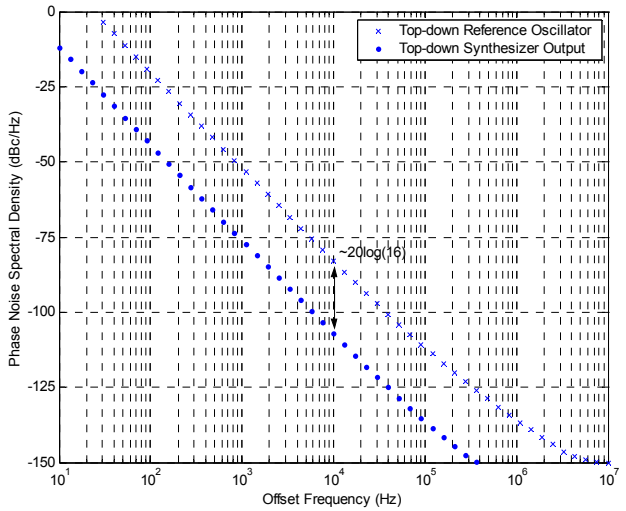

Figure 5. Top-down reference oscillator and synthesized clock phase noise spectral density. Phase noise was reduced by approximately 20*log*(16) due to frequency division.

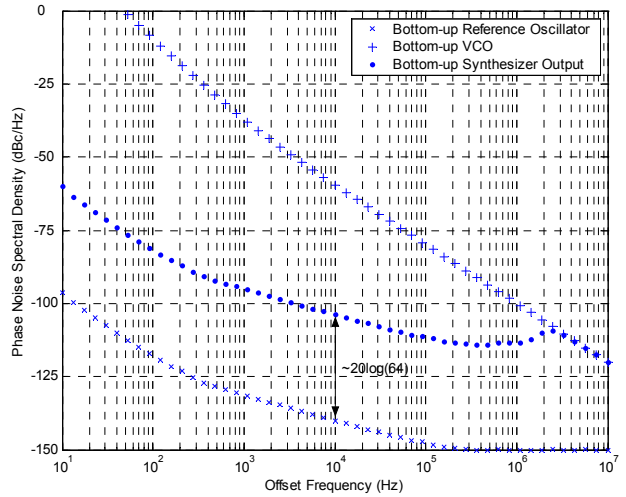

Figure 6. Bottom-up (PLL) reference oscillator, VCO, and synthesized clock phase noise spectral density. Phase noise was increased by approximately 20*log*(64) due to frequency division.

oscillator close to the fundamental, and the VCO far from the fundamental, as is expected.

Jitter metrics for each approach, shown in Table 2, were calculated using (5) at a 10kHz offset. The most significant observation is that the top-down approach realizes a frequency stability that is slightly better than the bottom-up approach. One could also integrate the phase noise densities to show similarity in the RMS jitter. The *LC* oscillator used in this approach contained a tank with a loaded quality factor of only 10, while the quality factor of the crystal reference was 10,000. The systemic accumulation error introduced in the PLL approach drastically reduces the high-performance delivered by the crystal-based reference. An enhanced *LC* oscillator could provide even more stable performance in a top-down system; the challenge still remains in attaining an accurate frequency.

6. CONCLUSION AND FUTURE WORK

We have analyzed and presented relationships describing the effects of frequency multiplication and division on short-term clock stability. Using a common application as a benchmark, the relationships were verified. A top-down approach to clock synthesis has been shown to be a simple alternative to the common bottom-up approach, while offering comparable stability. Moreover, this approach would enable the development of a monolithic clock reference. However, challenges still reside in realizing a high frequency reference for this approach that is both stable and accurate. Emerging technologies that enable the development of high quality factor references, such as microelectromechanical systems, likely hold the key to realizing a frequency synthesis system such as this. We intend to report on such a design in the future.

7. REFERENCES

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