Performance of Wireline Links Synchronized to Self-Referenced Solid-State Frequency Sources

Michael S. McCorquodale and Dongtai Liu
Mobius Microsystems, Inc.
Sunnyvale, CA USA 94086
{mccorquodale, liu}@mobiusmicro.com

***Abstract*—Self-referenced solid state oscillators (SSOs) are presented within the context of emerging frequency control devices targeted at crystal oscillator (XO) replacement. It is shown that SSOs typically exhibit lower far-from-carrier phase noise and lower period jitter than comparable XOs. This is considered in the wireline application, HS-USB, where a comparison is presented between the measured link performance when the link is synchronized to a 12MHz XO and SSO. It is shown that the SSO achieves superior link performance including a wider data eye and lower bit error rate while being implemented entirely in a solid-state process technology and with no external components.**

I. Introduction

Recently, there has been significant research, investment and commercial activity surrounding the development of silicon frequency sources including MEMS microresonators [1] and self-referenced solid-state oscillators (SSOs) [2]. These technologies have been developed to achieve integration and potentially displace piezoelectric quartz crystal oscillators (XOs) as the de facto frequency reference. Silicon frequency sources are capable of addressing certain limitations of quartz crystal (XTAL) technology including form-factor, cost structure and sensitivity to shock and vibration. However, recent reports make it clear that these technologies do not achieve performance which rivals XOs across all standard frequency control metrics [2][3]. Further, silicon frequency sources are not suited to narrowband wireless applications because these devices exhibit high close-to-carrier phase noise which results in reciprocal mixing and reduced receiver sensitivity. Nevertheless, silicon frequency sources continue to gain traction in wireline applications, such as HS-USB [4], where the limitations of quartz are relevant and frequency accuracy requirements are less stringent. Considering these trends, there exists an emerging interest in the system-level performance of links synchronized to silicon frequency sources.

In this work, a comparison is presented between the measured link performance of the wireline interface, HS-USB, when the link is synchronized to a 12MHz XO and SSO. In such applications, this low-frequency source is multiplied to the channel-rate by a phase-locked loop (PLL) in the physical (PHY) layer interface. It is shown that because the SSO exhibits lower far-from-carrier phase noise, lower period jitter and better power supply isolation than the XO, the data eye-width, and corresponding bit error rate, is superior with the SSO.

II. Self-Referenced Solid-State Oscillators

A. Background and Motivating Concepts

As shown in [2], the single sideband (SSB) phase noise power spectral density (PSD) of an oscillator can be related to the time-domain period jitter by the following expression,

$$\sigma_T = \sqrt{\frac{8}{\omega_o^2}\int_0^\infty \left(\frac{N_o}{P_o}\right)_{f_m} \sin^2(\pi f_m T_o)\,df_m}, \qquad (1)$$

where σ_T is the RMS period jitter (or the root of the classical variance of the period), ω_o is the fundamental radian frequency, N_o/P_o is the SSB phase noise PSD at frequency offset f_m from the fundamental and T_o is the oscillation period. The practical upper limit of the integral is bounded by the system bandwidth (BW), the measurement BW, or the loop BW of a channel-rate PLL utilized for frequency multiplication. The expression in (1) indicates that when transforming the frequency-domain phase noise to time-domain period jitter, the phase noise is masked by a $\sin^2$ function with one-half of the period of the oscillation frequency. This implies that the close-to-carrier phase noise is squelched and the far-from-carrier phase noise dominates the transformation. Thus, low far-from-carrier phase noise is paramount to achieving low period jitter.

Noting this, SSOs have been introduced where recent and representative examples include [2] and [4]. These devices are self-referenced to a frequency-trimmed and temperature-compensated radio-frequency (RF) *LC* oscillator. In [2], it was shown that ±26ppm total frequency error over process, voltage and temperature can be achieved with such devices. The architecture of these devices was motivated by the concepts just presented as well as the goal of solid-state integration. Considering the former, modern solid-state process technologies now support inductors with high quality (*Q*) factors and thin-film capacitors with low temperature coefficients. Thus, stable and accurate solid-state oscillators can be realized. Further, by designing the reference oscillator at RF, frequency division is exploited to reduce the phase noise PSD at the output frequency. For example, the reference oscillator in [4] operates at 1.536GHz and is frequency-divided by 128 to provide a 12MHz reference for USB. As shown in [2], and despite the comparatively low-*Q* of the *LC* reference oscillator, very low timing jitter is achieved.

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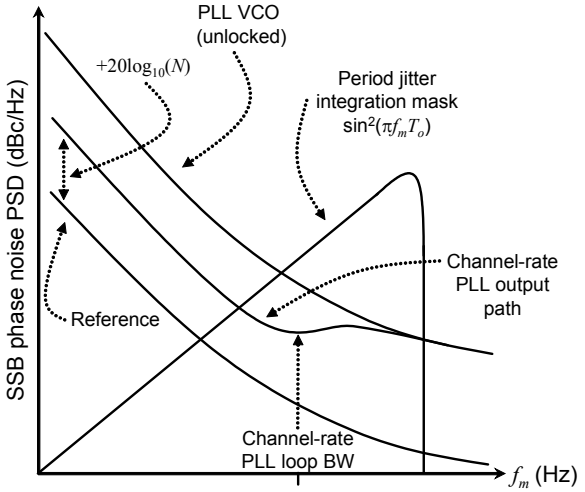


Figure 1. Illustration of the phase noise output path for a channel-rate PLL with multiplication factor, N. The phase noise is translated by $+20log(N)$ inside the loop BW. Outside the PLL loop BW, the VCO is tracked. The $\sin^2$ function in (1) illustrates how the phase noise is transformed to period jitter.

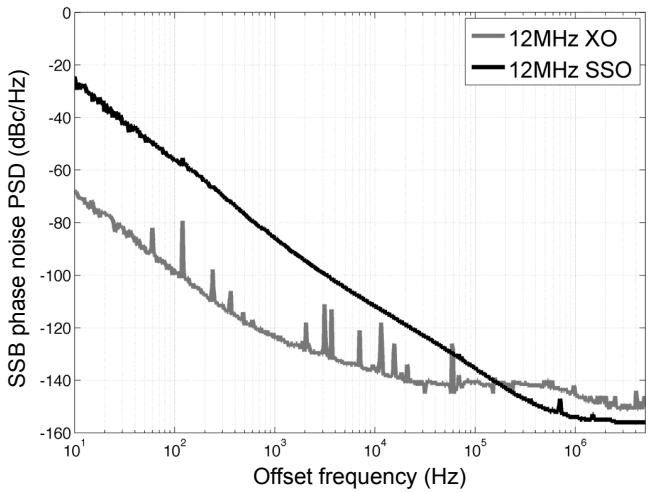


Figure 2. Measured SSB phase noise PSD for a 12MHz XO and SSO. The XO exhibits significantly lower close-to-carrier phase noise, more spurs and higher far-from-carrier phase noise than the SSO. The output of the XO passes through a wideband PLL with a unit loop multiplication factor.

In most wireline interfaces, a channel-rate PLL is synchronized to a low-frequency source. Fig. 1 illustrates the phase noise output path of a typical channel-rate PLL with frequency multiplication factor, N. Inside the PLL loop BW, the phase noise of the reference is shifted by $+20log(N)$ due to frequency multiplication. Outside the PLL loop BW, the VCO of the PLL is tracked. The $\sin^2$ function in (1) is also illustrated. The integral of the product of the output phase noise path and this function determines the channel-rate jitter. As illustrated in Fig. 1, the channel-rate jitter will depend on the phase noise of the reference, the PLL multiplication factor, the loop BW and the phase noise of the VCO. If the loop BW of the PLL is wide, then the majority of the jitter will originate from the reference. Further, if the loop multiplication is high, the phase noise and corresponding jitter will be high. In contrast, if the loop BW is narrow, channel-rate jitter will be dominated by the VCO.

B. Measured Frequency Reference Performance

A discrete 12MHz SSO, similar to that in [2], was tested and compared to a 12MHz XO in a commercial off-the-shelf thumb-drive with an HS-USB interface. In this platform, the reference clock is derived from a passive 12MHz XTAL that is mated to the HS-USB PHY which contains the sustaining circuit. The specific implementation details of that circuit are not known.

The measured SSB phase noise PSD for both devices is shown in Fig. 2. The XO exhibits much lower close-to-carrier phase noise because its Q-factor is significantly higher than the Q-factor of the SSO. However, the XO reaches a noise floor of approximately -140dBc/Hz while the floor for the SSO is below -155dBc/Hz. This is likely due to the fact that the sustaining circuit for the passive XTAL is power-limited. At offset frequencies in excess of 1MHz, the output of the XO in this platform is passed through the channel-rate PLL with a unit multiplication factor. At these offset frequencies, the output VCO is tracked, thus indicating the PLL loop BW is approximately 1MHz. Additionally, the XO exhibits significant spurs across the measurement BW. This occurs because the power supply on the PHY is not regulated; thus, significant noise from the channel-rate signaling is coupled into the oscillator circuit. This is not the case for the SSO because it is a separate and discrete device which contains internal power supply regulation.

The RMS period jitter of the two devices was measured with a 20GSa/s real-time oscilloscope with a 6GHz analog BW. Results are shown in Fig. 3 where 100kSa were captured for each device. The channel settings are identical for both devices, as shown, and the RMS period jitter is displayed on the line labeled "sdev." As expected from the phase noise measurements in Fig. 2 and as predicted from the expression in (1), the period jitter for the XO is higher than for the SSO because of the difference in far-from-carrier phase noise. Further, the significantly higher close-to-carrier phase noise in the SSO, as compared to the XO, did not have any bearing on the resulting period jitter.

III. Wireline Link Performance

A. Measured Link Performance

The channel-rate for HS-USB is 480Mbps and it is signalled differentially. For the PHY under test, the reference frequency must be 12MHz. Therefore, the loop multiplication factor is 20 and the approximate loop BW is 1MHz as shown in Fig. 2. The channel-rate performance of the link was measured using the same real-time oscilloscope as was used for period jitter measurements. First, the passive 12MHz XTAL

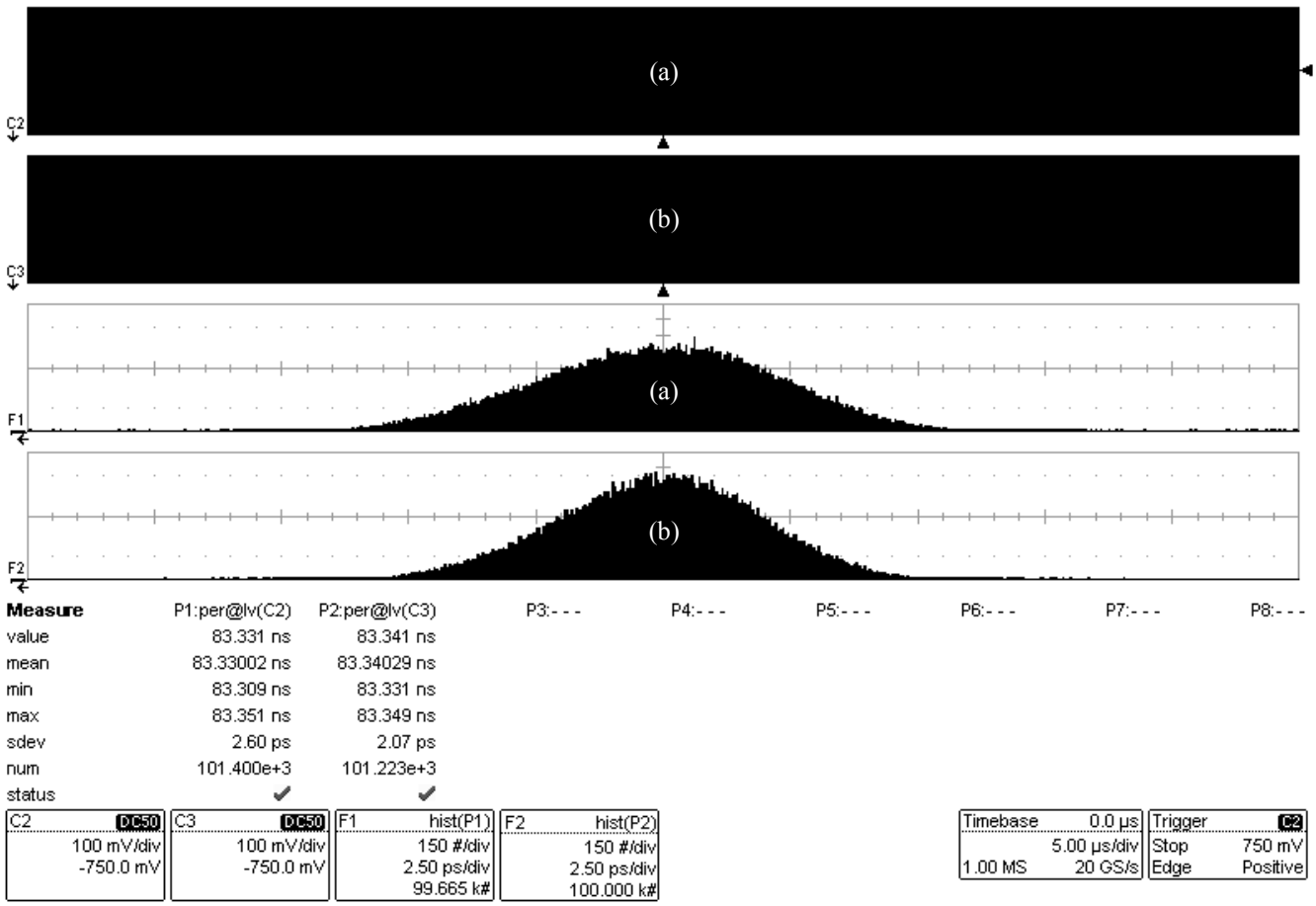


Figure 3. Measured RMS period jitter: (a) 12MHz XO: 2.60ps (b) 12MHz SSO: 2.07ps.

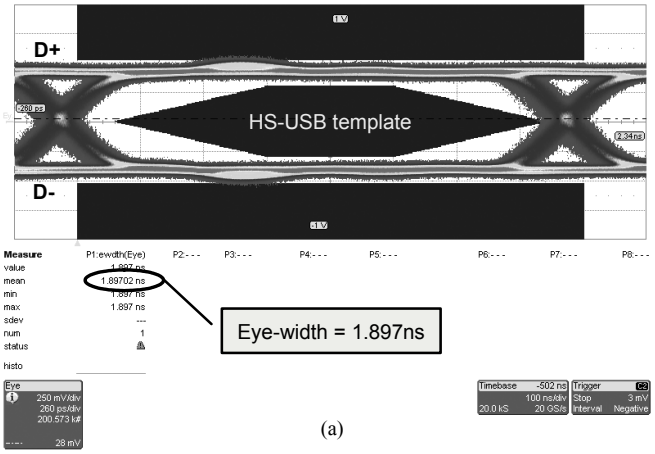
was mated to the PHY. Second, the XTAL was removed and the output of the SSO was driven onto the input pin on the PHY for the XTAL.

Eye-width measurements for the two different frequency references are shown in Fig. 4. Here, the PHY is placed into a mode where a standardized bit sequence is repeated for the measurement interval. The positive and negative data lines (D+ and D- respectively) were measured. To be compliant with the specification, these signalling lines must not cross into the eye template as shown. The instrument measures the eye-width at one-half of the peak-to-peak signalling level. When the PHY was referenced to the SSO, the eye-width was 30ps wider than when it was referenced to the XO. These results confirm that the channel-rate loop BW is wide and the far-from-carrier phase noise in the reference is tracked because there is a difference in performance. However, this difference is also small and less than 2%. This indicates that the output VCO of the PLL contributes significantly to the channel-rate jitter.

Bathtub curves were measured for both cases as well and are shown in Fig. 5. Here, the link bit error rate (BER) is estimated at different offsets across the unit interval (UI) by extrapolating the results from the jitter and eye-width measurements. 925mUI is a standard measurement offset for HS-USB. As shown in Fig. 5, when the PHY is referenced to the XO, the BER is $10^{-6.2}$ while it is $10^{-8.5}$ when referenced to the SSO. These results are consistent with the eye-width measurements where the SSO exhibited a wider eye-width.

B. Discussion

For this particular HS-USB PHY, the link performance was superior when referenced to the 12MHz SSO as opposed to the XO. However, and as described previously, the link performance is determined by several variables including the phase noise of the frequency reference, the loop multiplication factor, the loop BW and the phase noise of the channel-rate VCO. In this case, the channel-rate PLL loop BW was wide. Thus, the far-from-carrier phase noise in the frequency reference was tracked and contributed to the link performance where a clear difference in performance was observed between the XO and SSO. Additionally, the jitter of the 12MHz reference was influenced by power supply noise. This suggests that the common approach of integrating the oscillator circuit onto the PHY and mating it to a passive XTAL can compromise link performance.



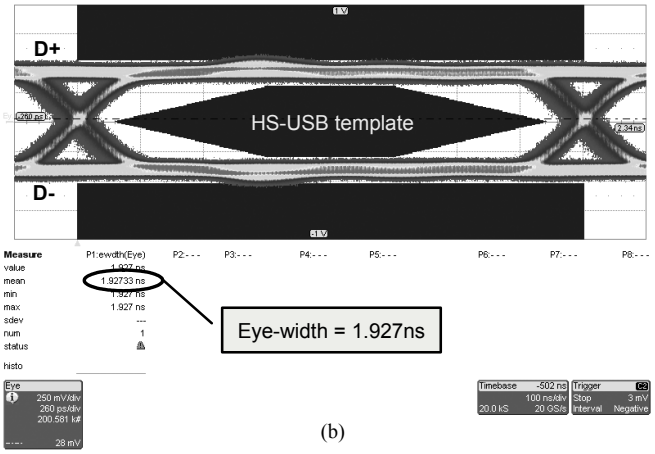
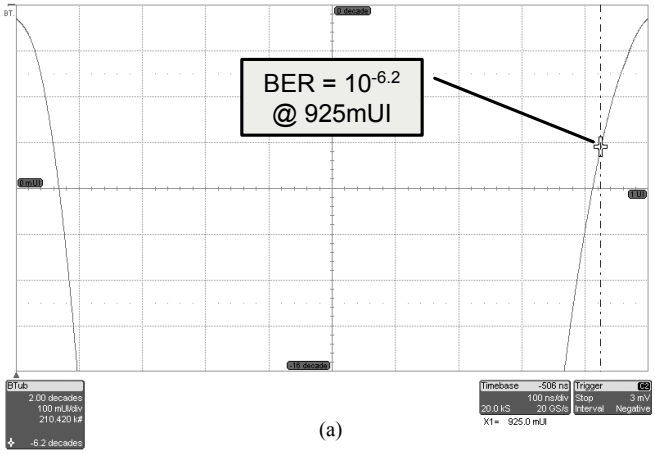


Figure 4. Measured eye-width for a 480Mbps HS-USB PHY referenced to a 12MHz: (a) XO (b) SSO. The eye-width is 30ps wider when the link is referenced to the SSO.



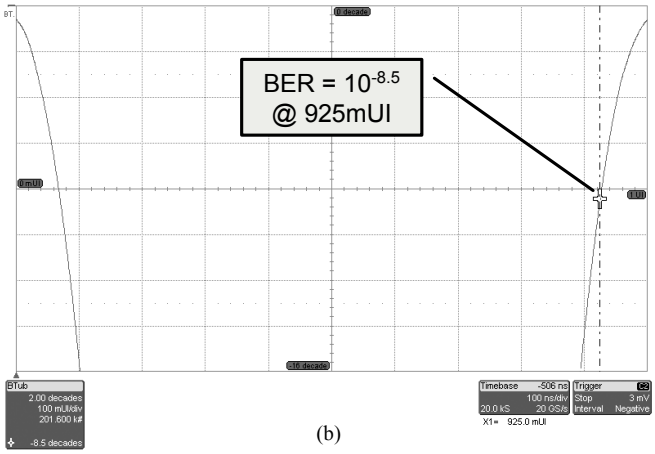


Figure 5. Measured bathtub curve for a 480Mbps HS-USB PHY referenced to a 12MHz: (a) XO (b) SSO. The BER is over 100 times lower at the standard offset of 925mUI when the link is referenced to the SSO.

IV. Conclusion

Self-referenced solid-state frequency sources have been introduced recently as a new frequency generation technology that is fully-integrated. Some of the motivating concepts behind the development of these devices were discussed briefly. Further, performance of SSOs was presented and compared to XOs where it was shown that SSOs exhibit higher frequency error and close-to-carrier phase noise than comparable XOs at the same frequency. However, SSOs typically exhibit lower far-from-carrier phase noise than comparable XOs. Consequently, SSOs exhibit timing jitter that is as low as, or lower, than XOs while achieving frequency accuracy well within the requirements for many wireline applications.

In this work, the link performance of a common wireline interface, HS-USB, was measured for two different frequency references: a 12MHz XO and a 12MHz SSO. It was shown that when the PHY was referenced to the SSO, the link performance, including eye-width and BER, was superior than when it was referenced to the XO. These results are explained by the fact that the XO exhibited higher far-from-carrier phase noise than the SSO due to limited power in the oscillator circuit and power supply noise coupling into the oscillator. Further, the PHY that was tested contained a wide BW channel-rate PLL. Thus, the far-from-carrier phase noise in the frequency reference was tracked and contributed to the link performance.

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