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An Integrated MEMS-BiCMOS SINCGARS Transceiver

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***Abstract*—This paper reports on the design of an integrated transceiver that supports SINCGARS (Single Channel Ground-Airborne Radio System). Utilizing both transistors and microelectromechanical systems (MEMS), the circuit transmits preprocessed discrete-time baseband data and receives RF passband signals that are mixed to 100kHz and sampled by a fast ADC for off-chip demodulation. By using micromechanical (μmechanical) resonators and filters a low-IF (or digital-IF) communication system architecture is realized. This design marks the advent of Very Large Scale Mechanical Integration (VLSMI) by merging 46,413 transistors in a 0.6μm BiCMOS process with 9,286 μmechanical devices using an embedded micromachining technique [1].**

I. Introduction

SINCGARS is a frequency-hopped spread-spectrum, VHF-FM voice and Binary Frequency Shift Keyed (BFSK) data communication system used by the US army in the forward battle area. The system utilizes 2,320 25kHz channels from 30-87.975MHz. BFSK data is transmitted via one of two frequency offsets, 5kHz or 10kHz, while the data rate is 16kbps. FM voice is transmitted with a frequency deviation of 6.5kHz. The 99% bandwidth of the system is 18.5kHz [2][3].

The designed system supports all of these modes of operation over all of the frequencies specified, but is unique by virtue of a system on a chip (SOC) architecture that is realized through the use of MEMS. Typically, the RF transmit (TX) and receive (RX) sections of a transceiver are integrated at the board level along with several other functional units in a communication system [4], which presents a bottleneck towards the miniaturization of current day transceivers. The system designed here integrates the RX and TX sections along with other frequency selection and synthesis components that are typically off-chip.

II. System Architecture

Many communication systems obtain frequency selectivity through the use of one or more fixed intermediate frequency (IF) filters with a narrow bandwidth, such as a surface acoustic wave (SAW) filter. In such systems the front end filter, or preselector, is generally a wideband filter that selects several signals and the mixer heterodynes one signal to the IF. Fig. 1 presents a system level schematic of this common superheterodyne architecture. It is well known that the third order intermodulation (IM_3) distortion of the low noise amplifier (LNA) coupled with the phase noise of the local oscillator (LO) that downconverts the input signal can cause receiver desensitization [5]. This concept is illustrated best by Fig. 2.

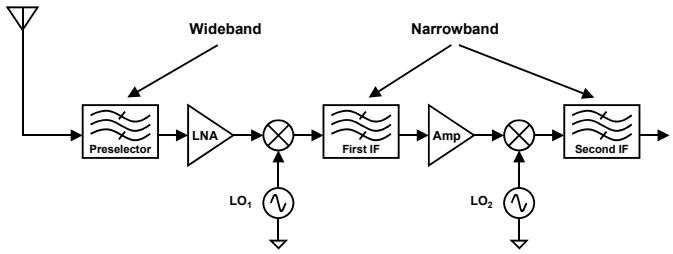


Fig. 1: Standard double conversion superheterodyne transceiver architecture with wideband preselector and narrowband IF filters.

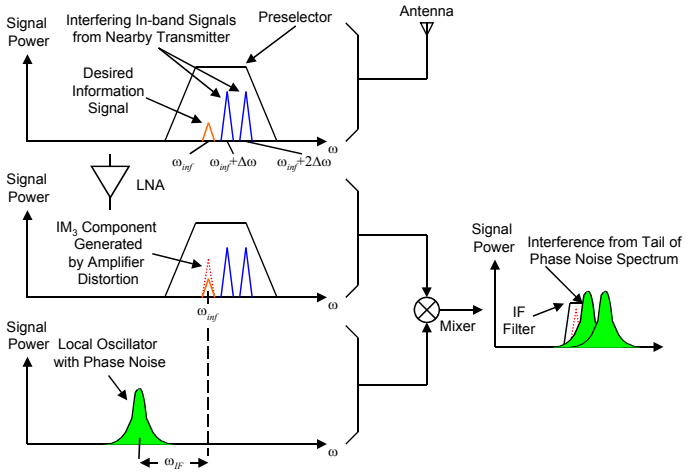


Fig. 2: Illustration of receiver desensitization due to LNA IM_3 and LO phase noise in standard heterodyning architecture.

The architecture selected for this design is novel since it replaces the preselector with a bank of narrowband μmechanical filters and therefore IF filtering is no longer required. Not only does this permit channel selection at RF, but it also relaxes the IM_3 requirements for the LNA and the phase noise requirements

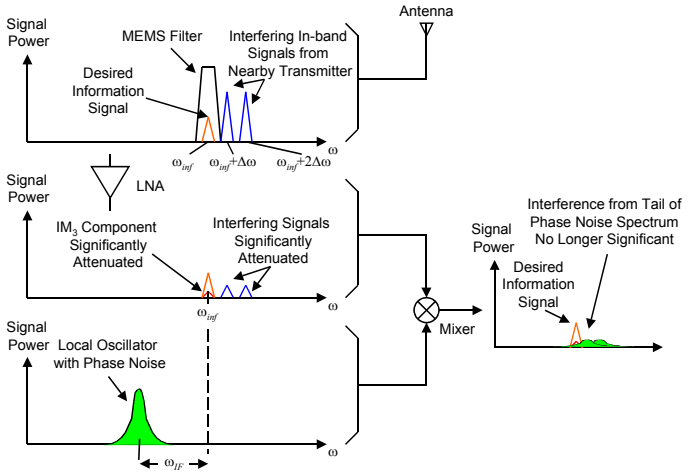


Fig. 3: Illustration of proposed architecture and reduced sensitivity to LNA IM_3 and LO phase noise.

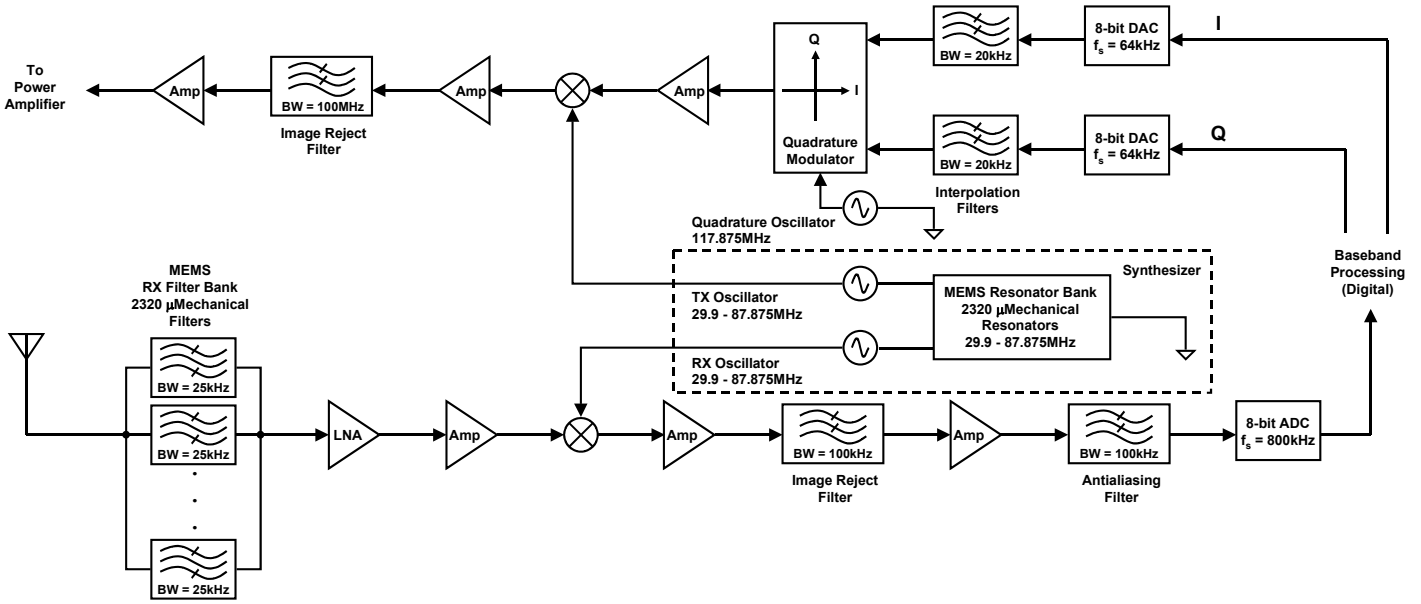


Fig. 4: Integrated MEMS-BiCMOS SINCGARS transceiver architecture.

for the reference oscillator as shown in Fig. 3. The complete transceiver architecture is presented in Fig. 4. This architecture cannot be realized on-chip with other highly selective filters due to their macroscopic size and incompatibility with CMOS processing. However with the current progress in merged micromachining and CMOS technology, it is possible to fabricate and integrate several thousand µmechanical filters directly on-chip.

The architecture features a unique technique of direct frequency synthesis using a bank of µmechanical resonators. The synthesizer contains one resonator per channel frequency in SINCGARS and therefore there is no need for an off-chip reference. The benefits and implications of this technique will be described later.

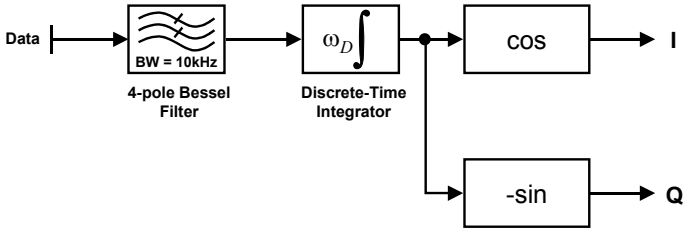
An off-chip digital circuit must preprocess the data to be transmitted and provide the in-phase and quadrature baseband components to the transceiver as shown in Fig. 5a. FM passband transmission is achieved by quadrature modulation via the following relationships:

$$s(t) = \cos\left(\omega_c t + \omega_D \int_0^t m(\tau)d\tau\right) \quad (1)$$

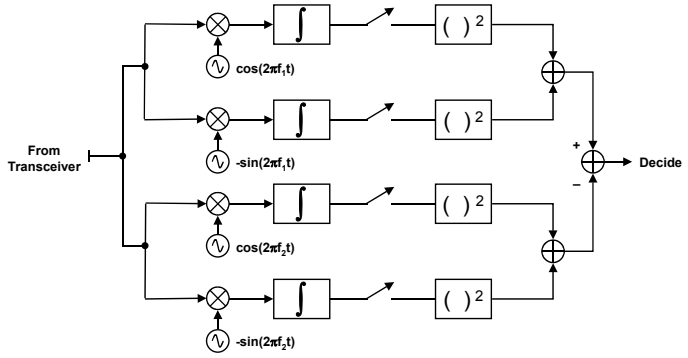
$$s(t) = \cos\omega_c t \cos\omega_D \int_0^t m(\tau)d\tau - \sin\omega_c t \sin\omega_D \int_0^t m(\tau)d\tau \quad (2)$$

$$s(t) = I\cos\omega_c t + Q\sin\omega_c t \quad (3)$$

where $m(\tau)$ is the information signal, ω_c is the carrier frequency, ω_D is the frequency deviation, $s(t)$ is the passband signal, and I and Q are the baseband in-phase and quadrature components respectively. This technique allows FM voice and BFSK data to be supported by the same hardware [6]. Additionally, the BFSK data is transmitted with continuous phase (CPFSK) which is known to provide superior performance as compared to switched phase FSK [7]. After modulation, the resulting signal is mixed down to the correct transmit frequency by the synthesizer and the image frequency is rejected. The signal is buffered and presented to the power amplifier, which is not integrated in this design.



(a)



(b)

Fig. 5: Required off-chip processing operations. (a) Discrete-time preprocessing prior to transmitter. (b) Demodulator and detector structure for data recovery after down conversion.

The receiver accepts RF signals through one activated filter in the µmechanical filter bank. The signal is amplified and down-converted to 100kHz. After image rejection and further amplification, the signal is bandlimited and sampled for demodulation [7][8][9] off-chip as shown in Fig 5b.

III. Subsystem Designs

μMechanical Resonators & Filters

The resonator topology used in this design is a free-free beam vertically driven resonator [10] shown in Fig. 6. The device is a capacitive transducer that operates by applying an AC excitation voltage to the drive electrode which will cause the suspended beam to deflect when the input signal frequency corresponds to the resonant frequency of the beam. The beam is supported by torsional mode quarter-wavelength supports that are anchored to the ground plane and connected to the beam at the node points of flexural deflection. By doing so, the beam is *virtually* levitated since the supporting structure presents effectively zero torsional-mode impedance to the device.

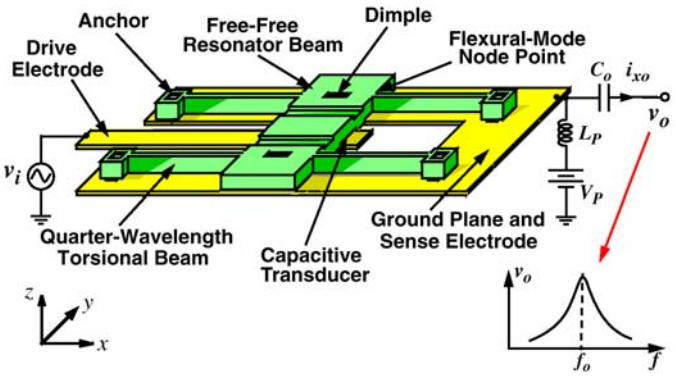


Fig. 6: Free-free beam μmechanical resonator.

This μmechanical structure was selected for its high quality factor over the frequencies of interest to this design. However, the design here is more aggressive than those reported in [10]. Specifically, the devices of this system were designed with a smaller electrode-to-beam gap, which lowers the motional series resistance of the device. This is desirable in order to present a reasonable impedance to the off-chip antenna matching network. Furthermore, low motional series resistance permits reference oscillator start-up at an acceptable power level.

A μmechanical filter is realized by linking two resonators at their low velocity coupling point with a flexural mode beam. To attain a properly flattened passband, termination resistors are required at the input and output ports of the filter. The termination resistance is given by:

$$R_{Qinput} = R_{Qoutput} = R_X\left(\frac{Q}{qQ_{fltr}} - 1\right) \quad (4)$$

where Q is the resonator quality factor, $Q_{fltr}=(f_{IF}/B)$ (where f_{IF} is the center frequency and B is bandwidth), q is a normalized Q value found in filter cookbooks [11], and R_X is the motional resistance associated with a particular resonator. With higher Q's, free-free beam resonators exhibit better filter performance (i.e. smaller insertion loss and narrower channel selection) than clamp-clamp beam resonators [10].

Synthesizer

Considering the detrimental effects of reference oscillator phase noise as shown previously, it is clearly desirable to generate a reference with low phase noise in a communication system. However, this task becomes difficult over a wide bandwidth since oscillator phase stability is related to quality factor and high Q generally restricts the tuning range achievable by a given oscillator. Commonly, high Q quartz crystal resonators are used to generate a stable reference and frequency synthesis is accomplished using a phase-locked-loop (PLL). This technique has two shortcomings. First, the phase noise performance at the PLL output is degraded by $20log(N)$ as compared to the reference, where N is the frequency multiplication factor around the loop. Second, the phase lock time becomes very long for large N [12], which is unacceptable for frequency-hopped spread spectrum systems.

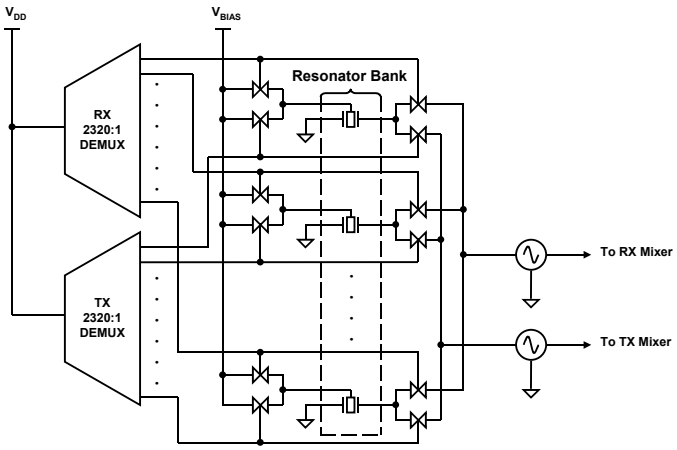


Fig. 7: Synthesizer architecture based on switchable MEMS resonator bank for selection of TX and RX oscillator tanks.

The solution is to utilize high Q μmechanical resonators by designing a switchable resonator bank such that one resonator per frequency can be selected and presented to the active circuit that sustains the oscillations. Such a notion is inconceivable with quartz crystal technology due to the macroscopic size of these devices and the inability to integrate quartz at the wafer level. However, the same is not true of μmechanical resonators.

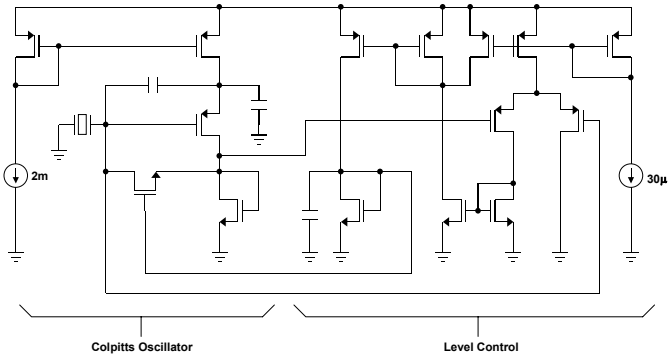


Fig. 8: Colpitts reference oscillator with active level control circuitry. Three instances exist in the design: TX, RX, and quadrature oscillators.

Since the transceiver does not transmit and receive at the same frequency, this bank can be shared by the receiver and transmitter subsystems as shown in Fig. 7. One μmechanical resonator was designed for each of the 2,320 channels used by SINCGARS. The two demultiplexers select and bias one resonator for the TX oscillator and another for the RX oscillator. The resonators are designed to present a constant tank resistance to the active circuit while operating at a 10V nominal

bias, which is well below the breakdown voltage of the devices in the BiCMOS process.

Oscillations are sustained by the active circuit shown in Fig. 8, which is a simple Colpitts oscillator [13][14] with level control circuitry [15] to provide a constant voltage to the mixers. Based on a tank Q of 10,000 the theoretical phase noise performance by the technique in [16] is less than -120dBc at 1kHz offset from the carrier, which is comparable to quartz crystal oscillator performance. The circuit dissipates 20mW of power and starts up in less than 3ms.

Quadrature Modulator

A μmechanical quadrature modulator is used to sum the I and Q signals from the baseband digital processor. The quadrature modulator is comprised of two independent μmechanical mixer+filter, a device previously reported in [17]. The concept of the mixer+filter is to perform both frequency translation and channel filtering using a simple mechanical device, with the advantage of low power consumption and minimum real estate on the chip. The mixer+filter consist of two clamp-clamp beam resonators, coupled by a highly nonconductive spring, as shown in Fig. 9. The coupling beam is made nonconductive by using an ion implantation blocking mask. Due to the nonconductive nature of the coupling spring and the electrode-to-beam gap, large isolation is achieved between the ports. Frequency translation is realized by a quadratic nonlinear voltage-to-force capacitive transducer at the input resonator, while frequency selection is automatically achieved by mechanical filtering in the device.

To insure that the phase and amplitude mismatch are well below 1° and 1dB, symmetry is preserved in the mask layout of the quadrature modulator. The advantage of a symmetrical layout is that noise and parasitics which affect the phase and amplitude are balanced and cancelled out. To minimize noise and maintain a low power design simple 5-transistor operational transconductance amplifier (OTA) buffers are used at the inputs and outputs of the mixer+filters. The I and Q outputs of the quadrature modulator are summed using a wideband operational amplifier. The oscillator signals driving the mixers are 90° phase shifted from each other by means of a RC-CR polyphase filter [14][18]. Due to uncontrollable process variation, the poles associated with the RC-CR network may vary, which in turn can lead to phase and amplitude mismatch. In order to alleviate this problem, the capacitors in the RC-CR network are implemented using tunable bipolar varactors, with a tuning range of approximately 3%. The capacitance can be set by adjusting the reverse bias voltage on the varactors.

Gilbert Cell Active Mixer

The mixers shown in Fig. 4 are four-quadrant predistorted bipolar Gilbert cells. This topology provides better noise performance, higher dynamic range, and lower conversion loss as compared to other structures [13]. Fig. 10 shows the schematic of the predistorted mixer. The differential pair to which the RF signal is applied is the predistortion section, which is required to linearize the cell. Emitter degeneration is used in both of the differential pairs to further improve linearity. The circuit is biased by an on-chip supply-independent voltage reference.

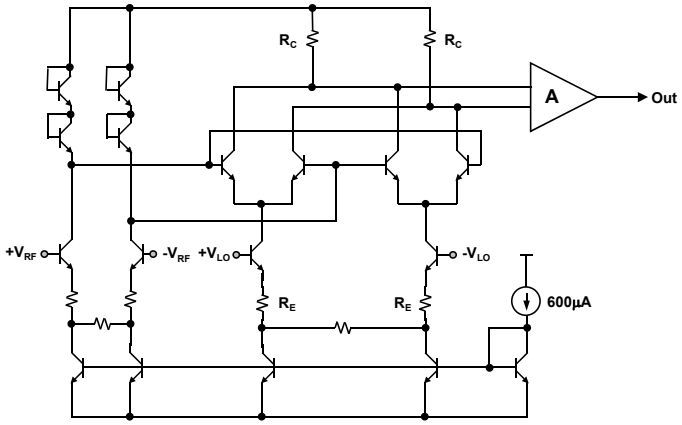


Fig. 10: Gilbert cell active mixer and OTA.

The output voltage of the mixer cell is given by:

$$v_o = K v_{LO} v_{RF} \; ; \tag{5}$$

$$K = \frac{4R_C}{R_E^2 I_{bias}} \tag{6}$$

where I_{bias} is the bias current and R_C and R_E are the collector and emitter resistors of the mixer.

At the output of the receiver mixer, an OTA is used in order to provide differential to single ended conversion and reject the high frequency component generated by the mixing operation. Additionally, the OTA provides signal amplification which compensates for conversion loss.

The mixer operates at frequencies between 29MHz and 90MHz, and provides an output signal at 100kHz with -9.76dB conversion loss. The OTA voltage gain is 44dB and the two circuits together consume 28mW of power.

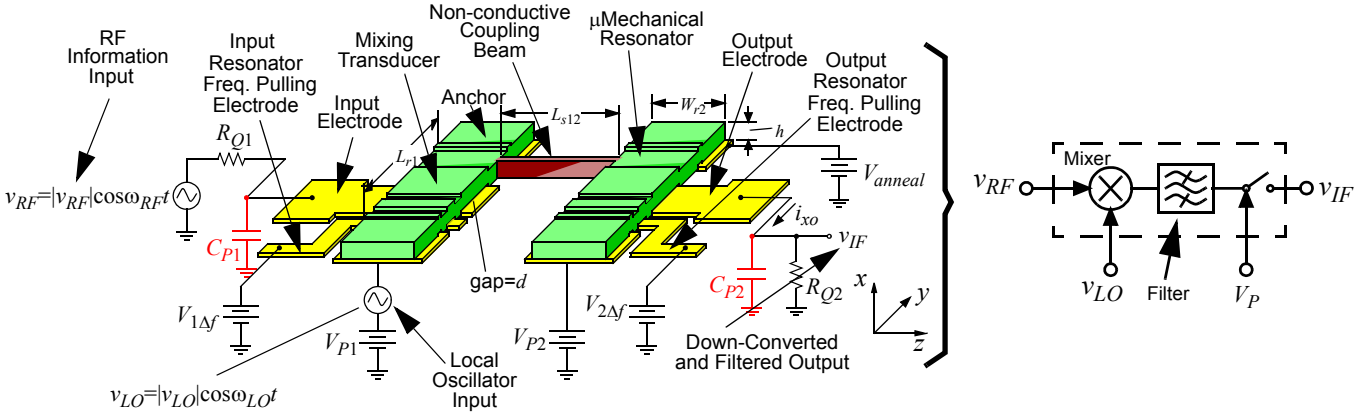


Fig. 9: μMechanical mixer-filter and equivalent functional diagram.

AMPLIFIERS

In order to meet the 90MHz system bandwidth requirement, the wideband amplifier (WBA) and the low noise amplifier use a BiCMOS topology as shown in Fig. 11. Bipolar transistors are utilized for the input differential pair because of their large transconductance, which translates to large gain, wide bandwidth and low noise. To maximize linearity, the bias current for the LNA is higher than in the WBA. Furthermore, the LNA is designed with a higher gain in order to set the system noise figure. The design specifications for the WBA and LNA are shown in Table I. The input equivalent noise is based upon the 25kHz bandwidth captured by the receiver input filter.

Table I: Amplifier Specifications

Parameters	WBA	LNA
Gain	30dB	35dB
Bandwidth	100MHz	119MHz
Power	2.5mW	3mW
Noise Figure	—	4.8dB
Input equivalent voltage noise ($\overline{v_{eq}}$)	—	0.5μV
Input equivalent current noise ($\overline{i_{eq}}$)	—	0.9pA

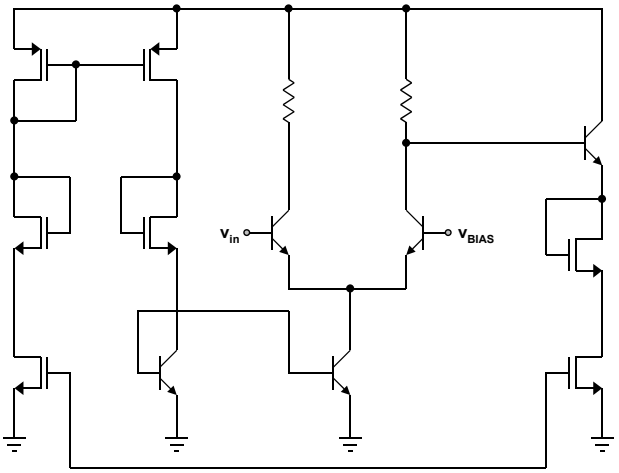


Fig. 11: Wideband and low noise amplifier topology.

ANALOG-TO-DIGITAL CONVERTER

An 8-bit analog to digital converter (ADC) defines the interface between the analog receiver and digital baseband processor. The least significant bits (LSBs) are converted using a 5-bit interpolating-folding technique [19][21][21], while the most significant bits (MSBs) are resolved using a 3-bit flash ADC, as presented in Fig. 12. This architecture is advantageous since it does not require as many comparators as a full flash converter

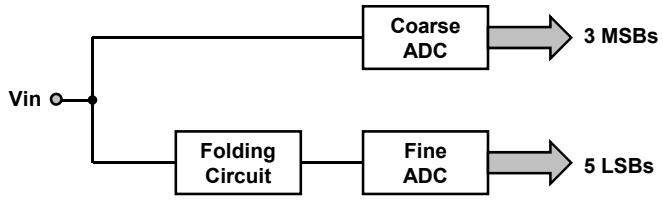


Fig. 12: ADC system block diagram: coarse and fine ADC in parallel.

yet it maintains the speed of a flash with lower power and complexity. Moreover, the three MSBs and five LSBs are generated synchronously, thus achieving the same throughput as a flash converter.

Each of the four folding signals, shown in Fig. 13 are generated from a network consisting of nine cross-coupled differential pairs presented in Fig. 14. Here the reference voltage is generated by a resistor ladder. To overcome the non-linearity due to the folding operation, the four folding signals are interpolated using two resistive networks to generate 32 signals. The 32 signals are then fed into 32 comparators for zero-crossing detection. The thermometer code at the output of comparators is converted to a circular form by XORing the adjacent bits [22]. This circular code sequence is fed into a 5-bit ROM decoder to generate the LSBs of the fine converter.

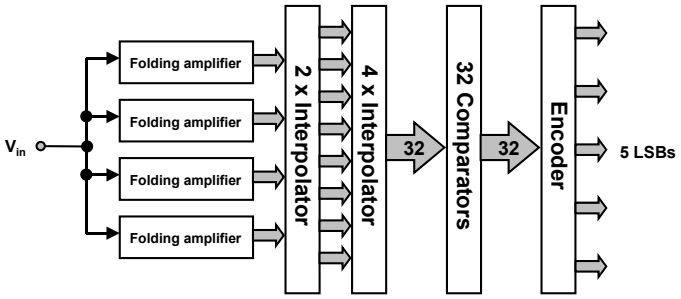


Fig. 13: Fine ADC system block diagram.

Due to the large amount of processing in the folding-interpolating section, the delay in the fine converter is inherently longer than in the 3-bit flash converter. In order to synchronize the outputs, a delay is introduced in the coarse converter.

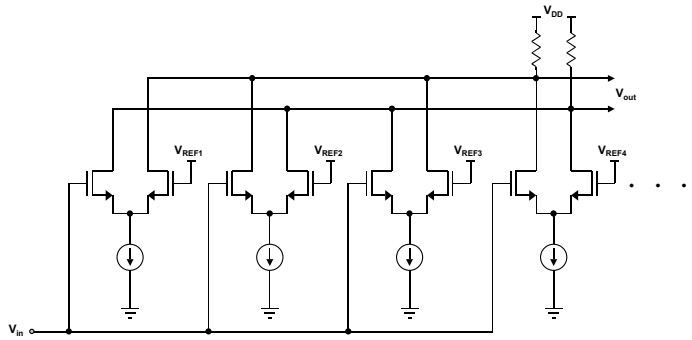


Fig. 14: Folding circuit based on cross-coupled differential pairs.

DIGITAL-TO-ANALOG-CONVERTER

Two 8-bit digital-to-analog converters (DACs) are used as an interface between the digital baseband processor and the analog transmitter subsystem. In order to reduce power consumption and still maintain high bandwidth, a simple two-step DAC was selected for the design [23]. The system schematic of the DAC is shown in Fig. 16. The primary advantage to using this architecture over charge and current mode DACs is that the number of active circuits (3 buffers) and resistors are kept to a manageable level. The majority of the circuit is comprised of CMOS digital logic, which consumes very little power. For 8-bit operation, the DAC is divided up into two 4-bit segments, where the first segment accounts for the coarse bits (MSBs). The four MSBs of the input word are decoded to 16 lines that control the connection of the buffers to the resistive network. Depending on the output of the LSB of the coarse section, the appropriate side of the fine DAC switched array is selected. The final output of

the DAC results from linearly interpolating the voltage drop between the fine resistive network. In each conversion cycle, the polarity of the voltage across the fine string is reversed by alternating between the two fine switch arrays.

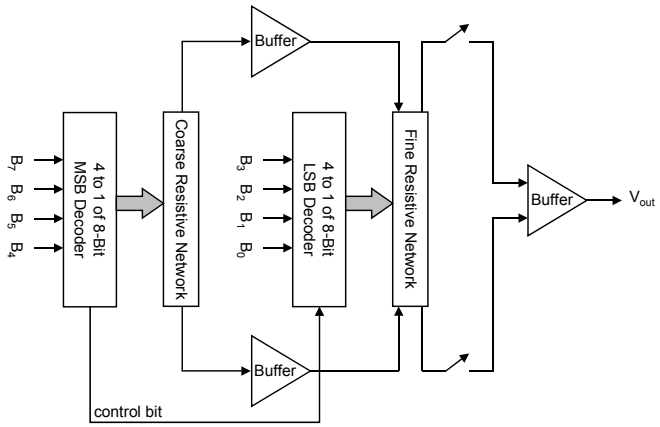


Fig. 16: Coarse-fine flash DAC system architecture.

ACTIVE FILTERS

In order to achieve correct data conversion at the DAC and ADC interface, an interpolation filter and antialiasing filter are required. These filters are 2nd order 0.1dB-ripple Chebyshev filters as shown in Fig. 17. The impedance of each is fixed and the frequency is tuned by selecting the appropriate capacitor values [24].

This same filter topology is used after the downconversion mixer for purpose of image rejection on the transmit side.

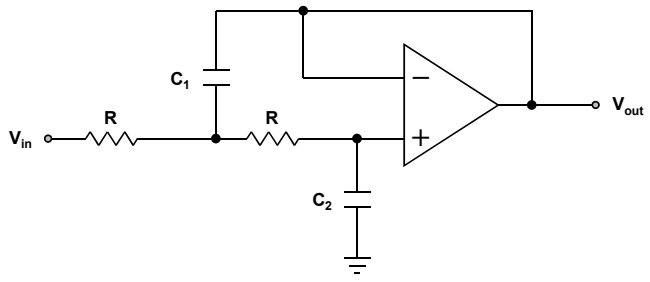


Fig. 17: Active filter topology: 2nd order 0.1-dB ripple Chebyshev LPF.

IV. LAYOUT & FABRICATION

The mask set for this design, shown in Fig. 18, was generated full-custom. This is largely due to the lack of computer aided design (CAD) tools for μmechanical devices and the desire to minimize and balance parasitic effects in the analog sections.

In order to complete this design, software was developed in the *Mathematica* environment to synthesize the dimensions for the μmechanical devices based upon process and design parameters. The filters were designed to meet bandwidth, termination resistance, frequency, and DC bias requirements while the resonators were designed to meet frequency, DC bias, and tank resistance specifications. This synthesis software coupled with a silicon compiler would not only expedite the μmechanical design process, but could potentially popularize designing in merged MEMS and circuits processes in the future. Indeed, this design shows there exists an application and commercial market for these CAD tools.

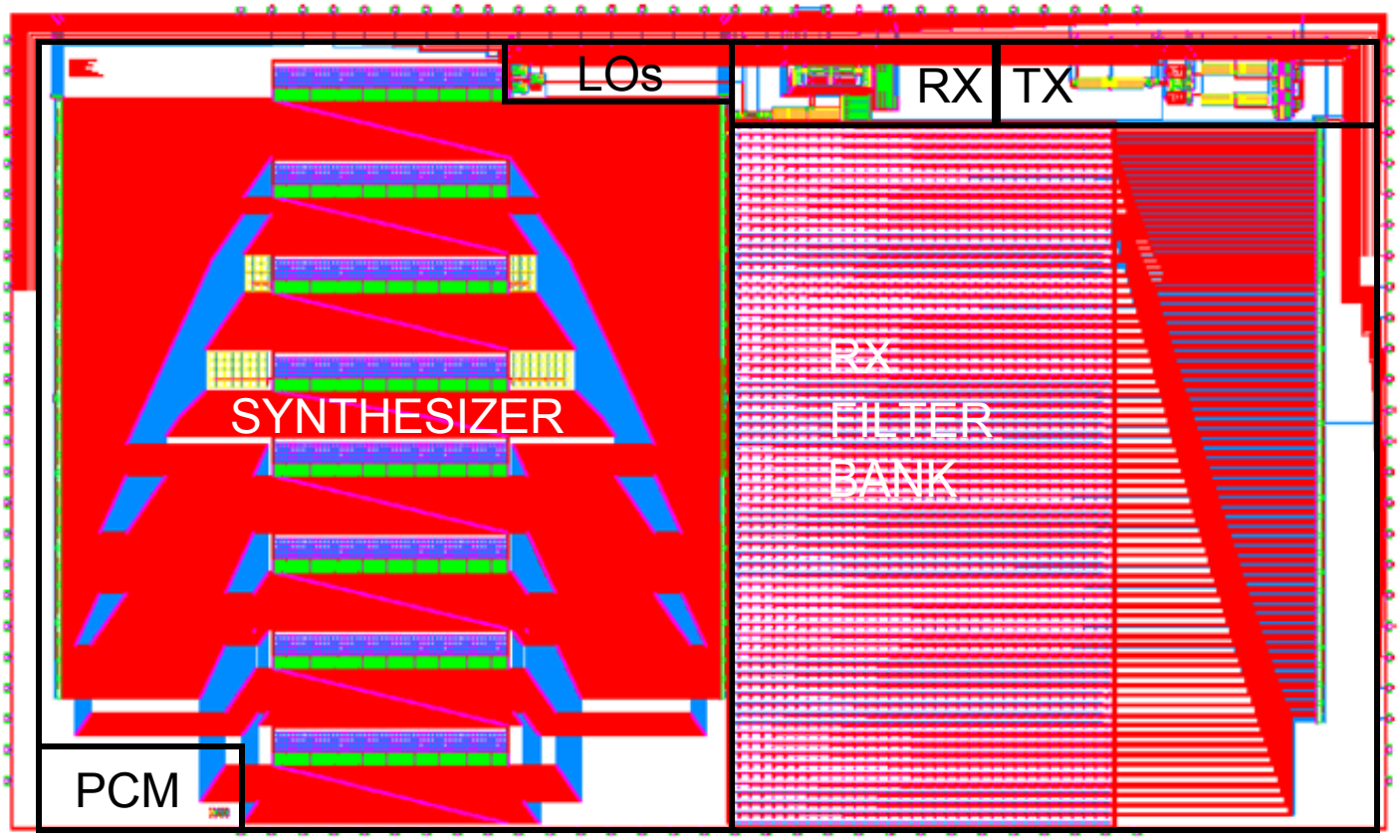


Fig. 18: Integrated circuit mask set.

Integration of the BiCMOS circuits and the μmechanical devices can be achieved by using a wafer level micromachining process as described in [1]. Using a MEMS-first technique, the μmechanical devices are fabricated in a trench that is etched into the starting silicon. The μmechanical resonators and filters are fabricated in the trench using a standard surface micromachining process as described in [25]. Both the structural and electrode materials are doped polycrystalline silicon while a sacrificial layer of oxide defines the electrode-to-beam gap. The trench is then sealed and standard microelectronic processing is carried out over the MEMS devices. The BiCMOS circuits are fabricated in a 0.6μm process with an f_T of 25GHz. Table II summarizes the statistics for the integrated circuit.

Table II: Integrated Circuit Statistics

Parameter	Value
No. of Transistors	46, 413
No. of μMechanical Devices	9,286
Die Area	3cm x 1.8cm
No. of I/O Pads	47
Power	213mW

V. Testing

Three analog design for test (DFT) techniques are employed in order to facilitate testing and functional verification of the system. First, small but critical circuits are designed into a process control module (PCM) for independent testing. For example, many of the reference circuits have been incorporated into this module in order to identify immediately a bias problem and its source.

Second, many small probe pads were strategically placed throughout the circuit in order to access critical sections of the system. These pads are positioned and sized in order to minimize parasitic loading effects.

Third, bypass test circuitry is incorporated into subsystems so test signals can be injected. For example, the input and output signals to the mixer can be switched to a probe pad for functional verification of the mixer as an independent unit. This DFT technique provides significant information over simple diagnostic probing pads at the expense of only a few transistors and little die area.

The μmechanical devices can be verified by diagnostic structures that are fabricated near the actual system devices. Adequate matching between μmechanical devices is assumed in this design, but a finite absolute error in the target frequency due to process variation is expected. This problem is overcome easily since the devices all exhibit at least 2% tuning with the bias voltage. Therefore the diagnostic structures can be tested in order to determine the actual operation frequency and the bias can be adjusted accordingly.

VI. Conclusion

The design of an integrated MEMS-BiCMOS SINCGARS transceiver has been presented. The system demonstrates the advantage of using μmechanical devices at the system and circuit levels. Specifically, a superior communication system architecture is realized using these devices while theoretical circuit level performance meets or exceeds the performance of comparable technologies that cannot be integrated in the manner described here. Additionally, the software front end to a silicon compiler has been developed for μmechanical resonator and filter synthesis. This software coupled with a mask generation tool could potentially popularize merged MEMS and circuit designs in the future.

Acknowledgment

The authors wish to thank Professor Kurt Metzger for his contributions and insight into the system architecture for SINCGARS, Seungbae Lee for his contributions to the Colpitts oscillator in the synthesizer section of this paper, and Payman Shanjani for the invaluable discussion on free-free beam filter design. Lastly, the encouragement and input from Professor Richard Brown during this design effort was indispensable.

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